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A NOVEL FPGA BASED CONTROL PLATFORM FOR PV FED UNIFIED POWER QUALITY CONDITIONER (PV-FED UPQC)

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ABSTARCT:
The main aim the project is a novel FPGA based control platform for PV fed Unified Power Quality Conditioner (PV-fed UPQC). Power quality problems have become more complex at all level of power system. The power electronic based power conditioning devices can be the effective solution to improve the quality of power supplied to the distributed system. UPQC is custom power device, designed to compensate both source current and load voltage imperfections. In this paper the design of combined operation of unified power quality conditioner and a hybrid power generation is proposed. The proposed system is composed of series and shunt inverters, PV array and WECS connected to DC link which is able to compensate the voltage sag, swell, harmonics and voltage interruption. The operation of PV-UPQC configuration is simulated through Xilinx system generator environment and results are presented

Keywords-Power quality (PQ), Photovoltaic Array (PV), Unified Power Quality conditioner (UPQC), PV-UPQC, Voltage Sag, Swell, FPGA

1. INTRODUCTION

Nowadays, generation of electricity from renewable sources has improved very much. Since most renewable energy sources are intermittent in nature, it is a challenging task to integrate a significant portion of renewable energy resources into the power grid infrastructure. Traditional electricity grid was designed to transmit and distribute electricity generated by large conventional power plants. The electricity flow mainly takes place in one direction from the centralized plants to consumers. In contrast to large power plants, renewable energy plants have less capacity, and are installed in a more distributed manner at different locations. The integration of distributed renewable energy generators has great impacts on the operation of the grid and calls for new grid infrastructure. UPQC was widely studied by many researchers as an eventual method to improve power quality in distribution system. The quality of the electrical power is affected by many factors like harmonic contamination, due to non-linear loads, such as large converters, rectifiers, voltage and current flickering due to arc in arc furnaces, sag and swell due to the switching of the loads etc. One of the many solutions is the use of a combined system of shunt and series active filters like unified power quality conditioner a new member of the custom power family.

This device combines a shunt active filter together with a series active filter in a back to back configuration, to simultaneously compensate the supply voltage and the load current or to mitigate any type of voltage and current fluctuations and power factor correction in a power distribution network. UPQC is able to compensate current harmonics reactive power, voltage distortions and control load flow but cannot compensate voltage interruption because of not having sources. PV-UPQC configuration has increased the complexity of control over conventional UPQC. However many researchers has presented various control schemes for the perfect control of UPQC. Instantaneous reactive power theory; Id-Iq theory; Space vector control are some easy way of UPQC control. Step wise development of control algorithms and its implementation through real-time hardware is a top task. Design of controller in simulation process and its real-time hardware validation requires checking of many compatibility issues; space for dumpingcode etc. So proper validation through verification steps are necessary to remove errors. During simulation also compatibility of the control algorithm code for target hardware is necessary. To address all those issues for algorithm development this paper adopts a novel FPGA method. Xilinx System Generator platform provides a virtual FPGA environment for controller design introducing all features of target hardware.

Simulation results can be achieved through System generator platform and controller code can also be downloaded to the target hardware directly without any compatibility check. Present paper proposes the Photovoltaic systemintegration to the grid through UPQC which makes the system complex. PV-UPQC system is designed in such a way to handle the power quality Issues related to current harmonics; voltage sag/swell and voltage interruption. Control algorithms are discussed for PV-UPQC.Advantages of System generator platform is presented and compared to conventional way for controller development. Xilinx system generator incorporated to simulink environment provides virtual FPGA capability. Simulation results are presented for current harmonics elimination; voltage sag and swell mitigation. Voltage interruption case is also well tackled.

2. PRPOSED SYSTEM

The novel configuration for integration of PVto grid through UPQC is shown in Fig.1. Series APF andShunt APF is connected back to back with DC-Linkcapacitor in between. Photovoltaic systems are connected tothe DC-Link of the UPQC to provide power to utility grid. Photovoltaic systems and UPQC together work in a uniqueway to maintain the power quality in the system. Wheneverthere is any disturbance of current and voltage quality issues;UPQC maintains it with the help of PV. On appearance ofthe voltage sag there is a chance of load voltage drop whichaffects the load operations. SO PV-UPQC combinationmaintains the load voltage by supplying the required voltageto load. Voltage Interruption from the AC main sourceinterrupts the supply of power from the source to the load.But in this case UPQC alone is unable to

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handle thissituation. So Photovoltaic systems connected to theconfiguration provide the required power to the load andmaintains the constant load voltage. Energy security can beachieved through integration of the power system to abackup energy.

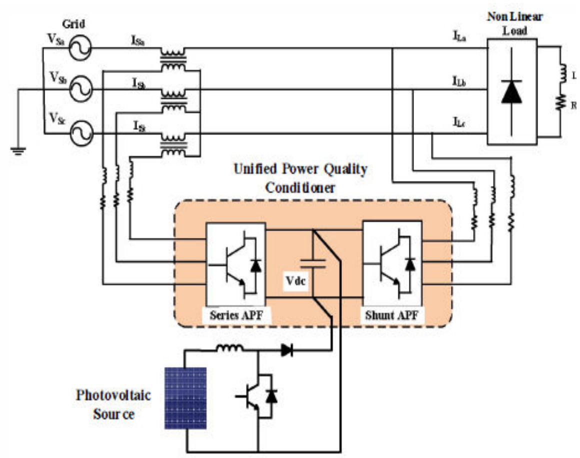

Fig. 1: Block Diagram of PV-UPQC Configuration

3. CONTROL STRATEGY FOR UPQC

PV-UPQC system control steps can be divided tothree major control algorithm types. (i) MPPT control to the PV systems to track maximum power; (ii)Series APF control of UPQC to handle the voltage related power quality issues; (iii) Shunt APF control for current harmonics elimination and maintain of load voltage during interruption. In various literature detail steps and structure of MPPT control is discussed.

3.1 Series APF Control Strategies

For generation of compensating signal power angle control method is introduced. Generation of the Injection angle is divided into three categories. (i) 0° injection angle which require very less voltage magnitude compare to other two cases; (ii) 90° injection angle requires higher voltage magnitude but it does not involve any power sharing with the line voltage (iii) any angle between 0° to 90° which involves real and reactive power transaction. The series voltage injection creates a phase difference between source voltage and load voltage called as power angle. Control of the power angle is done in such a way that that the resultant load voltage magnitude perfectly maintained as the source or any desired voltage.

A phase difference is generated due to the injection voltage from series APF. V_{Series} is the series injected voltage from the series APF. As the load voltage leads the load current also leads by the same power angle. The magnitude of the injected voltage IV_{series}I and the injected angle denoted as I¢$_{series}$I can be represented by the following equations:

$$|V_{series}| = V_s\sqrt{2(1-\cos\delta)}$$

$$|\phi_{series}| = 180 - \tan^{-1}\left(\frac{\sin\delta}{1-\cos\delta}\right)$$

$$\delta = \sin^{-1}(P_L - P_{solar})$$

In the above discussed equations PL is load average power and Pso1ar is PV source power. The series inverter of the UPQC has the capability to eliminate the disturbance created as voltage harmonics; voltage swell on the grid side.

The series inverter control calculates the reference voltage to be injected by the series inverter; comparing the positive-sequence component (Vabc') with the disturbed source voltage (Vsabc).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix}$$

$$\begin{bmatrix} p \\ q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$

The instantaneous real and imaginary power includes AC and DC values and can be expressed as follows

$$p = \overline{p} + \widetilde{p}$$
$$q = \overline{q} + \widetilde{q}$$

3.2 Shunt APF Control Stategies

The voltage provided by the source can be represented as

$$v_s = V_m \sin wt$$

The current drawn by the non linear load

$$i_L| = I_{m1} \sin(wt + \phi_1) + \sum I_{mh} \sin(hwt + \phi_h)$$

The load current contains the fundamental active current and fundamental reactive current as well as the harmonic part added by the nonlinear loads. The Total Harmonic Distortion constitutes the harmonics as well as the reactive part which is required to be removed. The higher order terms represented in (8) can be eliminated by the low pass filter.

On the other hand multiplying *sinwt*both side of equation (8); we get

$$i_L.\sin\omega t =$$
$$\frac{I_{m1}}{2}\cos\phi_1 - \frac{I_{m1}}{2}\cos 2\omega t \cos\phi_1 + \frac{I_{m1}}{2}\sin 2\omega t.\sin\phi_1$$

At the present stage this current is required to be passed through LPF.The generation of active reference current form this filtered out component can be done by multiplying with'2' . Then the result will be the DC Linkcapacitor gives a voltage Vdc; if this value is comparedwith a reference value then it results an error; which is fedto a PI controller. Now the controller results a current le.To get the peak value of the reference current le is addedto active reference current. Now the fundamental activereference current can be reconstitute by again multiplying.All the three phase Load current are sensed andcomputed to result the reference signal as shown in Fig. 2.

4. XILINX SYSTEM GENERATOR METHODOLOGY

System generator tool box is provided by Xilinx tolink the model based MATLAB/Simulink designenvironments to develop FPGA designs. It provides avirtual environment for FPGA designs; Xilinx blocksetpresent in the Simulink library browser provides all therequired design tools present inside an FPGA. Thetraditional FPGA design methodology of RTL; Text benchgeneration is not at all require to develop or to develop thehand written HDL code. All those process is taken care bythe Xilinx system generator tool. Using the Xilinx blockset is as simple as to use the Simulink environmentblocks from the Simulink library browser. Thus Systemgenerator can be used for hardware modelling on anFPGA. The Xilinx blockset contains adders; multipliers;delay; registers; get

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way in; get way out; Filters; FFTs etc.System generator uses the Xilinx ISE preinstalled andlinked to MA TLAB during initial stages. It has the specialability to generate automatically the HDL code for thedesigned model. It automatically goes through the FPGAimplementation steps to generate the bit file which isrequired to download to FPGA kit.

The FPGA architecture consists of three types of configurable elements-

(i) IOBs – a perimeter of input/output blocks

(ii) CLBs- a core array of configurable logic blocks

(iii) Resources for interconnection

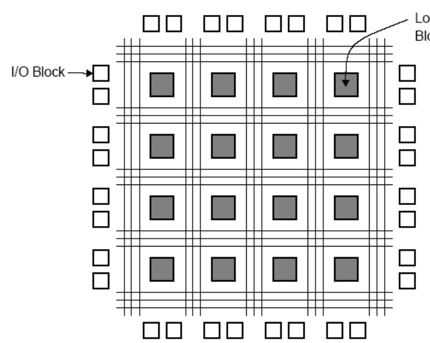
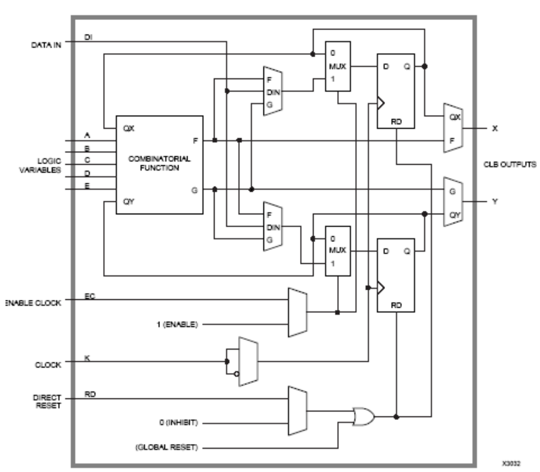
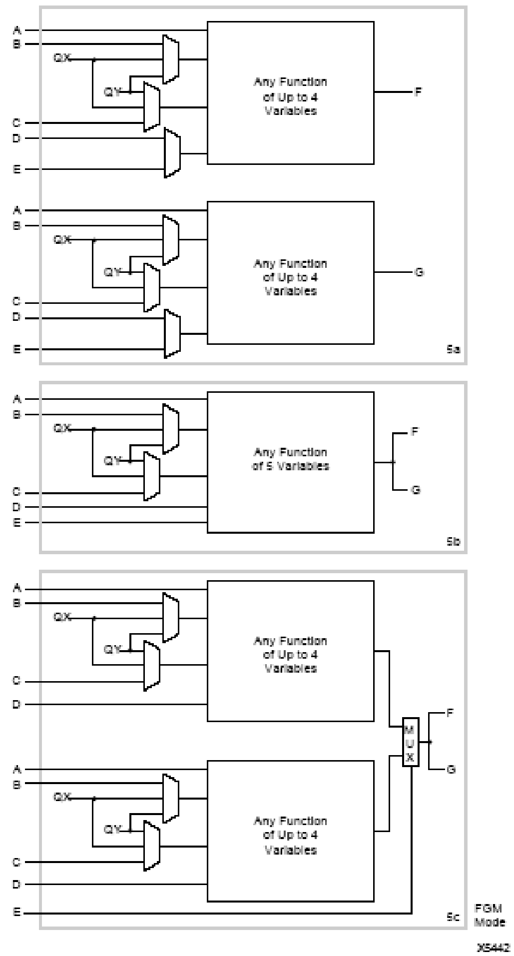


Figure 2 - *Structure of an FPGA.*

Configurable Logic Block:



The following fig shows the three different modes of operation for this block (i)FG mode,(ii)F mode,(iii)FGM mode



FG Mode:

The FG mode generates two functions of four variables each. One variable (A) must be common to both functions. The next two variables can be chosen from B, C, QX and QY. The remaining variable can be either D or E.

F Mode:

The F mode can generate one function of five variables (A, D, E, and two variables chosen from B, C, QX and QY).

FGM Mode: The FGM mode uses a multiplexer with E as a control input to select one of two four-variable functions. Each function inputs A, D and two of the inputs B,

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C, QX, QY. The FGM mode can realize the functions of six or seven variables.

5. SIMULATION RESULTS

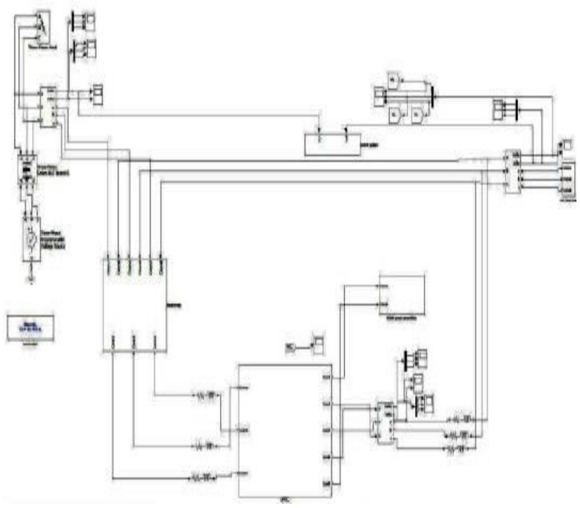
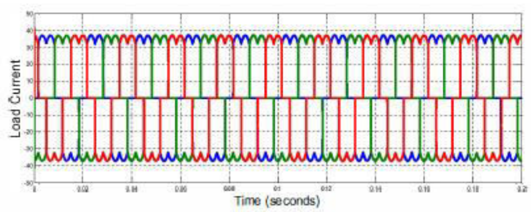
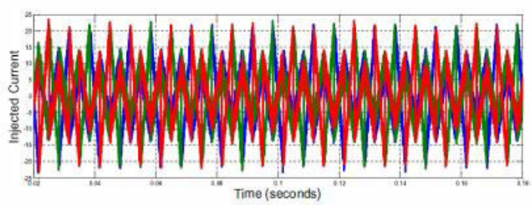


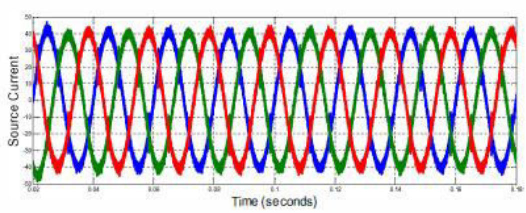
Fig 2. MATLAB/SIMULINK circuit diagram of proposed system



(a)

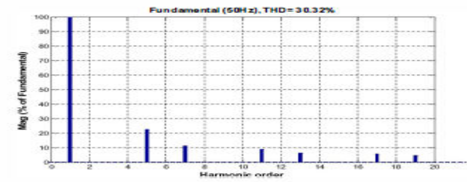


(b)

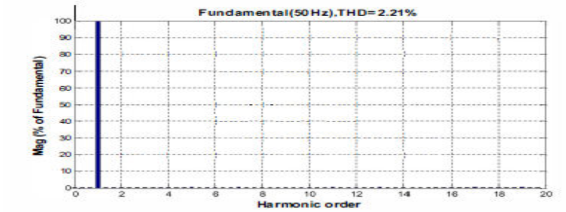


(c)

Fig. 3: Current Waveforms: Load Current (a);
Compensating Current (b); Source Current (c)

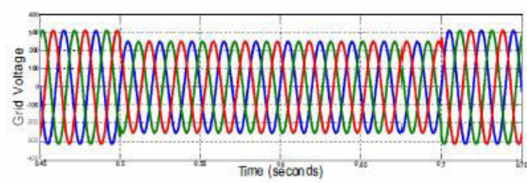


(a)

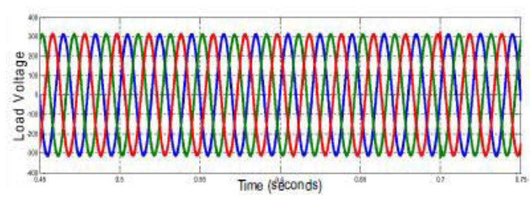


(b)

Fig. 4: FFT Analysis: (a) Load Current THD; (b); Source Current THD

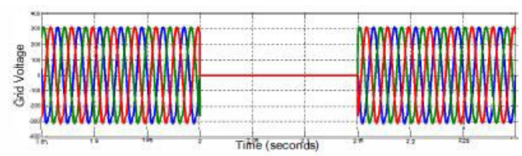


(a)

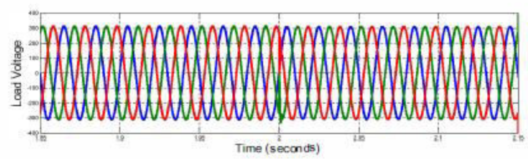


(b)

Fig. 5: Voltage Waveforms: (a) Grid Voltage with sag; (b) Load Voltage
after Sag Removed



(a)



(c)

Fig. 6: Source Voltage Interruption: (a) Grid Voltage Interruption (b)
Load Voltage Maintained by PV-UPQC

5. CONCLUSION

In this paper, the results of analyzing combined operation of UPQC and PV is explained. The proposed system is composed of series and shunt inverters, PV array system which can compensate the voltage sag, swell, interruption, and reactive power and harmonics. The advantage of proposed system is compensating the voltage interruption using UPQC because of connecting distributed generation to DC link. The proposed system can improve the power quality at the point of installation on power distribution system or industrial power systems. The discussed methodology is adopted for controller design Power Quality improvement through PV-UPQC. Various cases of Power Quality improvement is tested through simulation.

REFERENCES

[1] H. Akagi, H. Fuzita, A new power line conditional for harmonic compensation in power system, IEEE Trans. Power Del., vol.10, no.3, pp.1570-1575, Jul.1995.

[2] M.F. Farias, P.E. Battaiotto, Investigation of UPQC for sag compensation in wind farms to weak grid connection, IEEE Conf., .2010.

[3] N.G. Jayanthi, M. Basu, Rating requirement of UPQC to integrate the fixed speed induction generator type wind generation to the grid, IET Renew.PowerGener., vol. 3, iss. 2, pp.133-143, May 2008.

[4] Hurng-LiahngJou; Jinn-Chang Wu; Yao-Jen Chang; Ya-TsungFeng " A novel active power filter for harmonic suppression" IEEETrans on Power DeliverY,voI.20; no.2; pp. 1507-15 I 3. Apri1.2005.

[5] P. Acuna; L. Moran; M. Rivera; J. Dixon "Improved Active PowerFilter Performance for Renewable Power Generation Systems" IEEETrans on Power Delivery,voI.29; no.2; pp. 687-694. Feb. 2014.

[6] Gayadhar Panda; Pravat Kumar Ray; Pratap S Puhan; Santanu KDash "Novel schemes used for estimation of power systemharmonics and their elimination in a three-phase distributionsystem" International Journal of Electrical Power & EnergySystems 53; pp. 842-856; 20 I 3.

[7] H.Fujita and H.Akagi; "The Unified Power Qulaity Conditioner:The integration of shunt and series filters." IEEE Trans on PowerElectron, vol.I 3; no.2; pp. 3 I 5-322.Mar.I 998.

[8] Han; B. Bae "New Configuration of UPQC for Medium-VoltageApplication" IEEE Trans on Power Delivery; VOL. 2 I; NO. 3; pp. 1438-1444; July 2006.

[9] Han,B. Bae; H. Kim and S. Baek; "Combined Operation of UnifiedPower-Quality Conditioner With Distributed Generation" IEEE
Trans on Power Delivery; vol. 2 I; no. I; pp.330-338; Jan 2006.