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Paper Authors

***SANGANI INDRAJA, M SRI MANIKYAMBA.**

* Dept of ECE, Kakinada Institute of Engineering & Technology For Women.

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HIGH PERFORMANCE AND THROUGHPUT AMPLIFIER DESIGN FOR WIRELESS NETWORK

***SANGANI INDRAJA, **M SRI MANIKYAMBA**
*PG Scholar, Vlsi&Es, Dept of ECE, Kakinada Institute of Engineering & Technology For Women, Korangi, A.P.
**Assistant Professor, Dept of ECE, Kakinada Institute of Engineering & Technology For Women , Korangi, A.P.

ABSTRACT:

In this paper, a high gain broadband low noise amplifier with flat power gain is designed for using in the wireless systems in frequency range of 2-5.5 GHz. This LNA is designed employing two pHEMT devices which are in cascode while using current reuse structure. The low noise amplifier which is unconditionally stable in the over frequency range of 2-5.5 GHz, is achieved to have maximum power gain of 28.28 dB at 2.25 GHz. Minimum noise figure of the LNA is 0.939 dB. Maximum of input return loss, output return loss and reverse isolation are less than – 10.15 dB, less than – 10.53 dB and below – 39.18, respectively. The LNA consumes DC power of 54.92 mw. The figure of merit (FOM) of proposed broadband LNA was calculated that shows good improvement compared with other works.

INTRODUCTION:

The noise figure (NF) is a significant parameter for a high frequency amplifier design, the 1st stage of any receiver system has significant influence on the noise operation of total module, so, have a preamplifier with low NF is required, because, simultaneously achievement to minimum NF and maximum power gain is not accomplishable for a high gain LNA, then several trade-off have to be made [1]. A broadband LNA should have flat power gain and excellent input impedance match in the band of interest, achievement to maximum power gain in a narrow frequency range, is possible, although a LNA that is designed with less than maximum power gain, has better bandwidth, but input and output terms of the broadband LNA may be weekly matched [1]. High electron mobility devices have lower noise figures than some other transistors, so they are very excellent for using in LNA design [1]. So in this research, a GaAs pHEMT [2] is used for designing the LNA. In [3], a typical LNA by passive biasing is designed, The LNA schematic is shown in fig. 1.

In the design of proposed LNA, cascode structure is employed. The most important

benefits of cascode topology are low NF, flat and high forward power gain, but this topology has a trouble, its DC power consumption is very high, for solving this trouble, current reuse technique can be used [4]. In the some past researches, cascode topology with an inter-stage matching network, is used. E.g. in [5], in the design of a LNA, the conventional cascode architecture is assumed such as two-stage amplifier and result in an inter-stage impedance matching network is employed [5]. In [6], design of cascode amplifier in the frequency of 60 GHz by CMOS process is reported, the amplifier is implemented using an inter-stage impedance matching network, this network, improve the power gain and make an excellent impedance matching between the CS and the CG devices [6].In the second section of this paper, matching networks structure is discussed. In the third part, circuit techniques, such as current reuse topology and negative feedback is described. In the next section of this paper, schematic design of the proposed high gain broadband LNA, is explained. In 5 th part, simulation results is presented and these results is compared with past designs. In the final, conclusion is described.

System Overview

The main communication standards for short-range and low-power applications are IEEE 802.15.4, IEEE 802.15.6, and Bluetooth Low Energy (BLE). Among these, IEEE 802.15.6 is dedicated to wireless medical body-area networks (MBAN). The US MBAN operates in the 2.4 GHz ISM band ranges between 2.36 and 2.4 GHz, and the Federal Communication Commission (FCC) Part 15 unlicensed 2.4 GHz ranges from 2.4 to 2.5835 GHz, providing 118 channels across both bands. The standard specifies differential quadrature phase-shift keying (DQPSK) operating at a symbol rate of 600 ks/s. The sensitivity of −92 dBm is based on a data rate of 971.4 kb/s, and the required Signal to Noise Ratio (SNR) is 11.2 dB, leading to a maximum Noise Figure (NF) of 19.2 dB for the entire receiver. Moreover, the relaxed adjacent channel rejection ratio (ACRR) of only 9 dB leads, according to the derivation in [16], to the required adjacent channel IIP3 of −55 dBm, which is a very relaxed specification. On the other hand, in order to withstand larger out-of-band blockers, an out-of-band (OOB) IIP3 of −19 dBm is required [16]. Therefore, the requirements of the IEEE 802.15.6 standard (in terms of noise and linearity) are very easy to meet. To take advantage of such relaxed requirements in MBAN applications, designing a receiver with

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ultra-low power consumption is crucial. The first active component of the receiver is the Low Noise Amplifier (LNA), and this can generally be considered to be the most challenging and power-hungry component, due to its performing several significant tasks simultaneously. Firstly, input power matching the 50 Ω source impedance has to be preserved not only to maximize the available power, but also to guarantee proper operation of the external Surface Acoustic Wave (SAW) filters. Secondly, it must add as little noise as possible. Thirdly, the input signal must be amplified to reduce the noise contribution of the subsequent stages in the receiver. Finally, in the receiver chain, the LNA most likely limits the OOB IIP3, and its value has to be at an acceptable level.

3. LITERATURE REVIEW:-

One of the important implementation of Design and noise optimization for a RF low noise amplifier by Ravinder Kumar, Manish Kumar , and Viranjay M. Srivastava in this, they proposed Amplifier is a non-linear characteristics device and causes two main problems one is blocking and other is inter-modulation •Wenjian Chen, Tins Copani, Hugh J. Barnaby, SayfeKiaeiIn the context of A 0.13 um CMOS ultra-low power front-end receiver for wireless sensor networks they proposed feedback techniques to reduce the current consumption while optimizing the input matching and noise performance. • Another importantperformance of the forward-biased RF LNA with deep n-well n-MOS transistor given byS.F. WAN Muhamad Hatta, N. Soin in this they proposedThe common gate transformer feedback transconductance boosting is used to minimized the current consumption then gain is doubled due to the sum of n-mos and p-mostranscondctances. The main function of LNA is mutually dependent on a set of design parameter values. LNA desig

PROPOSED DESIGN:

LNA Modeling and Analysis LNA Core Description Figure 1 shows a two-stage LNA based on the common emitter topology with inter-stage coupling. It is designed for IEEE 802.11a, wireless local area network application. It is powered by one volt power supply. The bias stage utilizes band-gap reference circuit for a low supply voltage and low power dissipation [9]. It controls base currents for first and second stages. It is designed to provide stable band-gap reference voltage for the temperature drift and power supply variation. The simultaneous matching for input and output impedances including the

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effect of the load impedance is considered to reduce RF signal loss. The passives C1, Lb and Le are used for input matching. Lc , C2, Le and Ls are used for inter-stage matching between Q1 and Q2. Ld, C3 and C4 are used for output matching. The complete design consists of three BJTs and one MOS, five inductors, five capacitors and seven resistors all on a single chip

Research methodology to be employed:-

STEP 1:- Selection of MOS Transistor This is the first and the most important step while designing an on chip LOW NOISE AMPLIFIER. The selection of MOS depends on its mobility, so we have selected an enhancement type of n-MOS transistor. The three important parameters in the transistor are Vds ,Vgs and Ids.Values of Vds and Vgs are predetermined. We have to obtain the desired value of Ids which is dependent on W/L ratio of MOS transistor. Since we are using 0.09µm technology, our device length is fixed at 0.09 micrometer. The only parameter on which the Ids depends is "width" of the device.

$$I_{ds} = \left|\frac{\mu n \cdot cox}{2}\right| * \left|\frac{W}{L}\right| * (V_{gs}-V_t)^2$$

Values of µn and Cox are dependent on fabrication process. Since we are using 0.09µm technology Cox = 8.42 fF. For simulation purpose we are using BSIM 3 model, hence the device width is reduced by 20% to 30% of the calculated width.

Step 2- DC Simulation Biasing in electronics is the method of establishing predetermined voltages or currents at various points of an electronic circuit to set an appropriate operating point. The operating point of a device, also known as bias point, quiescent point, or Q-point, is the steadystate operating condition of an active device (a transistor or vacuum tube) with no input signal applied. The importance of DC simulation is to determine the quiescent point of the device MOS. The DC Simulation controller calculates the DC operating characteristics of a design under test (DUT). Fundamental to all RF/Analog simulations, DC analysis is used on allRF/Analog designs. It performs a topology check and an analysis of the DC operating point, including the circuit's power consumption. The simulator computes the response of a circuit to a particular stimulus by formulating a system of circuit equations and then solving them numerically.

The DC simulation accomplishes this analysis as follows:

• Solves a system of nonlinear ordinary differential equations (ODEs)

• Solves for an equilibrium point • All time-derivatives are constant (zero)

• System of nonlinear algebraic equations You can also set up the DC simulation to sweep one or more parameters, enabling you to perform tasks such as verifying model parameters by comparing the simulated DC transfer characteristics (I-V curves) of the model with actual measurements.

We are using a fixed biasing scheme for DC biasing. In self bias and voltage divider bias, resistors are involved, which increase the size and parasitic effect of device. So we are using self bias to optimize the devise.

STEP 3:-

Feedback Network Design Feedback can be either negative or positive. In amplifier design, negative feedback is applied to effect the following properties.

- Desensitize the gain
- Reduce non-linear distortion
- Reduce the effect of noise
- Control the input and output impedance STEP 4:-

S Parameter Analysis

The fact that the average analog engineer is unfamiliar with these concepts (and has probably never used a program like Genesis before), is not a good reason not to learn and use these techniques. It is quite certain that these tools are very useful even if you are designing low frequency circuits. A few of the many reasons this statement is made are:

1) The transistors you use don't know that they are supposed to work only at audio frequencies. They are perfectly happy to oscillate at many GHz if allowed.

2) Genesis (and other programs like it) contains modules that enable you to do EM modeling of things like circuit boards. This can be quite useful in making your circuit EMI hardened (a bane of many analog circuits).

3) These tools provide new insights into analog design broadening your knowledge and capabilities; insights that may help keep you ahead of your competitors. So while understanding s-parameters and having access to tools like Genesis is critical for the RF and high frequency, wide bandwidth analog designer, they are extremely useful for the low frequency analog designer as well. Scattering parameters are all about power; both reflected and incident in a linear two port system. It

assumes that the system must be treated like a transmission line system; lumped elements no longer adequately describe the system. For the following analysis, refer to Figure6.10.

STEP 5:- Noise Figure Analysis Besides stability and gain, another important design consideration for a microwave amplifier is its noise figure. In receiver applications, it is often required to have a preamplifier with as low a noise figure as possible, as the first stage of a receiver front end has the dominant effect on the noise performance of the overall system. The noise figure parameter, N, are given where, the quantities Fmin, Γopt and RN are the characteristics of the transistor being used and are called the noise parameters of the device.

STEP 6:- Impedance Matching

The impedance matching network is lossless and is placed between the input source and the device. The need for matching network arises because amplifiers, in order to deliver maximum power to a load, or to perform in a certain desired way must be properly terminated at both the input and the output ports. The impedance matching networks can be either designed mathematically or graphically with the aid of Smith Chart. Several types of matching networks are available, but the one used in this design is open single stubs whose length is found by matching done using smith chart manual. It is necessary to match this impedance to the impedance of the source driving the circuit. The output impedance must be similarly matched. It is very common to use reactive components to achieve this impedance transformation, because they do not absorb any power or add noise. Thus, series or parallel inductance or capacitance can be added to the circuit to provide an impedance transformation. Series components will move the impedance along a constant resistance circle on the Smith chart.

STEP 7:- Power Analysis

a) Third-Order Intercept Point One of the most common ways to test the linearity of a circuit is to apply two signals at the input, having equal amplitude and offset by some frequency, and plot fundamental output and inter-modulation output power as a function of input power as shown in Figure 5.7. From the plot, the third-order intercept point (IP3) is determined. The third-order intercept point is a theoretical point where the amplitudes of the intermodulation tones at 2V1 – V2 and 2V2 – V1 are equal to the amplitudes of the fundamental tones at V1 and V2. From table 5.1, if V1 = V2 = Vi , then the fundamental is given by

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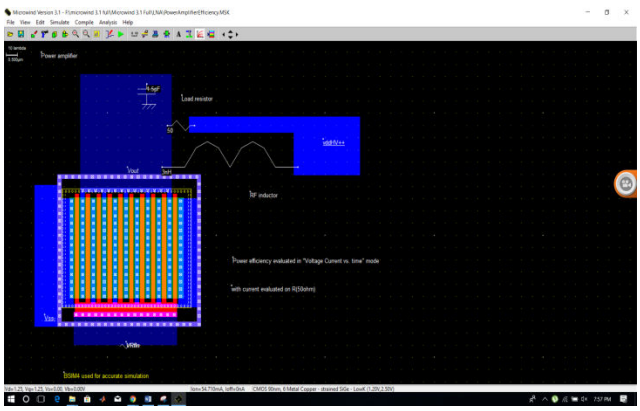
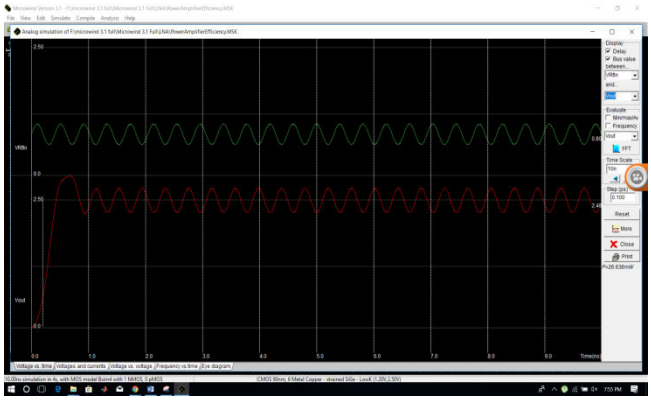
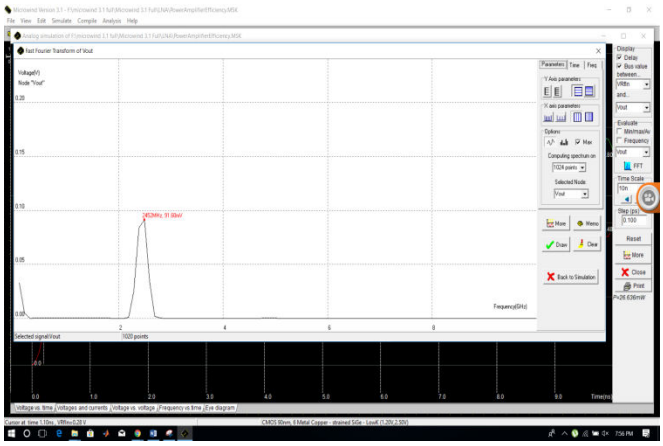
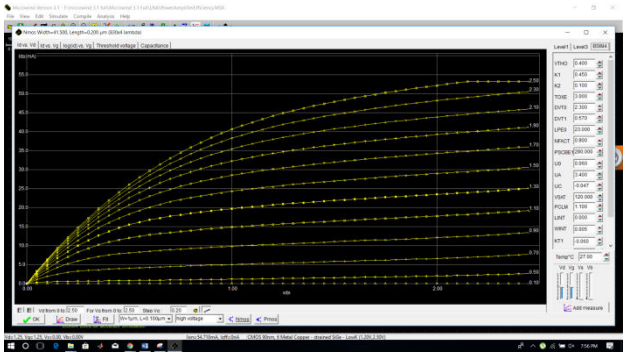
$$F_{und} = k_1 V_i((9/4)k_3 v_i^3)$$

RESULTS AND LAYOUT DIAGRAM FOR POWER AMPLIFIER









CONCLUSIONS

The design methodology and optimization of an ultra-low voltage LNA was presented in this paper. Thanks to the significantly reduced supply voltage and the utilization of transformer-based passive gain boosting, the power consumption of the proposed LNA is as low as 30 µW, while it operates with only 0.18 V supply voltage. The simulation results in 40 nm CMOS technology validate the LNA's functionality with respect to PVT variation, and it shows an NF of 5.2 dB and a voltage gain of 14 dB at the desired frequency. The proposed LNA is suitable for wireless medical body-area networks where the power budget is heavily reduced.

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