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SIMULATION OF CLOSED LOOP CONTROL OF HYBRID BOOSTING CONVERTER FOR PV CELL APPLICATIONS

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Abstract: Conventional sources like fossil fuels were used earlier to satisfy the energy demands. Nowadays these are being replaced by renewable sources like photovoltaic sources. In this paper, a hybrid boosting converter using photovoltaic system with closed loop Control is analyzed and simulated. A new hybrid boosting converter is used to increase the input dc voltage. In Existing method hybrid boosting converter used with one switch in the converter and produce pulses for that switch in open loop. By using the open loop method we get only output as produced amount of input which is given. Then we propose a closed loop method for HBC. By using this closed loop control technique we achieve required output voltage.

Key words: Bipolar voltage multiplier (BVM), hybrid boosting converter (HBC), nature interleaving, renewable energy, single switch single inductor, Induction motor drive.

I. INTRODUCTION

Solar energy is converted to electricity using an electronic device called solar panel using photo-voltaic effect. PV applications can be grouped into utility interactive and stand-alone applications [1]. Utility interactive applications provide a backup system to ensure that electricity is produced throughout the year irrespective of the weather conditions. While stand-alone systems without the utility connection uses the electricity where it is produced [2]. However, to cater to the energy needs during non-sunny and cloudy period PV-charged battery storage system is used. PV systems with batteries can be used to power dc or ac equipment [3-5]. PV systems with battery storage are being used all over the world to power lights, sensors, recording equipment, switches, appliances, telephones, televisions, and even power tools [6]. PV serves as an ideal source using the availability of low DC power requirement for mobile and remote lightning requirements [7]. Systems using several types of electrical generation combine the advantages of each. Engine generators can produce electricity anytime. Thus, they provide an excellent backup for the PV modules, which produce power only during daylight hours, when power is needed at night or on cloudy days. On the other hand, PV operates quietly and inexpensively, and it does not pollute [8]. In this paper a model of closed loop implementation of PI controller for hybrid boosting converter is presented. This controller

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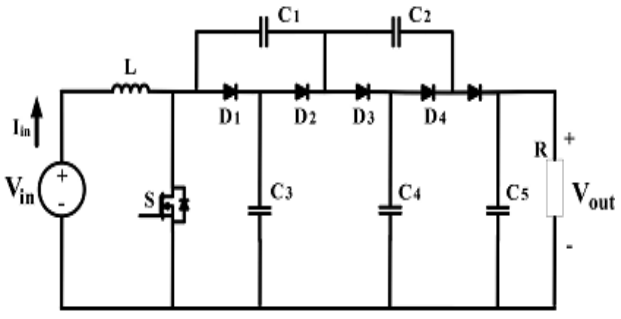
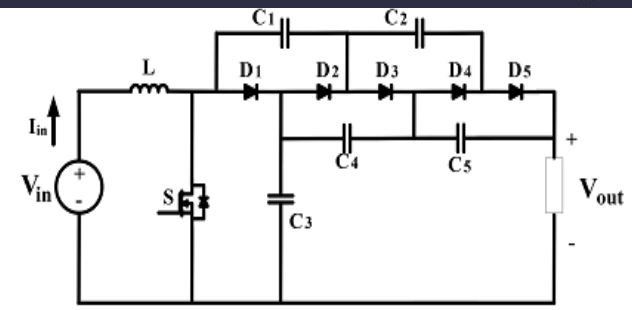
maintains constant output voltage of the converter near to the utility voltage [9-10]. The input voltage to the converter is fluctuating between 20-45V, according to the sunlight intensity on PV cell. MATLAB based simulation is developed with PI controller.The method of combining boost converter with traditional Dickson multiplier and Cockcroft–Walton multiplier to generate new topologies were proposed, such as topologies in Fig.1 (a) and (b). Air core inductor or stray inductor was used within voltage multiplier unit to reduce current pulsation. An elementary circuit employing the super lift technique was proposed and extended to higher gain applications such as Fig.1(c). Its counterpart of negative output topology and double outputs topology were proposed and discussed. The concept of multilevel boost converters was investigated and the topology of Fig.1 (d) was given as central source connection converter. Besides, two switched capacitor cells were proposed and numerous topologies were derived by applying them to the basic PWM dc–dc converters. Typical topologies are shown as Fig.1 (e) and (f). A modified voltage-lift cell was proposed and the topology of Fig.1 (g) was produced. Inspired by the above topologies, a new hybrid boosting converter (HBC) with single switch and single inductor is proposed by employing bipolar voltage multiplier (BVM) in this paper. The second-order HBC is shown as Fig.1 (h).



(a)



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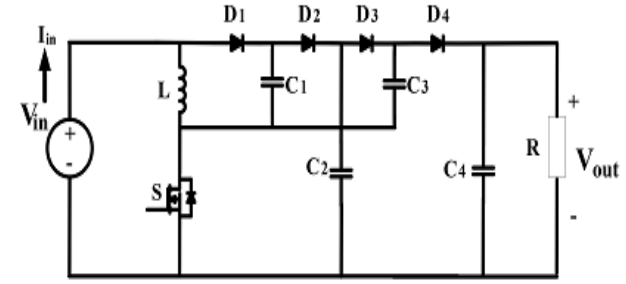

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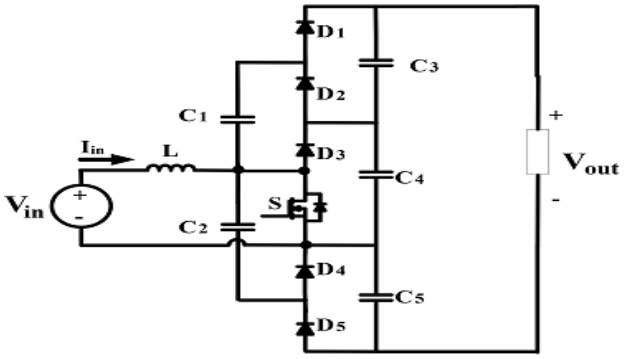

(c)

Fig.1. Previous high-gain dc–dc converters with single-switch single-inductor and proposed topology. (a) Boost + Dickson multiplier [16], (b) Boost + Cockcroft–Walton multiplier [16], (c) super lift with elementary circuit [18], (d) central source multilevel boost converter [21], (e) Cuk derived[22], (f) Zeta derived [22], (g) modified voltage lifter [23], and (h) proposed second-order HBC.

Recently, many more structures achieving higher gain were also reported [26]–[31], but they adopted at least two inductors or switches, or some are based on tapped inductor/transformer, which may complicate the circuit design and increase cost.

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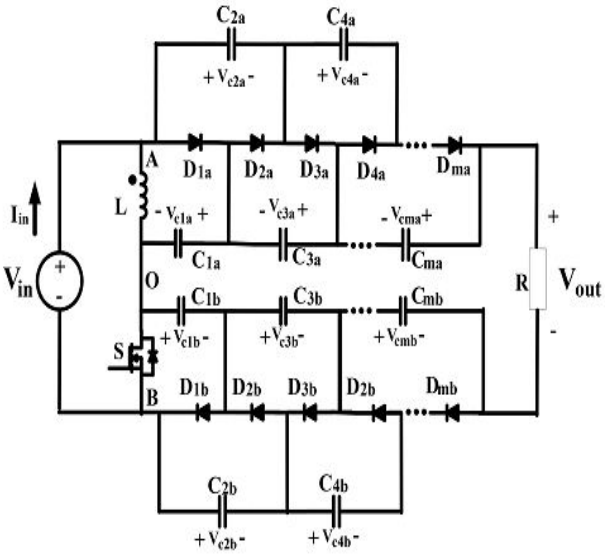
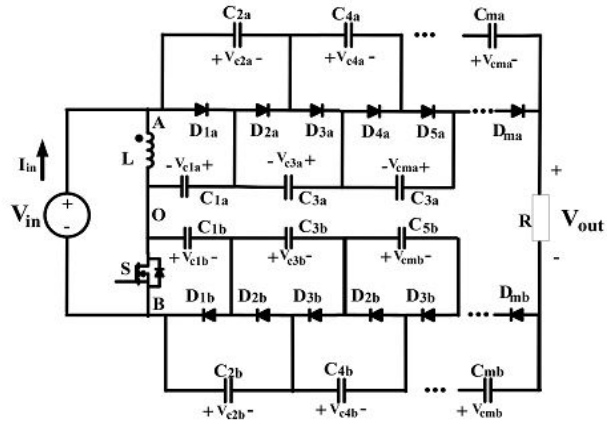
II PROPOSED GENERAL HBC TOPOLOGY AND ITS OPERATIONAL PRINCIPAL

The proposed HBC is shown in Fig.2. There are two versions of HBC, odd-order HBC and even-order HBC as shown in Fig.2 (a) and (b). The even-order topology integrates the input source as part of the output voltage, leading to a higher components utilization rate with respect to the same voltage gain. However, they share similar other characteristics and circuit analysis method. Therefore, only even-order topology is investigated in this paper.



(a)



(b)

Fig.2. Proposed general HBC topology. (a) Odd-order HBC. (b) Even-order HBC.

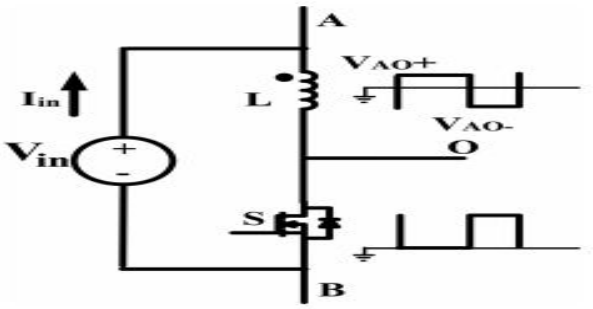


Fig.3. Inductive three-terminal switching core

A. Inductive Switching Core

In a HBC topology, the inductor, switch and input source serve as an "inductive switching core," shown as Fig.3. It can generate two "complimentary" PWM voltage waveforms at port AO and port OB. Although the two voltage waveforms have their individual high voltage level and low voltage level, the gap between two levels is identical, which is an important characteristic of inductive switching core for interleaving operation.

B. BVM

A BVM is composed of a positive multiplier branch and a negative multiplier branch, shown in Fig.4 (a) and (b). Positive multiplier is the same as traditional voltage multiplier while the negative multiplier has the input at the cathode terminal of cascaded diodes, which can generate negative voltage at anode terminal, shown in Fig.4 (b). By defining the high voltage level at input AO as VOA+, the low voltage level as VOA−, and the duty cycle of high voltage level as D, the operational states of the even-order positive multiplier is derived as Fig.5 and illustrated as following:

1) State 1[0, DTs]: When the voltage at port AO is at high level, diodes Dia (i=2k−1, 2k−3...3, 1) will be conducted consecutively. Each diode becomes reversely biased before the next diode fully conducts. There are K sub states resulted as shown in Fig.4 (a). Capacitor

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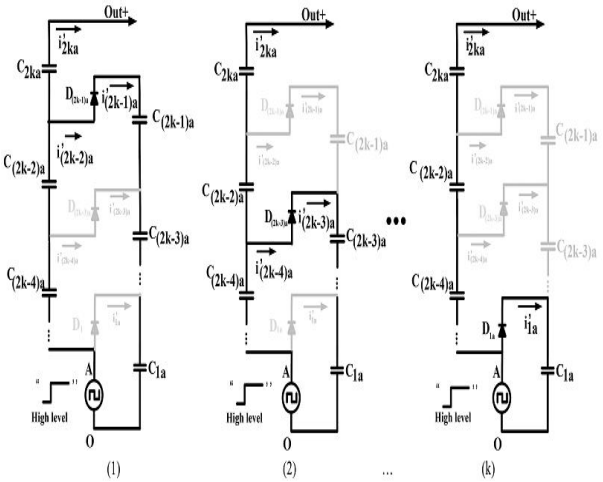
Cia (i=2, 4...2k) are discharged during this time interval. Assuming the flying capacitors get fully charged at steady state and diodes voltage drop are neglected, the following relationship can be derived:

$$V_{c1a} = V_{AO+} \quad (1)$$

$$V_{cia} = V_{c(i+1)a} (i = 2,4,6,...,2k-2) \quad (2)$$

2) State 2[dTs, Ts]: When the voltage at port AO steps to low level, diode D2ka is conducted first, shown as Fig.4 (b)-(1). Then the diodes Dia (i=2, 4, ... 2k−2) will be turned on one after another from high number to low. Each diode will be turned on when the previous one becomes blocked. Only diode D2ka is conducted for the whole time interval of [0, dTs], since capacitor C (2k−1) a has to partially provide the



(a)

Fig.4. Operation modes of even-order BVM positive branch. (a) State 1[0, DTs]. (b) State 2[DTs, Ts]

Load current during the whole time interval. Even though not all the diodes are conducted and blocked at the same time, the flying capacitors still have the following relationship by the end of this time interval:

$$V_{c2a} = V_{c1a} - V_{AO-} \quad (3)$$

$$V_{cia} = V_{c(i+1)a} (i = 3,5,7,\ldots,2k-1) \quad (4)$$

According to charge balance principal, the total amount of electrical charge flowing into capacitors Cia (i=2, 4, ... 2k) should equal to that coming out from them in a switching period at steady state, therefore

$$\sum_{i=1}^{k} \int_{0}^{DT_S} i'_{2ia} dt = \sum_{i=1}^{k} \int_{DT_S}^{T_S} i_{2ia} dt \quad (5)$$

Thus, the capacitor group Cia (i=2, 4...2k) can be replaced by an equivalent capacitor C_{2a} (eq).The diode group Dia (i=2, 4...2k) which provides the charging path for $C_{2a\,(eq)}$ is equivalent to a single diode $C_{2a(eq)}$. Similarly, the capacitor group Cia (i=1,3, ... 2k−1) can be replaced by an equivalent capacitor $C_{1a(eq)}$ and diode group Dia (i= 1,3, ... 2k−1) by $D_{1a(eq)}$. The final equivalent even-order positive multiplier branch is given as Fig.5 (a). A similar analysis yields the equivalent negative multiplier branch as shown in Fig.5 (b). According to (1)–(4), the voltage of equivalent capacitors $C_{1a(eq)}$, $C_{2a(eq)}$ can be expressed as following:

$$V_{c2a(eq)} = k(V_{AO+} - V_{AO-}) \quad (6)$$

$$V_{c1a(eq)} = (k-1)(V_{AO+} - V_{AO-}) + V_{AO+} \quad (7)$$

For the negative branch shown in Fig.5 (b), the following results can be obtained based on similar analysis:

$$V_{c2b(eq)} = k(V_{OB+} - V_{OB-}) \quad (8)$$

$$V_{c1b(eq)} = (k-1)(V_{OB+} - V_{OB-}) + V_{OB+} \quad (9)$$

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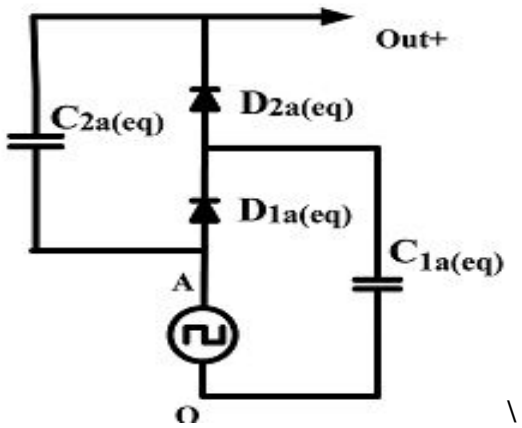
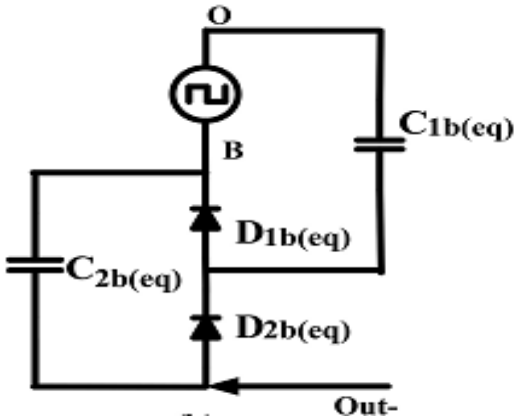


(a)



(b)

Fig.5. Equivalent circuit. (a) Even-order positive multiplier. (b) Even-order negative multiplier

Where $V_{OB}+$ is the high voltage level of input port OB and $V_{OB}-$ is the low voltage level.

3) Equivalent Capacitance Derivation: Assuming capacitors C_{ia} (i=1, 2, 3 ... 2k) have the same capacitance C, in order to derive the equivalent capacitance of $C_{2a(eq)}$ and $C_{1a(eq)}$ in expression of C, a voltage ripple-based calculation method is proposed in this section. Assuming the peak to peak voltage ripple of the flying capacitors can be expressed as ΔVcia (i=1, 2, 3...2k), the ripple of equivalent capacitor $C_{2a\ (eq)}$ is ΔV, the following relationship can be approximated:

$$\Delta V = \Delta V_{c2a} + \Delta V_{c4a} + \dots \Delta V_{c2ka} \quad (10)$$

$$\overline{i'_{ia(\mathrm{on})}} DT_S = \overline{i_{ia(\mathrm{off})}} D'T_S (i = 2, 4, \dots 2k) \quad (11)$$

At the same time, state 1 gives

$$\overline{i'_{ia(\mathrm{on})}} = \overline{i'_{(i+1)a(\mathrm{on})}} (i = 2, 4, \dots 2k-2) \quad (12)$$

State 2 gives

$$\overline{i_{ia(\mathrm{off})}} = \overline{i_{(i+1)a(\mathrm{off})}} (i = 1, 3, \dots 2k-3) \quad (13)$$

Based on the (11)–(13), the following relationship can be obtained:

$$\begin{aligned} \overline{i_{2a(\mathrm{off})}} &= \overline{i_{4a(\mathrm{off})}} = \dots \overline{i_{(2k-4)a(\mathrm{off})}} \\ &= \overline{i_{(2k-2)a(\mathrm{off})}} = \overline{i_{(2k-1)a(\mathrm{off})}} \end{aligned} \quad (14)$$

Based on charge balance of capacitor C_{2ka}, it can be derived that

$$\overline{i_{2(k-1)a(\mathrm{off})}} D'T_S = I_O T_S \quad (15)$$

$$\overline{i_{2ka(\mathrm{off})}} D'T_S = \overline{i'_{2ka(\mathrm{on})}} DT_S = I_o DT_S \quad (16)$$

Where

$$I_o = \frac{V_{\mathrm{out}}}{R}.$$

According to KCL in Fig.4 (b), voltage ripple of capacitors C_{ia} (i=2, 4...2k) can be obtained

$$\begin{cases} C\Delta V_{c2a} = (\overline{i_{2ka(\mathrm{off})}} + \overline{i_{2k-2a(\mathrm{off})}} + \dots \overline{i_{4a(\mathrm{off})}} \\ \qquad + \overline{i_{2a(\mathrm{off})}}) D'T_S \\ C\Delta V_{c4a} = (\overline{i_{2ka(\mathrm{off})}} + \overline{i_{2k-2a(\mathrm{off})}} + \dots \overline{i_{4a(\mathrm{off})}}) D'T_S \\ \qquad \dots \\ C\Delta V_{c2ka} = \overline{i_{2ka(\mathrm{off})}} D'T_S \end{cases} \quad (17)$$

Where

$$D' = 1 - D$$

Based on the equations from (14) to (16), the equation group (17) can be reduced to the following expression:

$$\begin{cases} C\Delta V_{c2a} = (k - 1 + D) I_O T_S \\ C\Delta V_{c4a} = (k - 2 + D) I_O T_S \\ \dots \\ C\Delta V_{c2ka} = (0 + D) I_O T_S \end{cases} \quad (18)$$

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Substituting (10) to (18), the following equation is derived:

$$C\Delta V = \left(\frac{k(k-1)}{2} + kD\right) I_O T_S \quad (19)$$

Meanwhile, the following equation can be derived based on discharging stage of equivalent capacitor $C_{2a(eq)}$

$$C_{2a(eq)}\Delta V = I_O D T_S \quad (20)$$

Based on (19) and (20), the equivalent capacitor $C_{2a\,(eq)}$ can be expressed

$$C_{2a(eq)} = \frac{2D}{k(k-1+2D)}C \quad (21)$$

Similarly, in order to derive the equivalent capacitance of $C_{1a\ (eq)}$, the following equation can be derived:

$$\begin{cases} C\Delta V_{c1a} = kI_O T_S \\ C\Delta V_{c3a} = (k-1)I_O T_S \\ \cdots \\ C\Delta V_{c2(k-1)a} = I_O T_S \end{cases} \quad (22)$$

At the same time, the following equation exists:

$$C_{1a(eq)}\Delta V' = I_O T_S \quad (23)$$

Where

$$\Delta V' = \Delta V_{c1a} + \Delta V_{c3a} + \cdots \Delta V_{c(2k-1)a}.$$

Therefore, the expression of $C_{1a(eq)}$ is obtained

$$C_{1a(eq)} = \frac{2}{(k+1)k}C \quad (24)$$

Because of the symmetry, the equivalent capacitance $C_{1b\ (eq)}$ and $C_{2b\ (eq)}$ is given as following:

$$C_{1b(eq)} = \frac{2}{(k+1)k}C \quad (25)$$

$$C_{2b(eq)} = \frac{2D'}{k(k-1+2D')}C \quad (26)$$

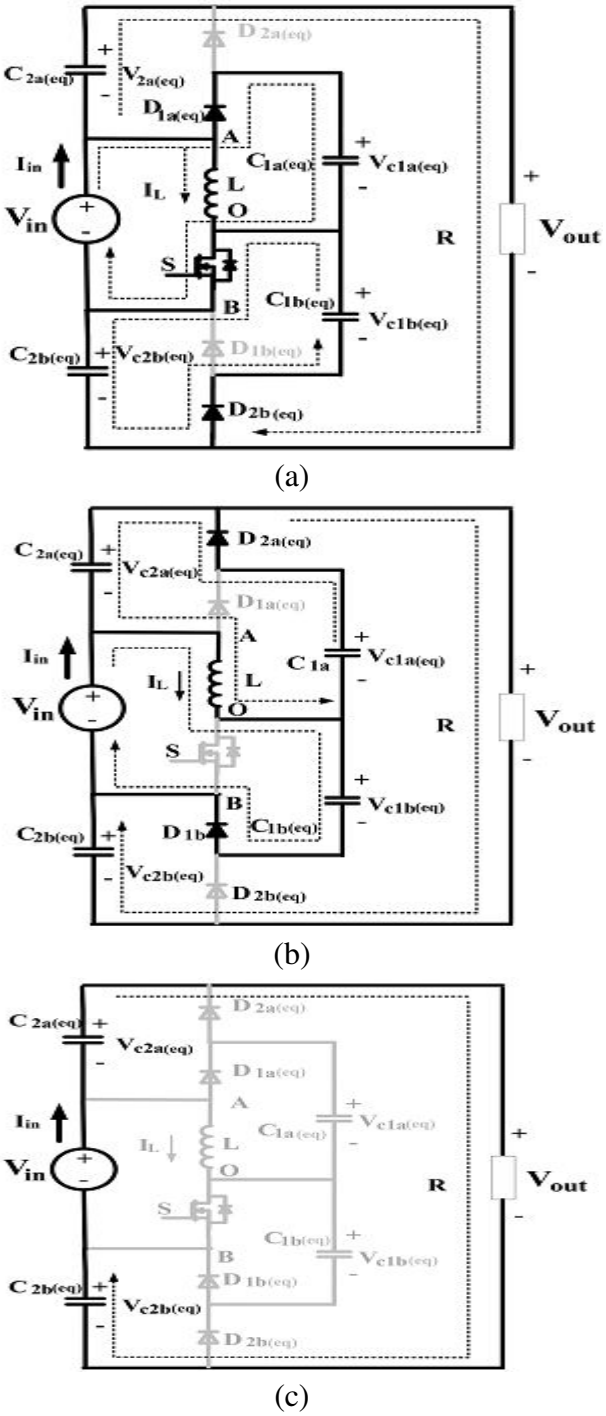

Fig.6. Three operation states. (a) State 1[0, DTs]. (b) State 2[DTs, (D+D1)Ts]. (c) State 3[(D+D1) Ts, Ts]

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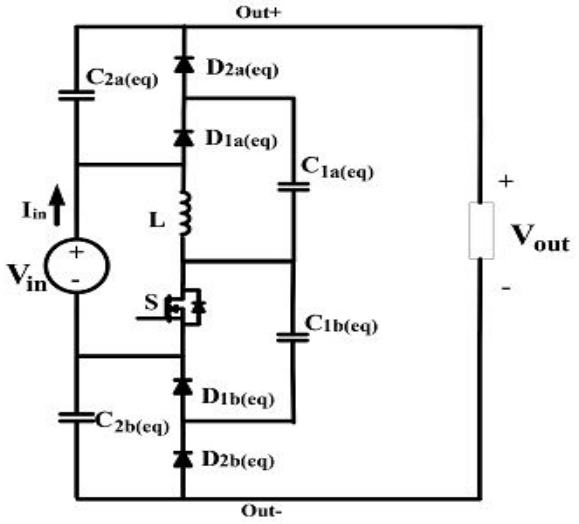

Fig.7. Equivalent even-order HBC

The derivation of voltage and equivalent value of the equivalent flying capacitors can facilitate the output voltage calculation and ripple estimation.

C. Operation Principle of General Basic HBC

Based on the simplification method discussed in previous section, the general even-order HBC in Fig.1 (b) can be simplified to an equivalent HBC circuit, shown as Fig.7. Careful examination of the topology indicates that the two "boost" like sub circuits are intertwined through the operation of the active switch S. The total output voltage of HBC is the sum of the output voltage of two boost sub circuits plus the input voltage.

1) State 1[0, DTs]: In Fig.6 (a), switch S is turned on and diodes $D_{1a\ (eq)}$, $D_{2b\ (eq)}$ conduct while diodes $D_{2a\ (eq)}$ and $D_{1b\ (eq)}$ are reversely biased. The inductor L is charged by the input source. Meanwhile, capacitor $C_{1a\ (eq)}$ is charged by input source and capacitor $C_{2b\ (eq)}$ is charged by capacitor $C_{2b\ (eq)}$. At this interval, the following equations can be derived based on the inductive switching core analysis:

$$V_{AO+} = V_{in} \quad (27)$$

$$V_{OB-} = 0 \quad (28)$$

2) State 2[DTs,(D+D1)Ts]: As illustrated in Fig.6 (b), when S is turned off, the inductor current will free wheel through diodes D2a (eq) and D1b (eq) .The inductor is shared by two charging boost loops. In the top loop, capacitor $C_{1a\ (eq)}$ is releasing energy to capacitor $C_{2a\ (eq)}$ and load at the same time. In the bottom loop, input source charges capacitor $C_{1b\ (eq)}$ through the inductor L. During this time interval, voltage generated at AO and OB is expressed as following based on inductor balance principal:

$$V_{AO+} = -V_{in}\frac{D}{D_1} \quad (29)$$

$$V_{OB+} = \frac{V_{in}(D+D_1)}{D_1} \quad (30)$$

3) State 3[(D+D1) Ts, Ts]: Under certain conditions, the circuit will work under DCM operation mode, thus the third state in Fig.6 (c) appeals. At this state, the switch S is kept off. The inductor current has dropped to zero and all the diodes are blocked. The capacitor C_{2a} *(eq)* and C_{2a} *(eq)* are in series with input source to power the load. During this time interval, voltage generated at port AO is zero while at OB is Vin

$$V_{c2b(eq)} = k\frac{V_{in}}{D'} \quad (31)$$

$$V_{c2a(eq)} = k\frac{V_{in}}{D'} \quad (32)$$

$$\frac{V_{out}}{V_{in}} = 1 + 2k\frac{1}{D'} \quad (33)$$

$$V_{out} = V_{in} + 2kV_{in}\frac{D+D_1}{D_1} \quad (34)$$

$$I_L = I_{D2a(eq)} + I_{D1b(eq)} \quad (35)$$

$$\overline{I_{D2a(eq)}} = \overline{I_{D1b(eq)}} = I_O \quad (36)$$

As current waveforms of $I_{D2a\ (eq)}$ and $I_{D1b\ (eq)}$ should both have triangle shape, they will share

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same peak current value, which is half of the inductor peak current. Therefore

$$I_{D2a(eq)p-p} = I_{D1b(eq)p-p} = \frac{1}{2}\frac{V_{\text{in}}}{L}DT_S \tag{37}$$

The average current of $I_{D2a(eq)}$ in a switching period is I_O, thus

$$\frac{1}{2}D_1T_S\frac{1}{2}\frac{V_{\text{in}}}{L}DT_S\frac{1}{T_S} = I_O \tag{38}$$

$$D_1 = \frac{4I_OL}{V_{\text{in}}T_SD} \tag{39}$$

Substituting (37) to (32), the following equation can be derived:

$$V_{\text{out}} = V_{\text{in}} + 2k\left(V_{\text{in}} + \frac{V_{\text{in}}^2D^2T_S}{4I_OL}\right) \tag{40}$$

Solving the (38) gives the voltage gain in DCM mode

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2k+1+\sqrt{(2k+1)^2+k\frac{2D^2T_SR}{L}}}{2} \tag{41}$$

In order to derive boundary condition for CCM and DCM mode, the average power balance is used

$$V_{\text{in}}(\overline{I_L} + \overline{I_{D1a(eq)}}) = V_{\text{out}}I_O \tag{42}$$

Where

$$\overline{I_{D1a(eq)}} = I_O = \frac{V_{\text{out}}}{R}$$

Thus, the average current of I_L under CCM condition is

$$\overline{I_L} = \frac{2k}{D'}\frac{V_{\text{out}}}{R} \tag{43}$$

The current ripple of inductor is

$$\Delta i_L = \frac{V_{\text{in}}}{2L}DT_S \tag{44}$$

Therefore, the CCM condition is

$$\frac{2k}{D'}\frac{V_{\text{out}}}{R} > \frac{V_{\text{in}}}{2L}DT_S \tag{45}$$

The criteria can be rearranged as

$$\frac{2L}{RT_S} > \frac{DD'^2}{2k(D'+2k)} = K_{\text{crit}}(D) \tag{46}$$

III. PHOTOVOLTAIC SYSTEM

A Photovoltaic (PV) system directly converts solar energy into electrical energy. The basic device of a PV system is the PV cell. Cells may be grouped to form arrays. The voltage and current available at the terminals of a PV device may directly feed small loads such as lighting systems and DC motors or connect to a grid by using proper energy conversion devices this photovoltaic system consists of three main parts which are PV module, balance of system and load. The major balance of system components in this systems are charger, battery and inverter.

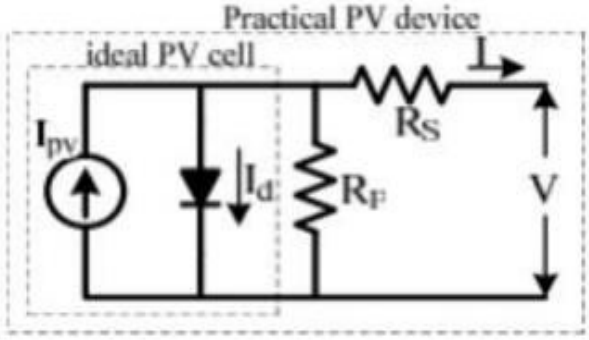

Fig.8 Equivalent circuit of Photovoltaic system.

A photovoltaic cell is basically a semiconductor diode whose p–n junction is exposed to light. Photovoltaic cells are made of several types of semiconductors using different manufacturing processes. The incidence of light on the cell generates charge carriers that originate an electric current if the cell is short circuited.

Fig.9 Characteristics I-V curve of the PV cell.

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The equivalent circuit of PV cell in the above figure the PV cell is represented by a current source in parallel with diode. Rs and Rp represent series and parallel resistance respectively. The output current and voltage form PV cell are represented by I and V. The I-Characteristics of PV cell are shown in fig.9. The net cell current I is composed of the light generated current I_{PV} and the diode current I_D

IV. MATLAB/SIMULINK RESULTS

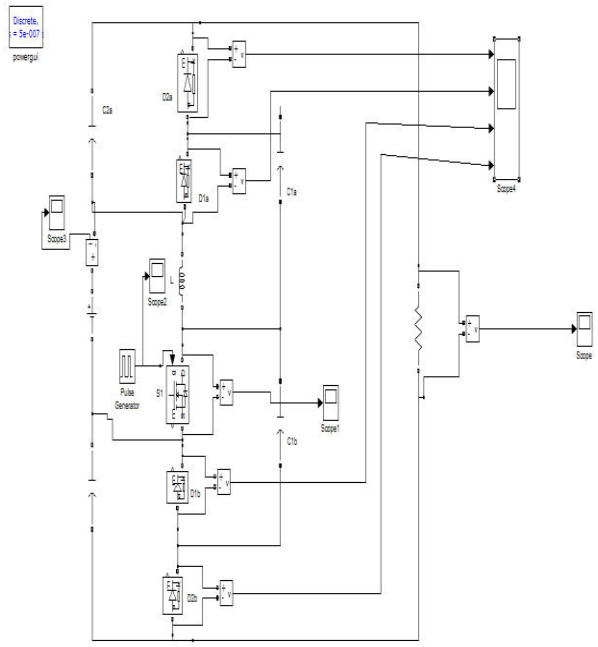
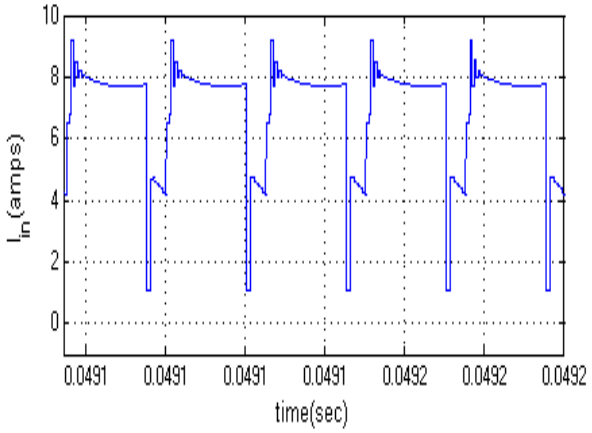
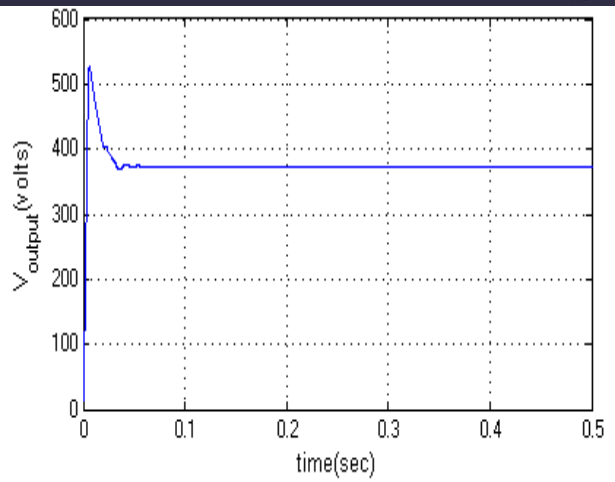
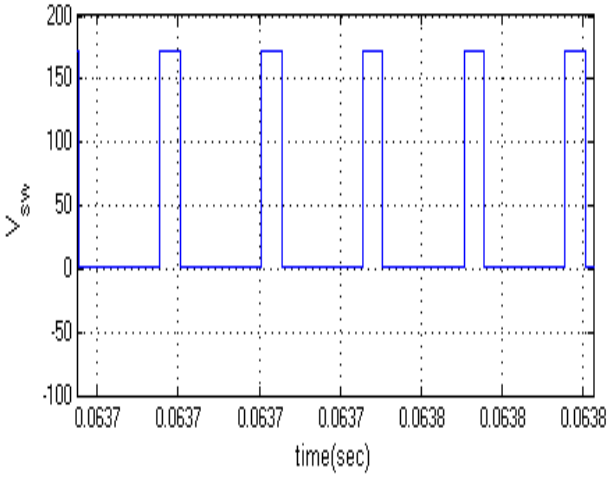


Fig.10 MATLAB/SIMULINK circuit for hydbrid boost convertr







(a)

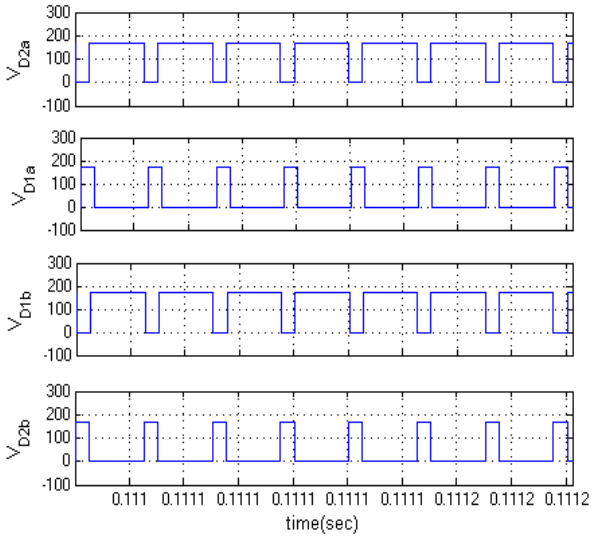


Fig.11 Experimental waveforms. (a)Vds, Iin, Vout, Vin. (b) Diodes voltage: Vd2a, Vd1a, Vd1b, Vd2b.

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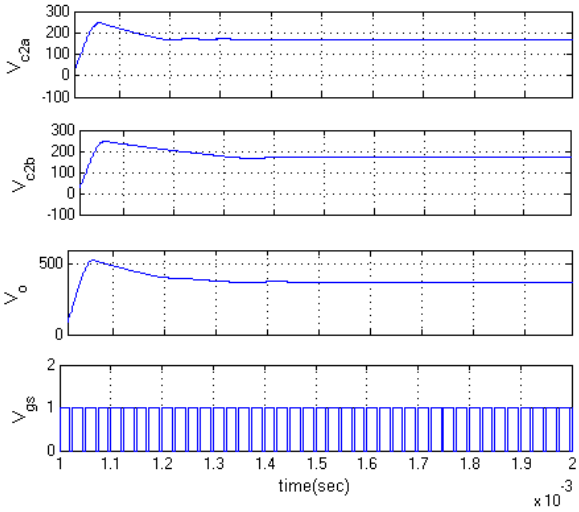

Fig.12. Experimental waveforms of voltage ripples: Vc2a, Vc2b, Vout and driving signal Vgs under (a) D=0.5

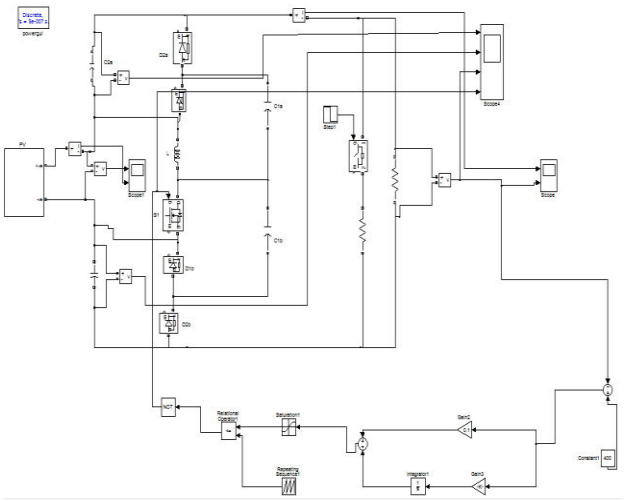

Fig.13 MATLAB/SIMULINK circuit for closed loop control of hydbrid boost convertr with PV system

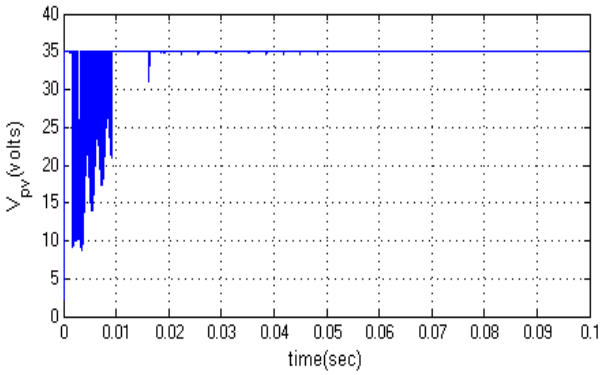

Fig.14 PV Voltage (V)

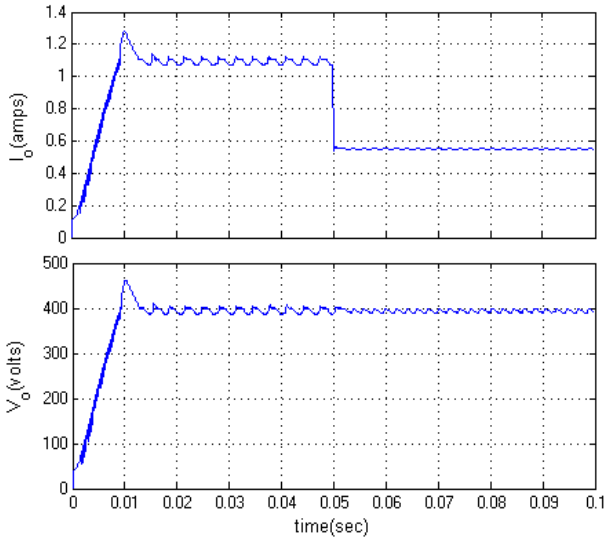

Fig.15 Outputs of Voltage and Current

Sudden Decrease in Load:

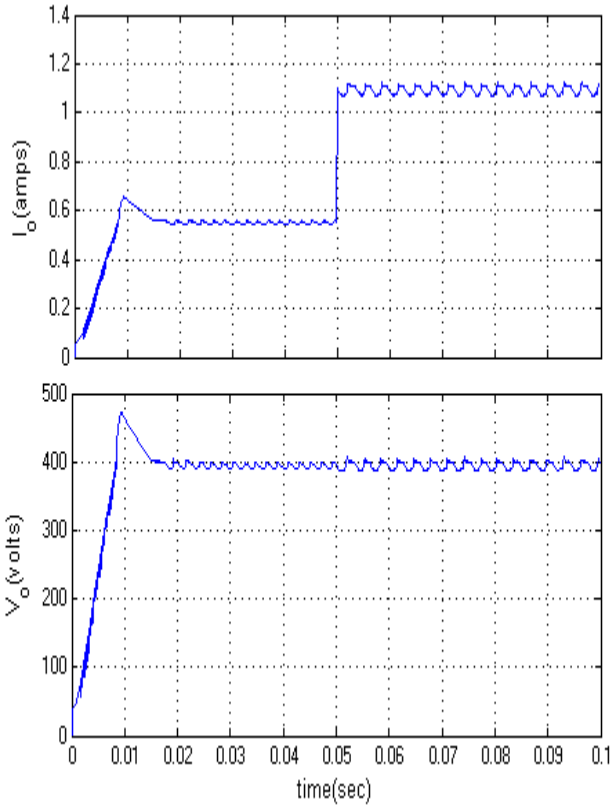

Fig.16 Outputs of Voltage and Current

VI. CONCLUSION

This paper presents a new HBC, used for boosting the input low voltage to high level voltage. In this paper the required amount of voltage is high so we go for close loop or

feedback method by using feedback method we take output voltage as feedback and compare that voltage with reference voltage or required voltage and give to PI controller and we tuned the error and produce pulses for switch which is used in hybrid boost converter. These pulses for switch used in the converter changes according to what amount of output voltage produced but in proposed method we get only one output and change that output because of there is no feedback but in extension method we use feedback we get required amount of voltage until the feedback gives signals and pulses that are changed according to these signals.

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