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HIGH SPEED AND ENERGY EFFICIENT APPROXIMATE ADDER FOR DSP APPLICATION

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Abstract

The aggressive CMOS technology scaling in the sub-100-nm regime leads to highly challenging VLSI design due to the presence of unreliable components. The delay failures in arithmetic units are increasing rapidly due to the increased effect of process variation (PV) in scaled technology. This paper introduces a novel process-tolerant lowpower adder (Prot-LA) architecture for error-tolerant applications. The proposed Prot-LA architecture segments the operands into two parts and computes addition of the upper parts in carry-propagate, whereas it computes the lower parts in a carry-free manner. In the Prot-LA, the number of bits in carry-propagate and carry-free additions can be reconfigured based on the amount of PV. An on-chip PV detector is embedded to determine the PV severity. Because of this reconfigurability, the proposed adder completes the carry propagation with minimum error even under severe process variation. The simulation results show that proposed Prot-LA provides 19.9% reduced power consumption over the state-of-the-art approximate adder. Adders are one of the key components in arithmetic circuits. Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. For applications related to human senses, approximate arithmetic can be used to generate sufficient results rather than absolutely accurate results. Approximate design exploits a tradeoff of accuracy in computation versus performance and power.

Keywords: **Image processing, median filter, SRAM-based FPGA, SEU, configuration memory, soft error.**

1. INTRODUCTION

The addition of two binary numbers is the fundamental and most often used arithmetic operation in microprocessors. In nearly all digital IC designs today, the addition operation is one of the most essential and frequent operations. Instruction sets for DSP's and general purpose processors include at least one type of addition. Other instructions such as subtraction and multiplication employ addition in their

operations, and their underlying hardware is similar if not identical to addition hardware. Often, an adder or multiple adders will be in the critical path of the design, hence the performance of a design will be often be limited by the performance of its adders. When looking at other attributes of a chip, such as area or power, the designer will find that the hardware for addition will be a large contributor to these areas. It is therefore beneficial to choose the correct adder to implement in a design because of the many factors it affects in the overall chip. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. Digital signal Processing (DSP) is finding its way into more applications [19], and its popularity has materialized into a number of commercial processors [18]. Digital signal processors have different architectures and features than general purpose processors, and the performance gains of these features largely determine the performance of the whole processor. Basic operation found in MAC is the binary addition. Besides of the simple addition of two numbers, addition forms the basis for many processing operations, from counting to multiplication to filtering. But also simpler operations like incrimination and magnitude comparison based on binary addition. Therefore, binary addition is the most important arithmetic operation. It comparison based on binary addition. Therefore, binary addition is the most important arithmetic operation. It is also a very critical one if implemented in hardware because it involves an expensive carry-propagation step, the evaluation time of which is dependent on the operand word length.

2. RELATED STUDY:

Approximate computing has been advocated as a new approach to saving area and power dissipation, as well as increasing performance at a limited loss in accuracy. While computation errors are in general not desirable, applications such as multimedia (image, audio and video) processing, wireless communications, recognition, and data mining are tolerant to some errors. Due to the statistical/probabilistic nature of these applications, small errors in computation would not impose noticeable degradation in performance. Generally, there are two types of methodologies for improving speed and power efficiency by approximation. The first methodology uses a voltage-over-scaling (VOS) technique for CMOS circuits to save power. The second methodology is based on redesigning a logic circuit into an approximate version. While the VOS technique is applicable to most circuits for error-tolerant applications, an approximate redesign pertains to the functionalities of different logic circuits. Approximately redesigned adders (simply referred to as approximate adders) are reviewed and a comparative evaluation is performed in this paper.

4. METHODOLOGY

A speculative design makes an adder significantly faster than the conventional design. Segmented adders are proposed. An

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n-bit segmented adder is implemented by several smaller adders operating in parallel. Hence, the carry propagation chain is truncated into shorter segments. Segmentation is also utilized, but their carry inputs for each sub-adder are selected differently. This type of adder is referred to as a carry select adder. Another method for reducing the critical path delay and power dissipation of a conventional adder is by approximating the full adder [2, 17, 20, 24]; the approximate adder is usually applied to the LSBs of an accurate adder. In the sequel, the approximate adders are divided into four categories. As the carry chain is significantly shorter than n in most practical cases, [23] has proposed an almost correct adder (ACA) based on the speculative adder design of [16]. In an n-bit ACA, k LSBs are used to predict the carry for each sum bit (n > k), as shown in Fig. 1. Therefore, the critical path delay is reduced to O(log(k)) (for a parallel implementation such as CLA, the same below). As an example, four LSBs are used to calculate each carry bit in Fig. 1. As each carry bit needs a k-bit sub-carry generator in the design of [16], (n − k) k-bit sub-carry generators are required in an n-bit adder and thus, the hardware overhead is rather high. This issue is solved in [23] by sharing some components among the sub-carry generators. Moreover, a variable latency speculative adder (VLSA) is then proposed with an error detection and recovery scheme [23]. VLSA achieves a speedup of 1.5× on average compared to CLA.

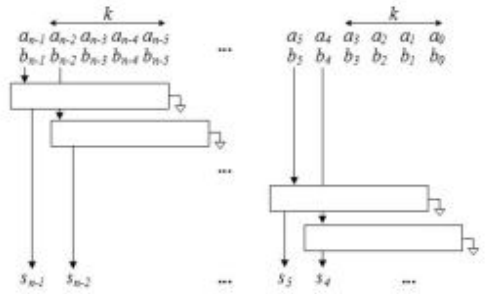

Fig.3.1. Proposed system.

The interconnect of an FPGA is very distinctive than that of a CPLD, however is as a substitute similar to that of a gate array ASIC. In Figure 5.4, a hierarchy of interconnect sources can be seen. There are long strains which may be used to connect important CLBs which might be bodily some distance from every different at the chip without inducing tons put off. They can also be used as buses within the chip. There are also brief traces that are used to attach person CLBs which might be placed bodily close to every different. There is often one or several switch matrices, like that during a CPLD, to attach these lengthy and brief strains collectively in unique methods. Programmable switches within the chip allow the connection of CLBs to interconnect strains and interconnect lines to every different and to the switch matrix. Three-country buffers are used to connect many CLBs to a long line, developing a bus. Special lengthy strains, called international clock strains, are mainly designed for low impedance and therefore rapid propagation times. These are related to the clock buffers and to each clocked element in every CLB. This is how the clocks are dispensed during the FPGA.

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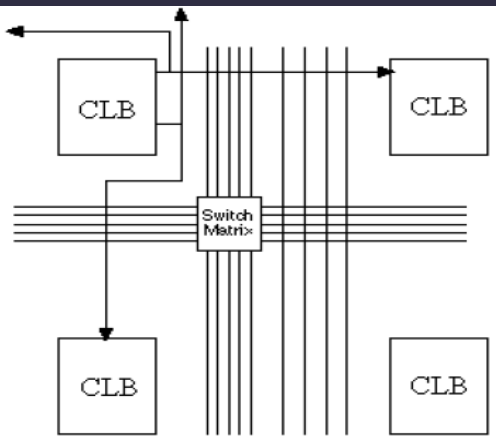

Fig.3.2 FPGA Programmable Interconnect

5. SIMULATION RESULTS

Progress within the fabrication of IC's has enabled us to create speedy and effective circuits in smaller and smaller gadgets. This also way that we are able to percent loads more of functionality into the equal location. The biggest application of this ability is determined within the design of ASIC's. These are IC's which might be created for specific purposes - each tool is created to do a particular process, and do it well. The maximum not unusual software area for that is DSP - sign filters, photograph compression, etc.

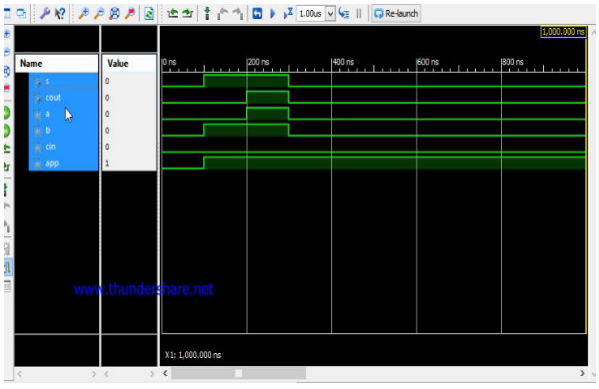

Fig.5.1. Simulation model 1.

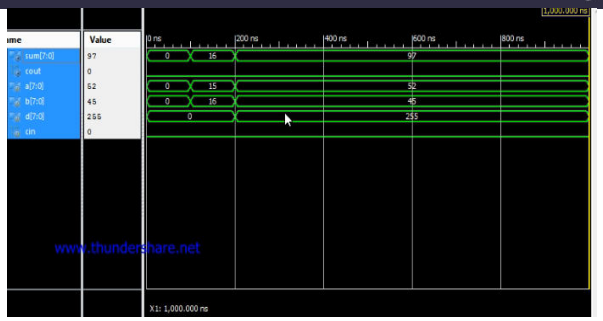

Fig.5.2. simulation model 2.

CONCLUSION

In this paper, we proposed approximate RCPFAs which propagate convey from most large to LSBs. The opposite deliver propagation furnished better stability in postpone variant. The efficacy of the proposed approximate FAs and the hybrid adders which found out them has been studied in 45-nm era. The outcomes indicated that making use of the proposed RCPFAs inside the hybrid adders affords, on average, 27%, 6%, and 31% postpone, energy, and EDP improvement. In addition, the proposed RCPFAs had been hired in FIR filter and DCT of the JPEG compression to evaluate the accuracy and efficiency of the proposed shape in DSP programs. The results showed that the use of the proposed approximate FAs supplied, on common, 60% and 39% power financial savings in DCT of the JPEG and FIR filter out applications, respectively.

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