

ARM7 BASED WIRELESS INDUSTRY DATA ACQUISITION SYSTEM

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Abstract—

In this project concern with designing and implementing multichannel data acquisition system which can be utilized effectively to reduce the human effort and accuracy of measurement of data. The data acquisition system is the base of automation technologies. The traditional signal acquisition systems are mostly by wire, i.e., the sensor connected acquisition system by cable, when measuring point is dispersed and hidden, especially when we control and monitor large complex equipment, it needs a large number of cabling work, and each measurement can only be concentrated in one area, otherwise, it has a very long connection cable, and a long connection cable will introduce a large number of noise and interference. The main aim behind this work is to make the instrumentation stream more power full by enabling it modern communication technologies. Here we are designing portable embedded solution which can be fixed to any real time running machines blast furnace, heater containments

etc. The temperature and the time will be formed as a packet and will be transmitted using a zigbee module.

I. INTRODUCTION

Process control is an efficient means of improving the operation of a process, the productivity of a plant, and the quality of products. In process engineering, even a small improvement in the operation of a process can have great economic and environmental influences. The pace of technology increased dramatically over the next few years forcing companies to evaluate their expectations of product life cycles.

The critical window of opportunity for any new product or project has become one of the main driving forces in industry today. More and more engineers turned to the wireless as the tool to help their time to market. Using the WIFI wealth of hardware expansion and software tools they have reduced the need to 're-invent the wheel' and were able to focus on the critical

hardware and software required to complete their projects.

This Project deals with development of multi-channel analog data through a WIFI. And a MAX 232 chip to convert the RS232 signal. The and lpc2148 each consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry. The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder.

2 LITERATURE SURVEY

Kanchan Mahajan: “Waste Bin Monitoring System Using Integrated Technologies” There are a number of techniques which are purposefully used and are being build up for well management of garbage or solid waste. Zigbee and Global System for Mobile Communication (GSM) are the latest trends and are one of the best combination to be used in the project. Hence, a combination of both of these technologies is used in the project. To give a brief description of the project , the sensors

are placed in the common garbage bins placed at the public places.

Islam, M.S: “Solid waste bin detection” The increasing requirement for Solid Waste Management (SWM) has become a significant challenge for municipal authorities. A number of integrated systems and methods have introduced to overcome this challenge. Many researchers have aimed to develop an ideal SWM system, including approaches involving software-based routing, Geographic Information Systems (GIS), Radio-frequency Identification (RFID), or sensor intelligent bins. Image processing solutions for the Solid Waste (SW) collection have also been developed; however, during capturing the bin image, it is challenging to position the camera for getting a bin area centralized image.

3 BLOCK DIAGRAM

3.1 INTRODUCTION:

This chapter provides the information about the project block diagram, its description and working. The block diagram is the representation of the project

model. It provides the list of the hardware which are required for the project. Based on this, we need to select the hardware components with proper characteristics. Here the major issue is depending upon the result the components should be selected and are assembled in an appropriate manner. The circuit description is stated below.

3.2 BLOCK DIAGRAM:

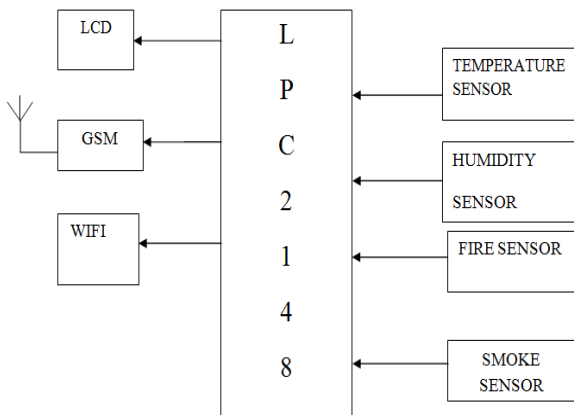


Fig 3.1: Block Diagram

3.3 BLOCK DIAGRAM DESCRIPTION:

LPC2148: Micro controllers based on a 32/16 bit ARM7TDMI-S CPU with real time

emulation and embedded trace support, that combines the micro controller with embedded high speed flash memory.

LCD: Liquid crystal display is used to display the result legibly.

ZIGBEE: Bluetooth and Wi-Fi should not be confused with Zgbee.

TEMPERATURE SENSOR: It can measure temperature more accurately.

HUMIDITY SENSOR: It can measure water moisture in air.

LIGHT SENSOR: We can measure the light intensity.

GSM: Global system for mobile communications is a globally accepted standard for digital cellular communication.

FIRE SENSOR: Fire sensor The Fire sensor, as the name suggests, is used as a simple and compact device for protection against fire. The module makes use of IR sensor and comparator to detect fire up to a range of 1 - 2 meters depending on fire density.

WI-FI: The ZG2100 single-chip 802.11b transceiver includes MAC, baseband, RF and power amplifier, and built in hardware support for AES, and TKIP (WEP, WPA,WPA2 security).

3.4 CIRCUIT IMPLEMENTATION:

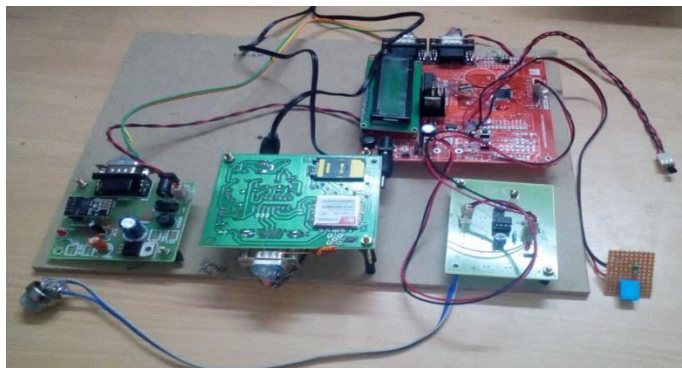


Fig 3.2:Tool kit

- Switch on the power supply.
- Bridge type full wave rectifier is used to rectify the ac output of secondary of 230/12v step down transformer.
- 7805 three terminal voltage regulator is used for voltage regulator.
- This voltage supply of 5 volts dc is given to the microcontroller.
- Here I am using LPC2148 microcontroller. Its acts as a control unit.

- WI-FI module is also interfaced through serial communication.
- parameter values can be measured from the message alerts.
- The device is LCD displaying the sensors values and ON and OFF values through sending from the sensors.

4 Hardware Components

4.1 INTRODUCTION:

This chapter consists of all the hardware components required for the project implementation. The component selection place in a vital role in the result. Some of the project components are ARM processor, LCD, light sensor, humidity sensor, temperature sensor.

4.2 MICROCONTROLLER(ARM7):

4.2.1 INTRODUCTION:

- The ARM7 family includes the ARM7TDMI, ARM7TDMI-S, ARM720T, and ARM7EJ-S processors. The ARM7TDMI core is the industry's most widely used 32-

bit embedded RISC microprocessor solution. Optimized for cost and power-sensitive applications, the ARM7TDMI solution provides the low power consumption, small size, and high performance needed in portable, embedded applications.

- The ARM7EJ-S processor is a synthesizable core that provides all the benefits of the ARM7TDMI low power consumption, small size, and the thumb instruction set while also incorporating ARM's latest DSP extensions and enabling acceleration of java-based applications. Compatible with the ARM9™, ARM9E™, and ARM10™ families, and Strong-Arm® architecture software written for the ARM7TDMI processor is 100% binary-compatible with other members of the ARM7 family and forwards-compatible with the ARM9, ARM9E, and ARM10 families, as well as products in Intel's Strong ARM and x scale architectures. This gives designers a choice of software-compatible processors with strong price-

performance points. **4.3ARM7**

TDMI:

- The ARM7TDMI core uses a three-stage pipeline to increase the flow of instructions to the processor. This allows multiple simultaneous operations to take place and continuous operation of the processing and memory systems. The instructions are executed in three stages: fetch, decode and execute.

5 SERIAL COMMUNICATIONS

5.1 INTRODUCTION:

Computers transfer data in two ways: parallel and serial. In parallel data transfers, often 8 or more lines (wire conductors) are used to transfer data to a device that is only a few feet away. Examples of parallel transfers are printers and hard disk; each uses cables with many wire strips. Although in such cases a lot of data can be transferred in a short amount of time by using many wires in parallel, the distance cannot be great. To transfer to a device located at many meters away, the serial method is used. In serial communication, the data is sent one bit at a time, in contrast to parallel

communication, in which the data is sent a byte or more at a time.

5.2 RS232 STANDARDS:

To allow compatibility among data communication equipment made by various manufacturers, an interfacing standard called RS232 was set by the Electronics Industries Association (EIA) in 1960. Today, RS232 is the most widely used serial I/O interfacing standard. However, since the standard was set long before the advent of TTL logic family, its input and output voltage levels are not TTL compatible. In RS232, a 1 is represented by -3 to -25V, while a 0 bit is +3 to +25V, making -3 to +3 undefined. For this reason, to connect any RS232 to a microcontroller system we must use voltage converters such as MAX232 to convert the TTL logic levels to the RS232 voltage levels, and vice versa. MAX232 IC chips are commonly referred to as line drivers.

5.2.1 DB-9 CONNECTOR:

Since not all the pins are used in PC cables, IBM introduced the DB-9 version of the serial I/O standard, which uses 9 pins only, as shown in the following table:

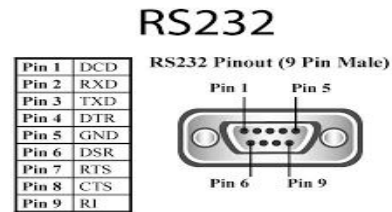


Fig 5.1: RS232 pin configura

PIN	DESCRIPTION
1	Data carrier detect (DCD)
2	Received data (RxD)
3	Transmitted data (TxD)
4	Data terminal ready (DTR)
5	Signal ground (GND)
6	Data set ready (DSR)
7	Request to send (RTS)
8	Clear to send (CTS)
9	Ring indicator (RI)

Table 5.1: Pin Description of DB-9 Connector

The D-subminiature or D-sub is a common type of electrical connector used particularly in computers. At the time of introduction they were some of the smaller connectors used on computer systems. A D-sub contains two or more parallel rows of pins or sockets usually surrounded by a D-shaped metal shield that provides

mechanical support, some screening against electromagnetic interference, and ensures correct orientation.

5.3 MAX232:

The MAX232 is an integrated circuit that converts signals from an RS-232 serial port to signals suitable for use in TTL compatible digital logic circuits. The MAX232 is a dual driver/receiver and typically converts the RX, TX, CTS and RTS signals.

5.3.1 PIN DIAGRAM OF MAX232:

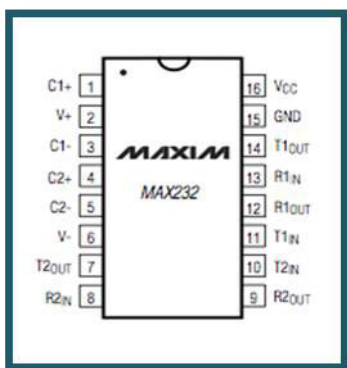


Fig 5.2: Pin

Diagram of MAX232

RS232 interfaced to MAX232:

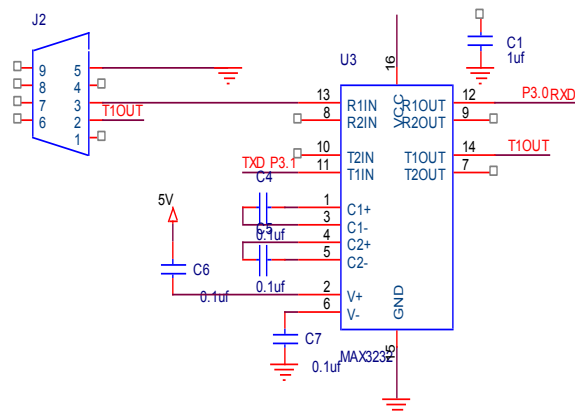


Fig 5.3: RS232

Interfaced to MAX232

RS232 is 9 pin db connector, only three pins of this are used ie 2,3,5 the transmit pin of RS232 is connected to Rx pin of MAX232.

5.3.2 VOLTAGE LEVELS:

It is helpful to understand what occurs to the voltage levels. When a MAX232 IC receives a TTL level to convert, it changes a TTL Logic 0 to between +3 and +15V, and changes TTL Logic 1 to between -3 to -15V, and vice versa for converting from RS232 to TTL. This can be confusing when you realize that the RS232 Data Transmission voltages at a certain logic state are opposite from the RS232 Control Line voltages at the same

logic state. To clarify the matter, see the table below.

RS232 Line Type & Logic Level	RS232 Voltage	TTL Voltage to/from MAX232
Data Transmission (Rx/Tx) Logic 0	+3V to +15V	0V
Data Transmission (Rx/Tx) Logic 1	-3V to -15V	5V
Control Signals (RTS/CTS/DTR/DSR) Logic 0	-3V to -15V	5V
Control Signals (RTS/CTS/DTR/DSR) Logic 1	+3V to +15V	0V

Table 5.2:

TTL Logic Levels

5.4 SERIAL COMMUNICATION IN LPC2148:

UART uses TxD(Transmit) Pin for sending Data and RxD(Receive) Pin to get data. UART sends & receives data in form of chunks or packets. These chunks or packets are also referred to as ‘transmission

characters’. The structure of a UART data packet is as shown below:

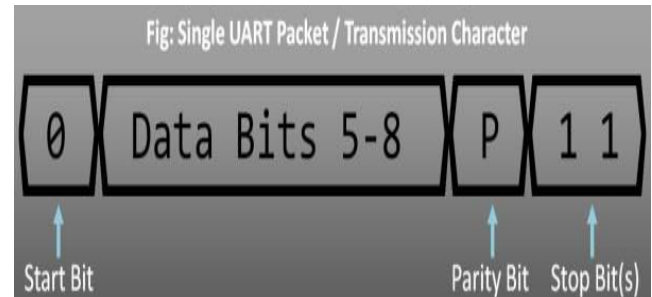


Fig 5.4: Single UART packet/Transmission Character

LPC214x has 2 UART blocks which are UART0 and UART1. For UART0 the TxD pin is P0.0 and RxD pin is P0.1 and similarly for UART 1 the TxD pin is P0.8 and RxD pin is P0.9 as shown in the table below:

Pins:	TxD	RxD
UART0	P0.0	P0.1
UART1	P0.8	P0.9

Table

5.3:UART pins

Data related registers:

- 1) U0RBR – Receiver Buffer Register (READ ONLY!)

This register contains the top most byte(8-bit data chunk) in the Rx FIFO i.e the oldest received data in FIFO. To properly read data from U0RBR , the DLAB(Divisor Latch Access) bit in U0LCR register must be first set to 0.

2) U0THR – Transmit Holding Register (WRITE ONLY!)

U0THR contains the top most byte in Tx FIFO and in this case it's the newest (latest) transmitted data. As in the case with U0RBR, we must set DLAB=0 to access U0THR for write operation.

Baud Rate Setup related registers:

1) U0DLL and U0DLM – Divisor Latch registers

Both of them hold 8-bit values. These register together form a 16-bit divisor value which is used in baud rate generation which we will see in later section. U0DLM holds the upper 8-bits and U0DLL holds the lower 8-bits and the formation is “[U0DLM:U0DLL]“. Since these form a divisor value and division by zero is invalid, the starting value for U0DLL is 0x01 (and not 0x00) i.e the starting value in combined formation is “[0x00:0x01]” i.e 0x0001.

2) U0FDR – Fractional Divider Register

This register is used to set the prescale value for baud rate generation. The input clock is the peripheral clock and output is the desired clock defined by this register. This register actually holds to different 4-bit values (a divisor and a multiplier) for prescaling which are:

Control status registers:

1) U0FCR – FIFO Control Register

Used to control Rx/Tx FIFO operations.

1. **Bit 0 – FIFO Enable** 1 to enable both Rx and Tx FIFOs and 0 to disable.
2. **Bit 1 – Rx FIFO Reset** Writing a 1 will clear and reset Rx FIFO.
3. **Bit 2 – Tx FIFO Reset** Writing a 1 will clear and reset Tx FIFO.
4. **Bits [7 to 6]** Used to determine that how many UART0 Rx FIFO characters must be written before an interrupt is activated.
[00] (i.e trigger level 0) for 1 character.
[01] (i.e trigger level 1) for 4 characters.
[10] (i.e trigger level 2) for 8

characters.

[11] (i.e trigger level 3) for 14 characters.

5. Others bits are reserved.

2) U0LCR – Line Control Register

Used to configure the UART block (i.e the data format used in transmission).

1. Bit [1 to 0] – Word Length

Select: Used to select the length of an individual data chunk. [00] for 5 bit character length. Similarly [01], [10], [11] for 6, 7, 8 bit character lengths respectively.

2. **Bit 2 – Stop bit select:** 0 for using 1 stop bit and 1 for using 2 stop bits.

3. **Bit 3 – Parity Enable:** 0 to disabled Parity generation & checking and 1 to enable it.

4. **Bit [5 to 4] – Parity Select:** [00] to Odd-parity, [01] for Even-parity, [10] for forced “1” (Mark) parity and [11] for forced “0” (Space) parity.

5. **Bit 6 – Break Control:** 0 to disable break transmission and 1 to enable it. TxD pin will be

forced to logic 0 when this bit is 1!

6. Bit 7 – Divisor Latch Access

bit: 0 to disable access to divisor latches and 1 to enable access.

5.5 WIFI MODULE(ZG2100M):

The ZG2100 single-chip 802.11b transceiver includes MAC, baseband, RF and power amplifier, and built in hardware support for AES, and TKIP (WEP, WPA,WPA2 security). The device has an API targeted for embedded markets so an operating system is not required for operation. There is a fully integrated radio ideal for 1 & 2Mbps operation with optional support for external PA and antenna switch operation.

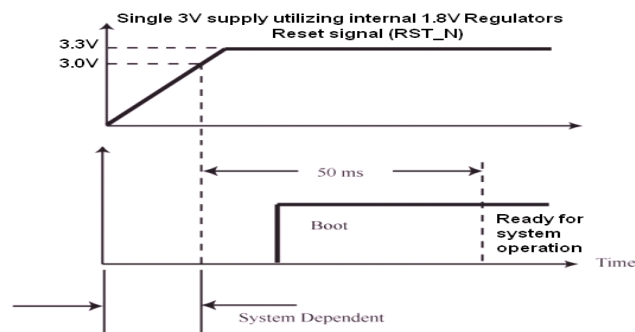


Fig 5.5:ZG2100M/ZG2101M ROM Boot Sequence Timing

5.5.1 ZG2100 POWER STATES:

Please refer to “Application Note 101 - Power-Up Reset Characteristics” for more information. The power state definitions are as follows:

	VDD33	VDD18	CE_N	Circuitry
OFF	0V	0V	0V	Power disconnected to ZG2100
HIBERNATE	3.3V		3.3V	All internal circuitries are OFF
SLEEP	3.3V		0V	Reference clock and internal bias circuitry are ON
RX ON	3.3V		0V	Receive circuits are ON
TX ON	3.3V		0V	Transmit circuits are ON
STANDBY				Transition State Only

Fig 5.6: ZG2100 power states

states

5.5.2 SPI INTERFACE:

SPI Slave Interface with Interrupt for Host:

Operation:

The slave Serial Peripheral Interface Bus (SPI) is used to interface with the HOST. The slave SPI interface works with ZG2100M/ZG2101M Interrupt line (INT_NX). When data is available for the HOST during operation, the INT_NX line is asserted low by ZG2100. The INT_NX line is de-asserted high, by ZG2100M/ZG2101M, after the data is

transferred to the HOST SPI buffer. The SPI CLK Speed can be up to 25MHz.

SPI Timing Characteristics

Single VCC = 3.3V (+/-10%)

Characteristic	Min	Max
SPI, Data setup to falling clock	1 ns	
SPI, Data hold from falling clock	1 ns	
SPI SLAVE CLK		25 MHz
SPI MASTER CLK		25 MHz

Figure 5.7: ZG2100M/ZG2101M

SPI Timing Characteristics

SPI Timing:

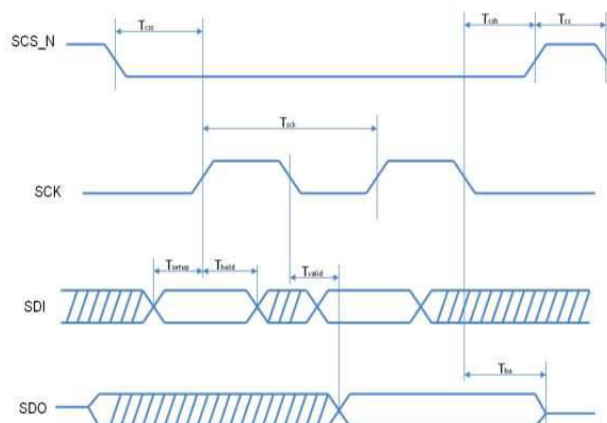


Fig 5.8: ZG2100M/ZG2101M SPI

Timing Waveform

Single VCC = 3.3V (+/-10%)

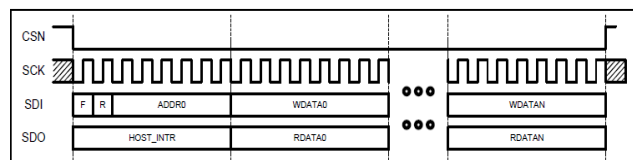


Fig 5.9: ZG2100M/ZG2101M SPI

Register Timing

5.5.3 FIFO INTERFACE:

HOST FIFO Basic Commands

FCMD[2:0]

0x0 – RFIFO_CMD

0x1 – WCONT (Continue Previous Packet)

0x2 – WSTART0 (Start Packet, head/continue)

0x3 – WSTART1 (Start Packet, head0/continue)

0x4 – WEND CMD

0x5 – REND CMD

FIFO Read:

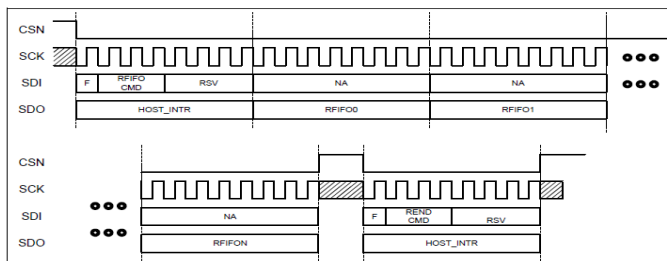


Fig .5.10:ZG2100M/ZG2101M

FIFO Read Timing FIFO Write:

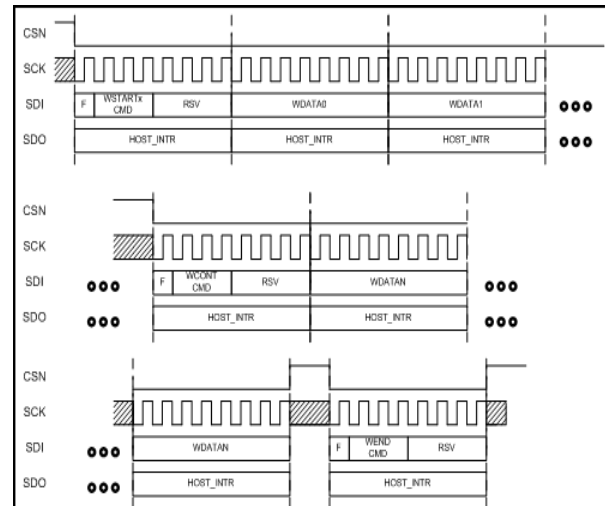


Fig 5.11:ZG2100M/ZG2101M

FIFO Write Timing

5.5.4 PACKAGE INFORMATION:

Module Drawing:

The antenna will need a reasonable ground plane area on the mother board area to be efficient. Do not use a metallic or metalized plastic for the enclosure. Plastic enclosure keep away dimension, from the antenna in any orientation, will be provided after module antenna characterizations. To maintain the efficiency and impedance for ZG2100M PCB antenna, designer should keep conductors and dielectrics, which are more than 0.5 mm thick, 15 mm from the antenna in all directions.

Module Use Schematic

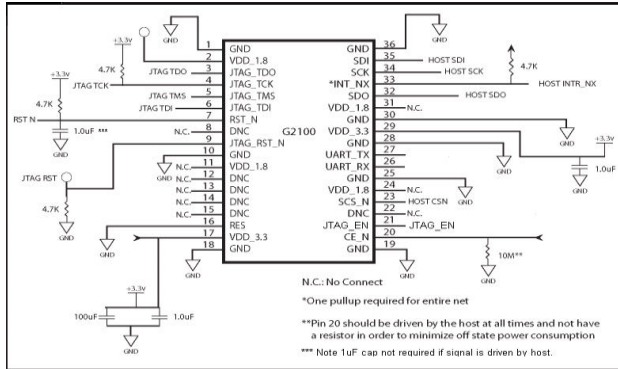


Fig 5.12:ZG2100M/ZG2101M Module Use Schematic

Power Consumption:

Nominal conditions: 25C, 3.3V supply applied to VDD33, commercial parts

Power Conservation Modes	Min	Typ	Max	Unit
Hibernate, CE_N=3.3v		0.1	5.6	uA
Sleep		250		uA
Standby (transitional power state)		10		uA
Core Supply	Min	Typ	Max	Unit
Rx On, Receive I _{rx} , -83dBm		85		mA
Tx On, Transmit I _{tx} , +0dBm		165		mA
Tx On, Transmit I _{tx} , +10dBm		230		mA

Fig 5.13:power consumption

Receiver 2.4GHz Band

RX Min Input Level Sensitivity, 2Mbps, 8% PER	-88		dBm
RX Max Input Level (Power), 1Mbps, 8% PER	-4		dBm
RX Max Input Level (Power), 2Mbps, 8% PER	-4		dBm

Fig 5.14:Digital Electrical Characteristics

Single VCC =3.3V (+/-10%)

Characteristic	Min	Typ	Max	Unit
V _{IL} (Input Low Voltage)	-0.3		0.8	V
V _{IH} (Input High Voltage)	2		V _{CC} *1.1	V
V _{OL} (Output Low Voltage)			0.4	V
V _{OH} (Output High Voltage)	2.4			V
I _{OL} (Low Level Output Current @ V _{OL} Max)		8.5		mA
I _{OH} (High Level Output Current @ V _{OH} Min)		15.4		mA

Fig 5.15:Module Reflow Profile

5.6 UART: The LPC2141/42/44/46/48 each contains two UARTs. Compared to previous LPC2000 microcontrollers, UARTs in LPC2141/42/44/46/48 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rate such as 115200 with any crystal frequency above 2 MHz In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware (UART1 in LPC2144/46/48 only).

Features:

- 16 byte Receive and Transmit FIFO.

- Register locations conform to '550 industry standard.
- Receiver FIFO triggers points at 1, 4, 8, and 14 bytes
- Transmission FIFO control enables implementation of software (XON/XOFF) Flow control on both UARTs.

I2C-bus serial I/O controller:

The LPC2141/42/44/46/48 each contains two I2C-bus controllers. The I2C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)).

Features:

- Compliant with standard I2C-bus interface.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).

SSP serial I/O controller:

The LPC2141/42/44/46/48 each contains one SSP. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Micro wire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master.

Features:

- Synchronous serial communication.
- Master or slave operation.

General purpose timers/external event counters:

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers

5.6.1 WATCHDOG TIMER:

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will

generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

Features:

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Programmable 32-bit timer with internal pre-scalar.

5.6.2 REAL-TIME CLOCK:

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously

6. Conclusion

In industry it is very difficult to major all the physical quantities manually. And sometimes it is not sure accurate even if we measure all the physical quantities manually. Also they are certain physical quantities such as temperature are it very high temperatures. Which needs to be measure without human interface. So a real -time wireless based wireless data acquisition

system developed for monitoring all these physical quantities. By using this project humidity, temperature, fire, smoke sensors can be monitored for remotely by using ARM7 controller.

FUTURE ENHANCEMENT:

1. We can monitor some hazardous parameters like overheat, LPG gas leakage.
2. We can provide voice announcement or voice feedback system to indicate the current state or the current operation of the circuit.

REFERENCES:

- [1] G. Varaprasad and R. S. D. Wahidabanu, "Flexible routing algorithm for vehicular area networks," in Proc. IEEE Conf. Intell. Transp. Syst. Telecommun., Osaka, Japan, 2010, pp. 30–38.
- [2] B. P. Gokulan and D. Srinivasan, "Distributed geometric fuzzy multiagent urban traffic signal control," IEEE Trans. Intell. Transp. Syst., vol. 11, no. 3, pp. 714–727, Sep. 2010.



[3] K. Sridharamurthy, A. P. Govinda, J. D. Gopal, and G. Varaprasad, "Violation detection method for vehicular ad hoc networking," *Security Commun. Netw.*, to be published. [Online]. Available:

<http://onlinelibrary.wiley.com/doi/10.1002/sec.427/abstract>

[4] M. Abdoos, N. Mozayani, and A. L. C. Bazzan, "Traffic light control in non-stationary environments based on multi agent Q-learning," in *Proc. 14th Int. IEEE Conf. Intell. Transp. Syst.*, Oct. 2011, pp. 580–1585.

[5] ZigBee Specifications, ZigBee Alliance IEEE Standard 802.15.4k2013, 2014. [Online]. Available: <http://www.zigbee.org/Specifications.aspx>

[6] Traffic Congestion in Bangalore—A Rising Concern. [Online]. Available:

<http://www.commonfloor.com/guide/traffic-congestion-in-bangalore-arising-concern-27238.html>, accessed 2013.

[7] A. K. Mittal and D. Bhandari, "A novel approach to implement green wave system

and detection of stolen vehicles," in *Proc. IEEE 3rd Int. Adv. Comput.*, Feb. 2013, pp. 1055–1059.

[8] S. Sharma, A. Pithora, G. Gupta, M. Goel, and M. Sinha, "Traffic light priority control for emergency vehicle using RFID," *Int. J. Innov. Eng. Technol.*, vol. 2, no. 2, pp. 363–366, 2013.

[9] R. Hegde, R. R. Sali, and M. S. Indira, "RFID and GPS based automatic lane clearance system for ambulance," *Int. J. Adv. Elect. Electron. Eng.*, vol. 2, no. 3, pp. 102–107, 2013.

[10] P. Sood. Bangalore Traffic Police-Preparing for the Future. [Online]. Available: <http://www.intranse.in/its1/sites/default/files/D1-S2->, accessed 2011.

[11] Traffic Management Centre. [Online]. Available:

http://www.bangaloretrafficpolice.gov.in/index.php?option=com_content&view=article&id=87&btp=87, accessed 2014.



[12] G. Varaprasad, “High stable power aware multicast algorithm for mobile ad hoc networks,” IEEE Sensors J., vol. 13, no. 5, pp. 1442–1446, May 2013.

[13] Traffic Solution. [Online]. Available: <http://phys.org/news/2013-05-physics-green-city-traffic-smoothly.html>, accessed 2013.

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