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LOW-POWER PROGRAMMABLE PRPG WITH TEST COMPRESSION CAPABILITIES

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ABSTRACT:

This paper describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date built-in self-test (BIST)- based pseudorandom test pattern generators. It is comprised of a linear finite state machine (a linear feedback shift register or a ring generator) driving an appropriate phase shifter, and it comes with a number of features allowing this device to produce binary sequences with preselected toggling (PRESTO) activity. We introduce a method to automatically select several controls of the generator offering easy and precise tuning. The same technique is subsequently employed to deterministically guide the generator toward test sequences with improved fault-coverage-to pattern- count ratios. Furthermore, this paper proposes an LP test compression method that allows shaping the test power envelope in a fully predictable, accurate, and flexible fashion by adapting the PRESTO-based logic BIST (LBIST) infrastructure. The proposed hybrid scheme efficiently combines test compression with LBIST, where both techniques can work synergistically to deliver high quality tests. Experimental results obtained for industrial designs illustrate the feasibility of the proposed test schemes and are reported herein.

1. INTRODUCTION

Although over the next years, the primary objective of manufacturing test will remain essentially the same— to ensure reliable and high quality semiconductor products— conditions and consequently also test solutions may undergo a significant evolution. The

semiconductor technology, design characteristics, and the design process are among the key factors that will impact this evolution. With new types of defects that one

will have to consider to provide the desired test quality for the next technology nodes such as 3-D, it is appropriate to pose the question of what matching design-for-test (DFT) methods will need to be deployed. Introduced a decade ago, has quickly become the main stream DFT methodology. However, it is unclear whether test compression will be capable of coping with the rapid rate of technological changes over the next decade. Interestingly, logic built-in self-test (LBIST), originally developed for board, system, and in-field test, is now gaining acceptance for production test as it provides very robust DFT and is used increasingly often with test compression. This hybrid approach seems to be the next logical evolutionary step in DFT. It has potential for improved test quality; it may augment the abilities to run at-speed power aware tests, and it can reduce the cost of manufacturing test while preserving all LBIST and scan compression advantages. Attempts to overcome the bottleneck of test data bandwidth between the tester and the chip have made the concept of combining LBIST and test data compression a vital research and development area. In particular, several hybrid BIST schemes store deterministic top-up patterns (used to detect random pattern resistant faults) on the tester in a compressed form, and then use the existing BIST hardware to decompress these test patterns. Some solutions embed deterministic stimuli by using compressed weights or by perturbing pseudorandom vectors in various fashions. If BIST logic is used to deliver compressed test data, then underlying encoding schemes typically take advantage of low fill rates, as originally proposed in LFSR coding which subsequently evolved first into static LFSR reseeding and then into dynamic LFSR reseeding. Thorough surveys of relevant test compression techniques can be found. As with conventional scan-based test, hybrid schemes, due to the high data activity associated with scan-based test operations, may consume much more power than a circuit under- test was designed to function under. With overstressing devices beyond the mission mode, reductions in the operating power of ICs in a test mode have been of concern for years. Full-toggle scan patterns may draw several times the typical Functional mode power and this trend continue to grow, particularly over the mission mode's peak power. This power induced over-test may result in thermal issues, voltage noise, power droop, or excessive peak power over multiple cycles which, in turn, cause a yield loss due to instant device damage, severe decrease in chip reliability, shorter product lifetime, or a device malfunction because of timing failures

following a significant circuit delay increase, for example. Abnormal switching activity may also cause fully functional chips to fail during testing because of phenomena, such as IR-drop, crosstalk, or di/dt problem. Numerous schemes for power reduction during scan. Among them, there are solutions specifically proposed for BIST to keep the average and peak power below a given threshold. For example, the test power

can be reduced by preventing transitions at memory elements from propagating to combinational logic during scan shift. This is achieved by inserting gating logic between scan cell outputs and logic they drive. During normal operations and capture, this logic remains transparent. Gated scan cells are also proposed. A synergistic test power reduction method of uses available on-chip clock gating circuitry to selectively block scan chains while employing test scheduling and planning to further decrease BIST power in the Cell processor. A test vector inhibiting scheme of asks test patterns generated by an LFSR as not all produced vectors, often very lengthy, detect faults. Elimination of such tests can reduce switching activity with no impact on fault coverage. The advent of low-transition test pattern generators has added a new dimension to power aware BIST solutions. For example, a device presented employs an LFSR to feed scan chains through biasing logic and T-type flip-flop. Since this flip-flop holds the previous value until its input is asserted, the same value is repeatedly scanned into scan chains until the value at the output of biasing logic (e.g., a k-input AND gate) becomes 1. Depending on k, one can significantly reduce the number of transitions occurring at the scan chain inputs. A dual-speed LFSR of consists of two LFSRs driven by normal and slow clocks, respectively. The switching activity is reduced at the circuit inputs connected to the slow-speed LFSR, while the whole scheme still ensures satisfactory fault coverage. Mask patterns mitigate the switching activity in LFSR-produced patterns as, whereas a bit swapping of achieves the same goal at the primary inputs of CUT. A gated LFSR clock allows activating only half of LFSR stages at a time. It cuts power consumption as only half of the circuit inputs change every cycle. Combining the low transition generator of (handling easy-to-detect faults) with a 3-weight pseudorandom test pattern generator (PRPG) (detecting random pattern resistant faults) can also reduce BIST switching activity, as demonstrated . The schemes of suppress transitions in LFSR-generated sequences by either statistical monitoring or injecting intermediate and highly

correlated patterns. Finally, a random single-input change generator can produce low power patterns in a parallel BIST environment. As the BIST power consumption can easily exceed the maximum ratings when testing at speed, scan patterns must be shifted at a programmable low speed, and only the last few cycles and the capture cycle are applied at the maximum frequency. In the burst-mode approach presented, typically five consecutive clock cycles are used. The first four cycles serve shifting purposes, whereas the last one is designated for capture. The objective is to stabilize the power supply before the last shift and capture pulses are applied, which are critical for at-speed tests. To reduce the voltage droop related to a higher circuit activity, a burst clock controller slows down some of the shift cycles. It allows a gradual increase of the circuit activity, thereby reducing the di/dt effect. The controller can gate the shift clocks, depending on the needs for gradually warming up of the circuit. Low power (LP) test compression schemes adapt again LFSR reseeding to reduce scan-in transitions as the low fill rates make it possible to deliver identical test data to scan chains for a number of shift cycles directly from the decompressor, thereby reducing the number of transitions. In this paper, we propose a PRPG for LP BIST applications. The generator primarily aims at reducing the switching activity during scan loading due to its preselected toggling (PRESTO) levels. It can assume a variety of configurations that allow a given scan chain to be driven either by a PRPG itself or by a constant value fixed for a given period of time. Not only the PRESTO generator allows loading scan chains with patterns having low transition counts, and thus significantly reduced power dissipation, but it also enables fully automated selection of its controls such that the resultant test patterns feature desired, user-defined toggling rates. We will demonstrate that this flexible programming can be further used to produce tests superior to conventional pseudorandom vectors with respect to a resultant fault-coverage-to-test-pattern-count ratio. This paper culminates in showing that the PRESTO generator can also successfully act as a test data decompressor, thus allowing one to implement a hybrid test methodology that combines LBIST and ATPG-based embedded test compression. This is the first LP test compression scheme that is integrated in every way with the BIST environment and lets designers shape the power envelope in a fully predictable, accurate, and flexible fashion. As a result, it creates an environment that can be used to arrive at an efficient hybrid solution

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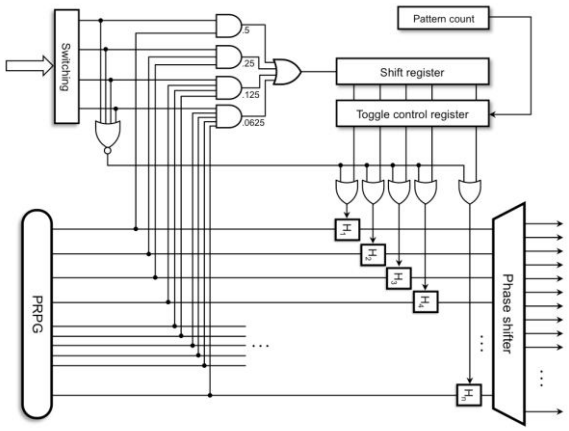
combining advantages of scan compression and logic BIST. In addition, both techniques can complement each other to address, for example, a voltage drop caused by a high switching activity during scan testing, constraints of at-speed ATPG-produced test patterns, or new fault models.



2 BASIC ARCHITECTURE

the basic structure of a PRESTO generator. An n-bit PRPG connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test patterns. A linear feedback shift register or a ring generator can implement a PRPG. More importantly, however, n hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an n-bit toggle control register. As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is said to be in the toggle mode. When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of PRPG, thus feeding the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode. It is worth noting that each phase shifter output is obtained by XOR-ing outputs of three different hold latches. Therefore, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output. As mentioned previously, the toggle control register supervises the hold latches. Its content comprises 0s and 1s, where 1s indicate latches in the toggle mode, thus transparent for data arriving from the PRPG. Their fraction determines a scan switching activity. The control register is reloaded once per pattern with the content of an additional shift register. The enable signals injected into the shift register are produced in a probabilistic fashion by using the original PRPG with a programmable set of weights. The weights are determined by four AND gates producing 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate allows choosing probabilities beyond simple powers of 2. A 4-bit register Switching is employed to activate AND gates, and allows selecting a user-defined level of switching activity. For

example, the switching code 0100 will set to 1, on the average, 25% of the control register stages, and thus 25% of hold latches will be enabled. Given the phase shifter structure, one can assess then the amount of scan chains receiving constant values, and thus the expected toggling ratio. An additional 4-input NOR gate detects the switching code 0000, which is used to switch the LP functionality off. It is worth noting that when working in the weighted random mode, the switching level selector ensures statistically stable content of the control register in terms of the amount of 1s it carries. As a result, roughly the same fraction of scan chains will stay in the LP mode, though a set of actual low toggling chains will keep changing from one test pattern to another. It will correspond to a certain level of toggling in the scan chains. With only 15 different switching codes, however, the available toggling granularity may render this solution too coarse to be always acceptable.

3.FULLYOPERATIONALGENERATOR

Much higher flexibility in forming low-toggling test patterns can be achieved by deploying a scheme presented. Essentially, while preserving the operational principles of the basic solution, this approach splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals. To move the generator back and forth between these two states, we use a T-type flip-flop that switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content. This is accomplished by placing AND gates on the control register outputs to allow freezing of All phase shifter inputs. This property can be crucial in SoC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods. If the T flip-flop is set to 1 (the toggle period), then the latches enabled through the control register can pass test data moving from the PRPG to the scan chains. Two additional parameters kept in 4-bit Hold and Toggle registers determine how long the entire generator remains either in the hold mode or in the toggle mode, respectively. To terminate either mode, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced in a manner similar to that of weighted logic used to feed the shift register. The T flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows selecting a

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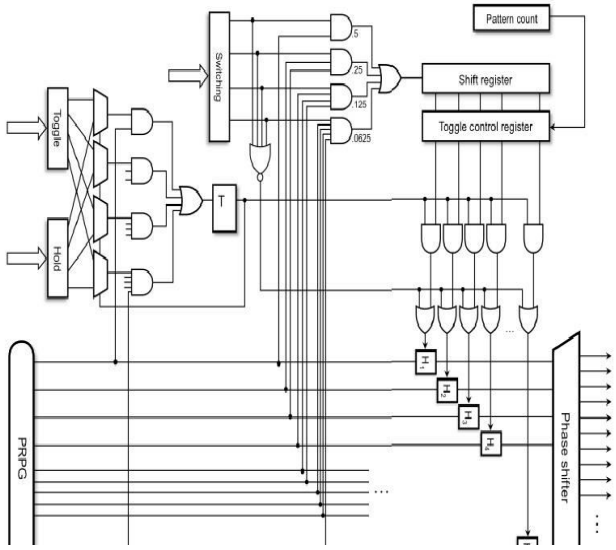
source of control data that will be used in the next cycle to possibly change the operational mode of the generator. For example, when in the toggle mode, the input multiplexers observe the Toggle register. Once the weighted logic outputs 1, the flip-flop toggles, and as a result all hold latches freeze in the last recorded state. They will remain in this state until another 1 occurs on the weighted logic output. The random occurrence of this event is now related to the content of the Hold register, which determines when to terminate the hold mode. A scan switching profile when deploying the PRESTO generator in a hypothetical environment with 15 scans chains



4.AUTOMATIC SELECTIONS OF CONTROLS

performance of the PRESTO generator depends primarily on the following three factors (note that in the BIST mode they are delivered only once, at the very beginning of the entire test session): 1) the switching code (kept in the switching register); 2) the hold duty cycle (HC); 3) the toggle duty cycle (TC). Given the size of PRPG, the number of scan chains and the corresponding phase shifter, the switching code as well as HC and TC values can be selected automatically in such a way that the entire generator will produce pseudorandom test patterns having a desired level of toggling T provided the scan chains are balanced.

1) For each switching code k, $k = 1, \ldots, 15$, determine the corresponding probability pk of injecting a 1 into the shift register. These values are as follows: $p1 = 0.5$, $p2 = 0.25$, $p3 = 0.625$, $p4 = 0.125$, $p5 = 0.5625$, $p6 = 0.34375$, $p7 = 0.671875$, $p8 = 0.0625$, $p9 = 0.53125$, $p10 = 0.296875$, $p11 = 0.6484375$, $p12 = 0.1796875$, $p13 = 0.58984375$, $p14 = 0.38476563$, and $p15 = 0.69238281$.

2) As can be seen in Fig. 2, the values pk btained in step 1 determine as well the probability of asserting the T flipflop input for each hold (toggle) code k, and then the corresponding duration hk (tk) of the hold (toggle) duty cycle. Clearly, $hk = tk = 1/pk$. 3) Given the size n of PRPG, determine, for each switching code k, the average number nk of 1s occurring in the control register. As can be easily verified, $nk = pk \times n$. 4) For each value of

nk (the number of enabled hold latches), find the average number *ak* of active scan chains, i.e., scan chains that are not in the LP mode. This number is determined by the phase shifter architecture, and it also depends on the actual locations of 1s in the control register. Therefore, 1000 *n*-bit random combinations having exactly *nk* 1s are generated to obtain the number of active scan chains in each case, and finally the number *ak* of active scan chains is averaged over all 1000 samples.

5) Given a desired level of toggling *T* (%), one can determine the resultant (hypothetical) number *A* of active scan chains from the following equation:

$A = (T \times S)/50$ (1)

where *S* is the total number of scan chains. The above proportion assumes that if all *S* scan chains are active, then the resultant toggling is about 50%. 6) For each switching code *k*, and thus the resulting number *ak* of active scan chains, determine how many additional scan chains should be disabled. In each case, this quantity is given by $dk = ak - A$. If $dk \leq 0$, thn disregard the next steps, as the switching code *k* does not guarantee even the smallest (required) number of active scan chains.

7) Since disabling extra scan chains cannot be implemented through the control register, this action is carried out by equivalent disabling—with help of HCs—of selected cells belonging to active scan chains. The value of *dk* is therefore converted into the number of corresponding cells in active scan chains . Let *L* be the scan chain length.

5 VALIDATING EXPERIMENTS

The approach presented in Section IV has been validated by experiments run on five different scan architectures (203× 300, 122 × 104, 84 × 416, 128 × 353, 160 × 541) used

in five industrial designs, and with a 33-bit ring generator implementing a primitive polynomial $x33+x25+x16+x8+1$ and feeding 33-input phase shifter for 10 000 pseudorandom test patterns. The average toggling rates measured by means of the WTM are plotted against successive values of a desired switching activity (the requested toggling). The standard deviation is used to assess a possible dispersion from the average toggling values. Clearly, the lower the values of the standard deviation, the smaller the spread of toggling activity with respect to the desired level of switching activity. The plot consists of four different curves. The central red line represents the average value of the toggling ratio computed

over all examined designs and all test patterns for successive values of the desired (user-

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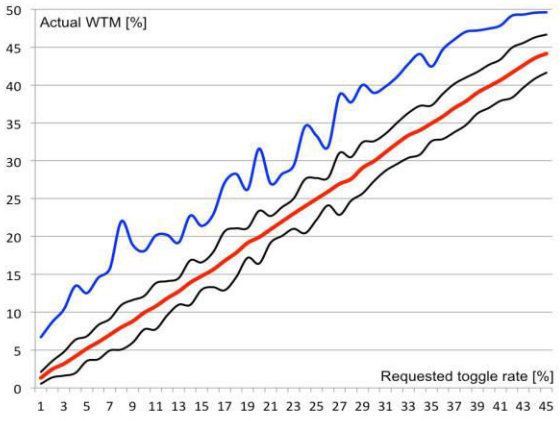
selected) toggling rate varying from 1% to 45% in steps of 1%. Two black lines correspond to



s tandard deviation bounding the average value curve from the top and the bottom. The last (blue) curve represents maximal values (averaged over maximal values obtained for all examined designs) recorded for each toggling rate. As can be seen, the resultant switching activity follows closely, with small values of standard deviation, the requested rates. Gathers experimental results similar to those of but obtained in a slightly different way. Before plotting the actual values of toggling rates and the remaining statistics, experiments for every single toggling rate were performed for 32- and 33-bit PRPGs (the 32-bit ring generator uses a primitive polynomial $x32 + x25 + x15 + x7 + 1$). Note that phase shifters are separately synthesized in each case. The resultant toggling rates were compared, and switching activity with a smaller absolute dispersion from the expected value was chosen as the final result. It appears that in certain cases it is preferable to pick a 32-bit PRPG rather than a 33-bit one, or *vice versa*. This strategy yields virtually a straight line with respect to toggling rates, hence offering an accurate mapping between the user-selected values of switching activity and the actual circuit response. One can also observe reduced maximal values and smaller standard deviations in this case

.

6 IMPROVING FAULT COVERAGE GRADIENT

A quest to achieve higher BIST fault coverage with shorter test application time generated an immense amount of research in the past. Typically, LFSR-based pseudorandom test sequences were modified either by placing a mapping logic between the PRPG outputs and inputs of a circuit under test or by adjusting the probabilities of outputting 0s and 1s so that the resultant vectors capture characteristics of test patterns for hard-to-detect faults, as done in various forms of weighted-random testing Test patterns leaving a PRPG can also be transformed in a more deterministic fashion. Along the same lines, we will demonstrate that PRESTO-produced LP test patterns are also capable of visibly improving a faultcoverage-to-pattern-count ratio. Assuming that the toggle

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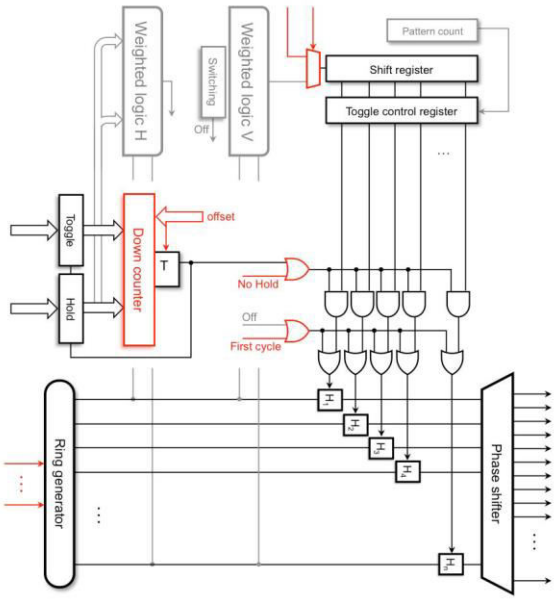
control register can also be driven by deterministic test data (see location of an additional multiplexer in the front of a shift registe, test patterns can be produced with better-than-average fault coverage. The proposed method begins by computing the PRESTO parameters,



as described. Subsequently, ATPG is repeatedly invoked until either a desired PRESTO pattern count or a fault coverage limit is reached. The ATPG produces test cubes in one per fault fashion. The number of generated test cubes is limited (in each iteration) for performance reasons. As confirmed by many experiments, the properly selected limithas a negligible impact on test quality. The obtained test cubes are now deployed to arrive with the content of the control register, as described in the following. Given the PRESTO switching code, our goal is now to find the corresponding distribution of 1s in the control register that maximizes the fault detection probability. The procedure starts by reducing each ATPG-produced test cube to a set of scan chains containing more than one specified bit. This set will be further referred to as a base. For example, let a test cube feature the following specified scan cells: {*(s, c)*: *(*4, 13*), (*4, 2*), (*13, 34*), (*13, 31*), (*45, 11*)*}, where *s* is a scan chain, and *c* is a cell location within the scan chain. The base is thus given by {4, 13}; note that chain 45 is not included as it features only one specified scan cell. A good chance (50%) of producing a given logic value in a purely pseudorandom fashion is a rationale behind excluding from any base scan chains hosting a single specified bit. As a result, more bases can be subsequently combined together to produce a single control setting.

7 ENCODING ALGORITHM

The decompressor architecture presented in Section VII is tightly coupled with a compression procedure. It partitions a given test pattern into several blocks corresponding alternately to hold and toggle periods. Recall that in the hold mode, all phase shifter inputs are frozen due to disabled hold latches, whereas

the toggle mode allows certain inputs of the phase shifter to receive data from the ring generator provided the corresponding bits of the toggle control register are asserted. Since this register is updated once per pattern, scan chains driven only by disabled hold latches are loaded with constant values, and thus remain in the LP mode for the entire pattern.

The remaining chains receive either constant values (the HCs) or results of XOR-ing certain outputs of PRPG (during the TCs) among which at least one is enabled.

8.EXPERIMENTAL RESULTS

This section presents experimental results obtained for the PRESTO generator and several industrial designs whose characteristics For each test case, the table provides the number of gates, the number of scan chains, and the size of the longest scan chain. Furthermore, the column TC reports the resultant test coverage after applying 128K pseudorandom test patterns produced by the PRESTO generator with its LP features disabled. The next column (EP) lists the corresponding number of test patterns that effectively contributed to that level of fault coverage. Finally, the last two columns provide the WTM load for scan shift-in operations and the weighted switching activity (WSA) during the capture operation. As can be seen, WTM remains close to 50%, as typically observed in scan vectors produced in a pseudorandom fashion. The primary objective of the experiments was to measure test coverage as a function of several parameters, including:

1) The number of test patterns;
2) The switching activity code;
3) The duration of Toggle (T) period;
4) The duration of Hold (H) period.

9.CONCLUSION

As shown in the paper, PRESTO—the LP generator—can produce pseudorandom test patterns with scan shift-in switching activity precisely selected through automated programming. The same features can be used to control the generator, so that the resultant test vectors can either yield a desired fault coverage faster than the conventional pseudorandom patterns while still reducing toggling rates down to desired levels, or they can offer visibly higher coverage numbers if run for comparable test times. This LP PRPG is also capable of acting as a fully functional test data decompress or with the ability to control scan shift-in switching activity through the process of encoding. The proposed hybrid solution allows

one to efficiently combine test compression with logic BIST, where both techniques can work synergistically to deliver high quality test. It is therefore a very attractive LP test scheme that allows for trading-off test coverage, pattern counts, and toggling rates in a very flexible manner.

10. REFERENCES

[1] A. S. Abu-Issa and S. F. Quigley, "Bit-swapping LFSR for low-power BIST," Electron. Lett., vol. 44, no. 6, pp. 401–402, Mar. 2008.

[2] C. Barnhart et al., "Extending OPMISR beyond 10x scan test efficiency," IEEE Design Test, vol. 19, no. 5, pp. 65–73, Sep./Oct. 2002.

[3] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "Low-power scan design using first-level supply gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 3, pp. 384–395, Mar. 2005.

[4] M. Chatterjee and D. K. Pradham, "A novel pattern generator for nearperfect fault-coverage," in Proc. 13th IEEE Very Large Scale Integr. (VTSI) Test Symp., Apr./May 1995, pp. 417–425.

[5] F. Corno, M. Rebaudengo, M. S. Reorda, G. Squillero, and M. Violante, "Low power BIST via non-linear hybrid cellular automata," in Proc. 18th IEEE Very Large Scale Integr. (VTSI) Test Symp., May 2000, pp. 29–34.

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