



# International Journal for Innovative Engineering and Management Research

A Peer Reviewed Open Access International Journal

www.ijiemr.org

## COPY RIGHT

**2017 IJIEMR.** Personal use of this material is permitted. Permission from IJIEMR must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. No Reprint should be done to this paper, all copy right is authenticated to Paper Authors

IJIEMR Transactions, online available on 24<sup>th</sup> July 2017. Link :

<http://www.ijiemr.org/downloads.php?vol=Volume-6&issue=ISSUE-5>

Title: High Step-Up Dual Switch Converter With Coupled Inductor and Voltage Multiplier For Grid Connected System.

Volume 06, Issue 05, Page No: 2089 – 2099.

Paper Authors

**\*G.RADHAKRISHNA, M.CHANDRA SHEKHAR, MR. JADAPALLI SREEDHAR.**

\* of EEE, Annamacharya Institute of Technology & Sciences.



USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per **UGC Guidelines** We Are Providing A Electronic Bar Code

## HIGH STEP-UP DUAL SWITCH CONVERTER WITH COUPLED INDUCTOR AND VOLTAGE MULTIPLIER FOR GRID CONNECTED SYSTEM

<sup>1</sup>G.RADHAKRISHNA, <sup>2</sup>M.CHANDRA SHEKHAR, <sup>3</sup>MR. JADAPALLI SREEDHAR

<sup>1</sup>PG Scholar, Dept of EEE, Annamacharya Institute of Technology & Sciences, Hyderabad, RR (Dt), Telangana, India.

<sup>2</sup>Assistant Professor, Dept of EEE, Annamacharya Institute of Technology & Sciences, Hyderabad, RR (Dt), Telangana, India.

<sup>3</sup>HOD, Dept of EEE, Annamacharya Institute of Technology & Sciences, Hyderabad, RR (Dt); Telangana, India.

### ABSTRACT:

A novel high step-up converter, which is suitable for a PV cell is proposed in this paper. The proposed converter is composed of the dual switches structure, the coupled inductor, and voltage multiplier cells in order to achieve the high step-up voltage gain. The dual switches structure is beneficial to reduce the voltage stress and current stress of the switch. In addition, two multiplier capacitors are, respectively, charged during the switch-on period and switch-off period, which increases the voltage conversion gain. Meanwhile, the energy stored in the leakage inductor is recycled with the use of clamped capacitors. Thus, two main power switches with low on-resistance and low current stress are available. As the leakage inductor, diode reverse-recovery problem is also alleviated. Therefore, the efficiency is improved. This paper illustrates the operation principle of the proposed converter; discusses the effect of the leakage inductor; analyzes the influence of parasitic parameters on the voltage gain and efficiency, the voltage stresses and current stresses of power devices; and a comparison between the performance of the proposed converter and the previous high step-up converters is performed. In the ordinary voltage step-up situation, the conventional step-up converters, such as the boost converter can satisfy the voltage step-up requirement. However, in the high step-up situation, the conventional converter cannot achieve a high step-up conversion with high efficiency by extreme duty cycle or high turns ratio because of the parasitic parameters or leakage inductance.

**Key Words:** Dual switches, high step-up converter, switched capacitor, three-winding coupled inductor, Photo Voltaic System.

### I. INTRODUCTION

In recent years, the boost dc/dc converters have been widely used to step up the renewable energy sources in various industrial applications such as ESS, UPS, and EV etc. In those applications, boost dc/dc converters generally step up the voltage to the high

voltage output. For that reason, to obtain a high voltage gain, many converter topologies were reported [3]-[6] for this application. Direct

voltage step up using high frequency transformer is a Simple and easily controllable converter providing high gain. Isolated current

fed dc-dc converters [7]-[9] are example of this category. However, these topologies result in high voltage spikes across the switch (due to leakage inductance) and large ripple in primary side transformer current as the turn's ratio in the high frequency transformer increases. Most

of the non-isolated high voltage gain dc-dc power converters employ coupled inductor (to achieve higher voltage gain) [11] in contrast to a high frequency transformer used by the isolated versions. The coupled inductor-based dc-dc converter has advantages over isolated transformer-based dc-dc converter in minimizing current stress, using lower rating components and simple winding structure. Modeling procedure of the coupled inductor is described in [12]. For high power converter applications, interleaved coupled inductor-based boost converters [13]-[15] have also been proposed. Voltage gain of the converter can be increased without increasing the duty cycle of the switch by connecting an intermediate capacitor in series with the inductor [6]. The intermediate energy storage capacitor with coupled inductor charges in parallel and discharges in series with the coupled inductor secondary.

A demerit of coupled inductor-based systems is that they have to deal with higher leakage inductance, which causes voltage spikes across the main switch during turn-OFF time and current spike during turn-ON time, resulting in a reduction of the overall circuit efficiency. The effects of leakage inductance can be eliminated by using an active clamp network shown in [9], which provides an alternate path to recover leakage energy. But active clamp network is not as efficient as a

passive clamp because of conduction losses across the power switch of the active clamp network. Active clamp network consists of a switch with passive components while passive clamp network [4] consists of passive components such as diode, capacitor, and

resistor. The passive clamp circuit is more popular to reduce voltage stress across the converter switch by recycling leakage energy. To overcome such disadvantages of the conventional converters. A closed-loop control system, a sensor monitors the system output and feeds the data to a controller that adjusts the control to maintain the desired system output and hence remain unaffected to the external noise sources. A closed loop control has high reliability, easy implementation and output short circuit and overload protection.

In this paper, we propose coupled inductor boost converter that features low switch voltage stress and high gain. To achieves high voltage through a coupled inductor connected in interleaved manner that charges an intermediate buffer capacitor and a passive clamp network to recover the leakage energy. Coupled inductor leads to the incorporation of "turn's ratio" into the gain expression that leads to high efficiency without increasing the duty ratio. As compared to existing high-gain dc-dc converters, the number of passive components used in the proposed converter is less, which reduces the cost and improves the efficiency. Though the proposed converter is applicable to any low voltage source applications such as solar PV, fuel cell stack, battery, etc. The typical renewable energy system is shown in Fig.1. The system can convert the low voltage from

the fuel cells source and photovoltaic cells source into the high voltage via the high step-up converter, and, then, the renewable energy is transformed into the load and utility through the inverter. Therefore, the high step-up converter is indispensable.

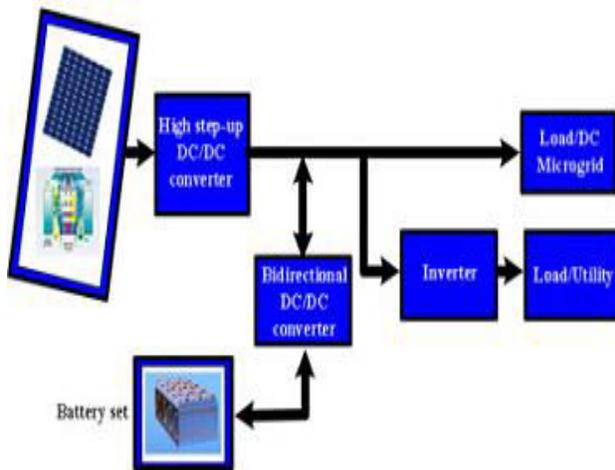


Fig.1. Typical renewable energy system

## II. OPERATION PRINCIPLE OF THE DUAL SWITCHES CONVERTER

Fig.2 shows the circuit topology of the proposed converter. The equivalent circuit model of the three-winding coupled inductor includes the magnetizing inductance  $L_m$ , the leakage inductance  $L_k$ , and an ideal transformer with primary winding  $N_1$  turns and two secondary windings  $N_2$  and  $N_3$  turns. The proposed converter consists of two active switches, five diodes, and five capacitors. The switches  $S_1$  and  $S_2$  share the same operation signal and one control circuit is needed. The leakage inductor energy of the coupled inductor is recycled to the capacitors  $C_1$  and  $C_2$ , and the voltage spikes on the switches are significantly reduced. This makes low conducting resistance  $R_{ds(on)}$  of the switches available. Thus, the efficiency is upgraded and the high step-up

conversion gain can be achieved. Also, the voltages across the capacitors  $C_3$  and  $C_4$  can be adjusted by the turns ratio of the coupled inductor. To simplify the circuit analysis of the proposed converter, the following assumptions are made:

- 1) The Capacitors  $C_1, C_2, C_3, C_4$ , and  $C_o$  is large enough; thus,  $V_{C1}, V_{C2}, V_{C3}, V_{C4}$ , and  $V_o$  are regarded as constant values;
- 2) The power devices are ideal, but the parasitic capacitors of the switches are considered;
- 3) The coupling coefficient of the coupled inductor  $k$  is equal to  $L_m / (L_m + L_k)$ , and the turns ratio of the coupled inductor is  $N_1:N_2:N_3 = 1:1:N$ . The primary winding with  $N_1$  turns, two secondary windings with  $N_2$  and  $N_3$  turns of the ideal transformer with are, respectively, represented by  $L_1, L_2$  and  $L_3 (L_1 : L_2 : L_3 = 1:1:N_2)$ .

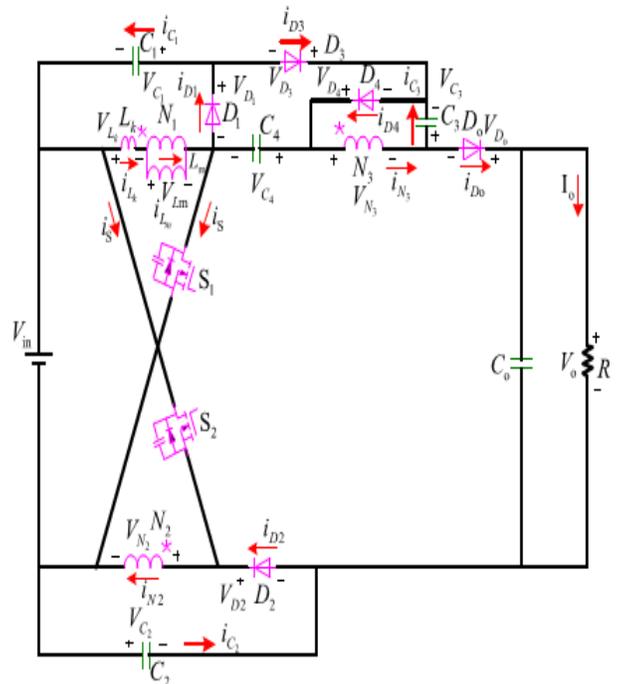


Fig.2. Circuit configuration of the proposed converter

The operating principles for the continuous conduction mode (CCM) are analyzed in detail herein. Fig.3 shows the typical waveforms of the proposed converter during one switching period. Fig.4 shows the topological stages of the proposed converter.

The eight operating modes are described as follows.

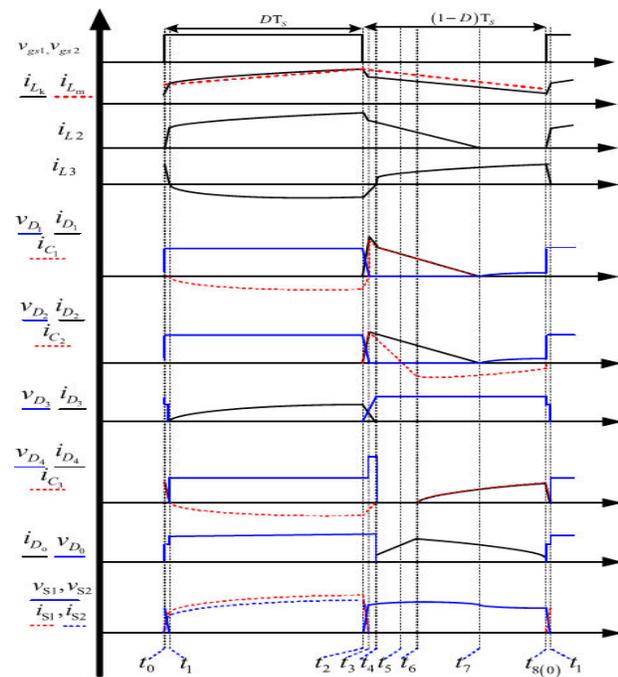


Fig.3. Typical waveforms of the proposed converter during one switching period

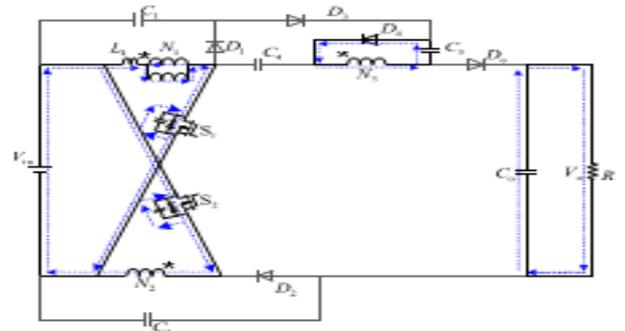
### A. CCM Operation

**Mode I [t<sub>0</sub>, t<sub>1</sub>]:** In this transition interval, the switches S<sub>1</sub> and S<sub>2</sub> start to conduct. Diodes D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>, and D<sub>o</sub> are reverse biased. Diode D<sub>4</sub> is forward biased. The current flow path is shown in Fig.4 (a). The leakage inductance L<sub>k</sub> and magnetizing inductance L<sub>m</sub> are charged by the input source V<sub>in</sub>. The inductor L<sub>2</sub> is also charged by the input source. The leakage inductor current i<sub>Lk</sub> increases linearly. Due to the leakage inductance, the

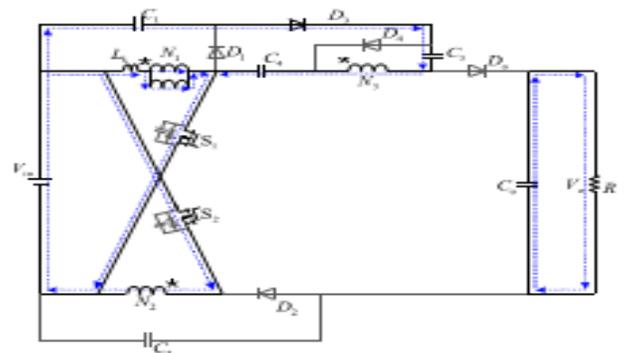
inductor current i<sub>L3</sub> and diode current i<sub>D4</sub> decrease slowly.

Therefore, the voltage of diode D<sub>3</sub> is clamped by input source V<sub>in</sub>, clamped voltages V<sub>C1</sub> and V<sub>C4</sub>; the voltage of diode D<sub>o</sub> is clamped by blocking voltages V<sub>C3</sub>, V<sub>C4</sub>, and V<sub>C2</sub>. The voltage steps are formed. The output capacitor

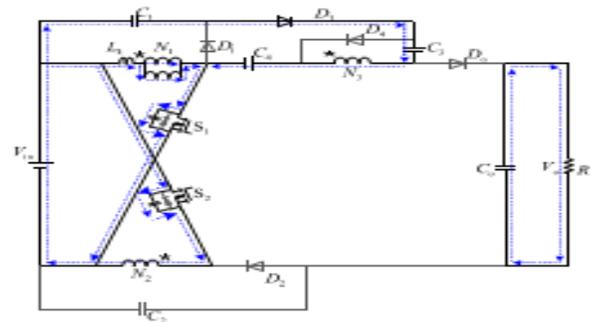
C<sub>o</sub> provides the energy to load R. When the current i<sub>D4</sub> becomes zero (i.e., i<sub>Lk</sub> = i<sub>Lm</sub>), this operating mode ends.



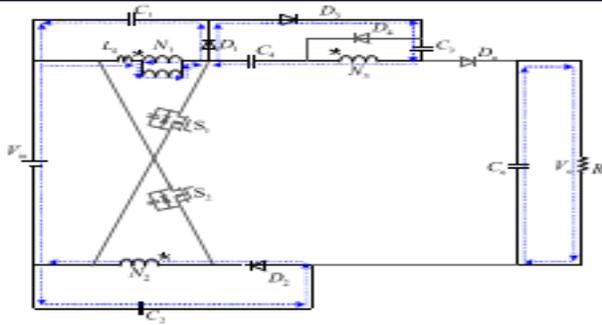
(a)



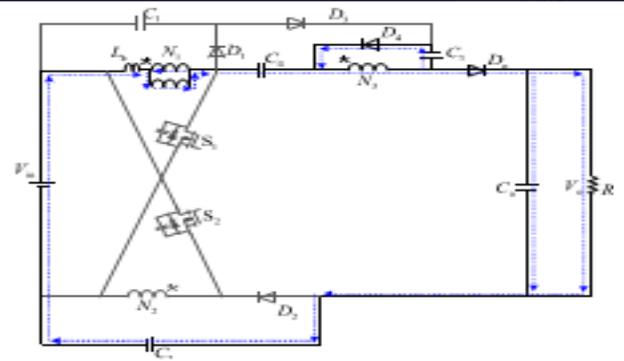
(b)



(c)

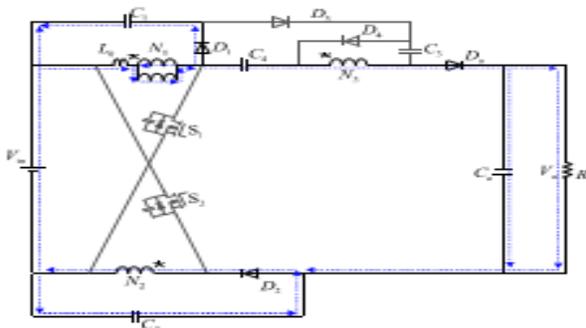


(d)



(h)

Fig.4. Equivalent circuit of the proposed converter



reverse biased. Fig.4 (d) shows the current-flow path. The energies of the leakage inductance  $L_k$  and magnetizing inductance  $L_m$  are released to the clamped capacitor  $C_1$  and energy of the inductor  $L_2$  is transferred to the clamped capacitor  $C_2$ . The blocking capacitor  $C_4$  keeps charging. In addition, due to the leakage inductance, and the diode current  $i_{D3}$  keeps flowing through diode  $D_1$ ; therefore, the voltage across the diode  $D_4$  is clamped by the blocking voltage  $V_{C4}$ . The output capacitor  $C_o$  provides

the energy to load  $R$ . When the currents  $i_{D3}$ ,  $i_{C3}$ , and  $i_{L3}$  decrease to zero at  $t = t_4$ , this operating mode ends.

**Mode V [ $t_4, t_5$ ]:** In this transition interval, the switches are turned off. Diodes  $D_1$ ,  $D_2$ , and  $D_o$  are forward biased. Diodes  $D_3$  and  $D_4$  are reverse biased. The current-flow path is shown in Fig.4 (e). The energies of the leakage inductance  $L_k$  and the magnetizing inductance  $L_m$  are released to the clamped capacitor  $C_1$  and the energy of inductor  $L_2$  is transferred to the clamped capacitor  $C_2$ . The diode current  $i_{D_o}$  increases almost at a constant slope. The input source  $V_{in}$ , three-winding coupled inductor, and the blocking voltage  $V_{C4}$  are connected in series to charge the output capacitor  $C_o$  and provide energy to the load  $R$ . When the diode current  $i_{D_o}$  is equal to diode current  $i_{D2}$  (i.e., capacitor current decreases to zero) at  $t = t_5$ , this operating mode is finished.

**Mode VI [ $t_5, t_6$ ]:** In this transition interval, the switches are turned off. Diodes  $D_1$ ,  $D_2$ , and  $D_o$  are forward biased. Diodes  $D_3$  and  $D_4$  are reverse biased. The current-flow path is shown in Fig.4 (f). The operating mode is almost the same as Mode V except that the capacitor  $C_2$  is discharged instead of charged.

When the diode  $D_4$  is forward biased at  $t = t_6$ , this operating mode ends.

**Mode VII [ $t_6, t_7$ ]:** In this transition interval, the switches are turned off. Diodes  $D_1$ ,  $D_2$ ,  $D_3$ , and  $D_o$  are forward biased. Diode  $D_4$  is reverse biased. The current-flow path is shown in Fig.4 (g). The energies of the leakage inductance  $L_k$  and the magnetizing inductance  $L_m$  are released to the clamped capacitor  $C_1$ . The inductor  $L_2$  and the capacitor  $C_2$  are connected in parallel to discharge the energies to the load and the output capacitor  $C_o$ .

Meanwhile, the input source  $V_{in}$ , inductors  $L_1$  and  $L_2$ , as well as the blocking voltage  $V_{C4}$  provide energy to the output capacitor  $C_o$  and the load  $R$ . The output diode current  $i_{D_o}$  drops almost at a constant slope. In addition, the part energy of the inductor  $L_2$  is transferred to the capacitor  $C_3$ . When the diode currents  $i_{D1}$  and  $i_{D2}$  are equal to zero at  $t = t_7$ , this operating mode ends.

**Mode VIII [ $t_7, t_8$ ]:** In this transition interval, the switches are turned off. Diodes  $D_3$  and  $D_o$  are forward biased. Diodes  $D_1$ ,  $D_2$ , and  $D_4$  are reverse biased. The current-flow path is shown in Fig.4 (h). The leakage inductance  $L_k$ , the magnetizing inductance  $L_m$ , the input source  $V_{in}$ , the inductor  $L_3$ , the blocking voltage  $V_{C4}$ , and the clamped capacitor voltage  $V_{C2}$  are connected in series to provide energy to the output capacitor  $C_o$  and the load  $R$ . Meanwhile, capacitor  $C_3$  keeps charging.

The voltages across the diodes  $D_1$  and  $D_2$  are clamped by the windings of the coupled inductor and the clamped capacitors  $C_1$  and  $C_2$ . Therefore, the voltage steps of diodes  $D_1$  and  $D_2$  are formed, and the voltage drops of the switches are obtained. The output diode current  $i_{D_o}$  drops linearly. When the output diode  $D_o$  is

reverse biased at  $t=t_8$ , this operating mode ends. When the switches are turned on, the new switching period begins.

### III. PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

#### A. Voltage Gain Expression

When the proposed converter operates in the switching-on state, the following equations can be found in Fig.4 (b):

$$V_{L_m} = kV_{in} \quad (1)$$

$$V_{L_k} = (1 - k) V_{in} \quad (2)$$

At modes V–VII, the energies of the leakage inductors are released to the capacitors C1 and C2. According to Tang et al, the duty cycle of the released energy can be approximately obtained

$$D_c = 2(1 - D) / (N + 1) \quad (3)$$

By using the volt-second balance principle on the leakage inductance  $L_k$  and magnetizing inductor  $L_m$ , the voltages of  $L_k$  and  $L_m$  are found as

$$V_{L_m} = DkV_{in} / (1 - D) \quad (4)$$

$$V_{L_k} = D(1 - k)(N + 1)V_{in} / (2(1 - D)) \quad (5)$$

$$V_{N_3} = NDkV_{in} / (1 - D) \quad (6)$$

The voltages of capacitors  $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_4$  can be expressed as

$$V_{C_3} = NDkV_{in} / (1 - D) \quad (7)$$

$$V_{C_1} = V_{C_2} = V_{L_k} + V_{L_m} = \frac{V_{in}D((1+k)+N(1-k))}{2(1-D)} \quad (8)$$

$$V_{C_4} = V_{in} + V_{C_1} + V_{C_3} + V_{N_3}$$

$$= \frac{2 + Dk + DN - DNk - D + 2Nk}{2(1 - D)} V_{in} \quad (9)$$

According to (7)–(9), collecting the terms, the voltage gain can be expressed as

$$G_k = \frac{V_o}{V_{in}} = \frac{V_{C_1} + V_{C_2} + V_{C_3} + V_{C_4} + V_{in}}{V_{in}} = \frac{2 + Nk}{1 - D} + \frac{D(N(1.5 - 0.5k) + (1.5k - 0.5))}{1 - D} \quad (10)$$

$$G = \frac{V_o}{V_{in}} = \frac{2 + N}{1 - D} + \frac{D(N + 1)}{1 - D} \quad (11)$$

$$V_{S1} = V_{S2} = V_{D1} = V_{D2} = \frac{V_{in}}{1 - D} = \frac{V_o}{2 + N + (N + 1)D} \quad (12)$$

$$V_{D4} = \frac{NV_{in}}{1 - D} = NV_o / (2 + N + (N + 1)D) \quad (13)$$

$$V_{D3} = V_{D0} = \frac{(N + 1)V_{in}}{1 - D} = \frac{(N + 1)V_o}{2 + N + (N + 1)D} \quad (14)$$

$$I_{D0}(t_2, t_8) = I_o / (1 - D) \quad (15)$$

$$I_{D1}(t_2, t_7) = I_{D2}(t_2, t_7) = I_o / D_c \quad (16)$$

Then, based on the capacitor charge balance, during the time interval  $[t_0, t_2]$ , the average current of capacitor  $C_1$  can be written as

$$I_{C1}[t_0, t_2] = I_o / D \quad (17)$$

Therefore, the currents of secondary-side  $N_3$  of the coupled inductor can be obtained

$$I_{N3}[t_0, t_2] = I_o / D \quad (18)$$

$$I_{N3}[t_2, t_8] = I_o / (1 - D) \quad (19)$$

During the time interval  $[t_2, t_8]$ , while using KCL, at junction points of the primary side  $N_1$  of the coupled inductor, diode  $D_1$  and capacitor  $C_4$ , the average current of the leakage inductor can be expressed

$$I_{L_k}[t_2, t_8] = (N+3) I_o / (2(1-D)) \quad (20)$$

$$N_1 I_{N1}[t_0, t_2] + N_2 I_{N2}[t_0, t_2] - N_3 I_{N3}[t_0, t_2] = N_1 I_{N1}[t_2, t_8] + N_2 I_{N2}[t_2, t_7] + N_3 I_{N3}[t_2, t_8] \quad (21)$$

$$I_{N1}[t_0, t_2] = I_o (2D + N + DN) / (2D(1-D)) \quad (22)$$

Then, the RMS values of the switches  $S_1$  and  $S_2$  are

$$I_{RMS-S_1} = \sqrt{\frac{1}{T_S} \int_0^{DT_S} \left( I_{N1}[t_0, t_2] + \frac{I_o}{D} - 0.5\Delta I_L + \frac{\Delta I_L}{DT_S} t \right)^2 dt}$$

$$dt = \sqrt{\frac{(2D + N + DN)^2}{4D(1-D)^2} I_o \left( \frac{K^2}{12} + 1 \right) + I_o \frac{2D + N + DN}{D(1-D)} + \frac{I_o^2}{D}}$$

$$I_{RMS-S_2} = \sqrt{\frac{1}{T_S} \int_0^{DT_S} \left( I_{[t_0, t_2]} - 0.5\Delta I_L + \frac{\Delta I_L}{DT_S} t \right)^2 dt}$$

$$dt = \frac{2D + N + DN}{2D(1-D)} I_o \sqrt{D} \sqrt{\frac{K^2}{12} + 1} \quad (23)$$

$$M = \frac{\frac{2+N+D(N+1)}{1-D} - \frac{5V_D}{V_{in}}}{1 + R_L A + R_{DS} B + \frac{(4R_D + (4N+6)R_L)}{R(1-D)} + \frac{R_D + NR_L}{RD}} \quad (24)$$

Where

$$A = (N + ND + 3D)(N + ND + 2D) / (RD(1-D)^2)$$

$$B = (N + ND + D + 1)(N + ND + 2D + 1) / (RD(1-D))$$

$$\eta = \frac{2 + N + D(N+1) - \frac{5V_D}{V_{in}}(1-D)}{\left( 1 + R_L A + R_{DS} B + \frac{(4R_D + (4N+6)R_L)}{R(1-D)} + \frac{R_D + NR_L}{RD} \right) (2 + N + D(N+1))} \quad (25)$$

## IV. MATLAB/SIMULINK RESULTS

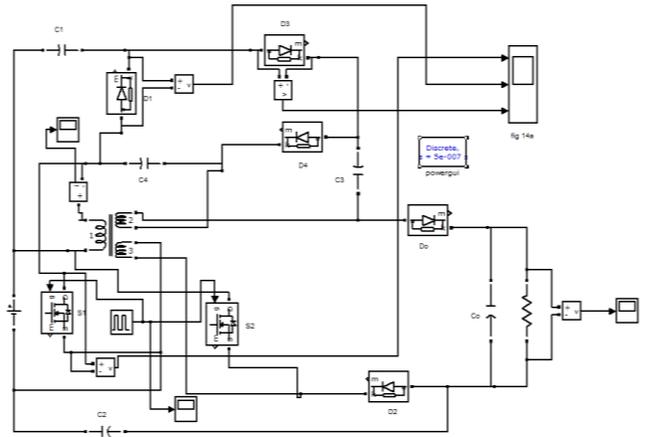


Fig.5 shows the matlab/Simulink model of proposed system

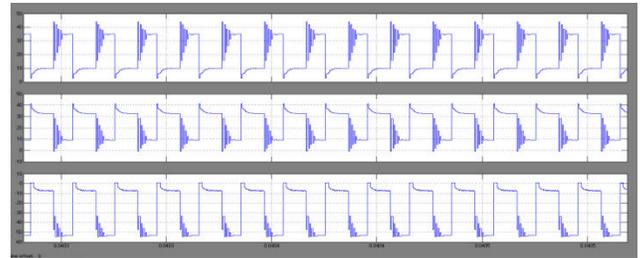


Fig.6 shows the simulation waveforms of proposed system like diode voltages and switch voltages.

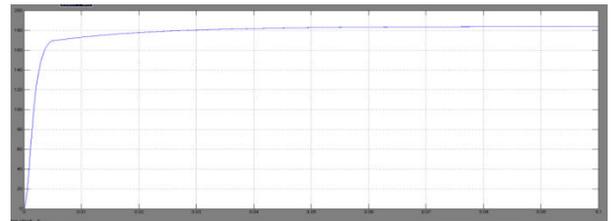


Fig.7 shows the output voltage of proposed converter

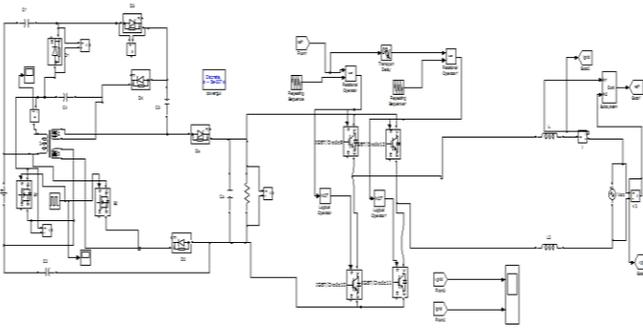


Fig.8 shows the proposed converter with grid connected system

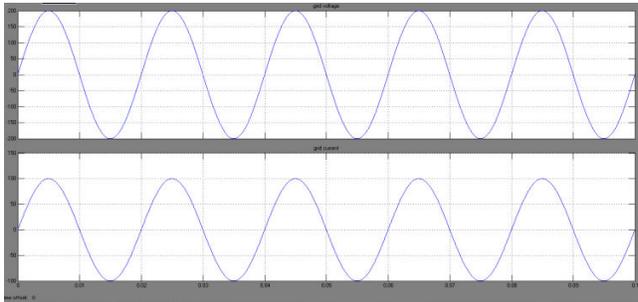


Fig.9 shows the grid outputs of grid voltage and grid current

## V. CONCLUSION

The paper introduces closed loop control of high step up dual switch converter with coupled inductor and voltage multiplier cell for secondary grid connected applications. An additional control freedom is provided by the voltage multiplier cell to achieve extremely high voltage conversion ratio and to minimize the current ripple. The energy stored in the leakage inductance of the coupled inductor is recycled by using switched capacitors. The voltage stress across the main switch is reduced. Here the gate signals are generated using PWM control schemes. The proposed converter operated under open-loop & closed loop manner. The proposed converter has successfully implemented an efficient high

step-up conversion through the voltage multiplier module. The interleaved structure reduces the input current ripple and distributes the current through each component. In addition, the lossless passive clamp function recycles the leakage energy and constrains a large voltage spike across the power switch. Meanwhile, the voltage stress on the power switch is restricted and much lower than the output voltage.

## REFERENCES

- [1]. Moumita Das and Vivek Agarwal, Student Member, IEEE, "Design and Analysis of a High efficiency DC-DC Converter with Soft Switching Capability for Renewable energy Applications Requiring High Voltage Gain" IEEE Trans. Ind. Electron., vol .63, NO. 5, May 2016.
- [2]. W. Li and X. He, "Review of non-isolated high-step up DC/DC converters in photovoltaic grid connected applications," IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1239–1250, Apr. 2011.
- [3]. K. W. Ma and Y. S. Lee, "An integrated fly-back converter for DC uninterruptible power supply," IEEE Trans. Power Electron., vol. 11, no. 2, pp. 318–327, Mar. 1996.
- [4]. Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC–DC converters," IEEE Trans. Power Electron., vol. 18, no. 1, pp. 65–73, Jan.2003
- [5]. G. C. Silveira, F. L. Tofoli, L. D. S. Bezerra, and R. P. Torrico-Bascope, "A non-isolated dc–dc boost converter with high voltage gain and balanced output voltage,"

IEEE Trans. Ind. Electron., vol. 61, no. 12, pp. 6739–6746, Dec. 2014.

[6]. C. T. Pan, C. F. Chuang, and C. C. Chu “A novel transformer-less adaptable voltage quadrupler DC converter with low switch voltage stress,” IEEE Trans. Power Electron., vol. 29, no. 9, pp. 4787– 4796, Sep.2014.

[7]. P. Xuwei and A. K. Rathore, “Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles,” IEEE Trans. Ind. Electron., vol. 61, no. 5, pp. 2307–2315, May 2014.

[8]. C. T. Choi, C. K. Li, and S. K. Kok, “Modeling of an active clamp discontinuous conduction mode flyback converter under variation of operating conditions,” in Proc. IEEE Int. Power Electron. Drive Syst. (PEDS), 1999, vol. 2, pp. 730–733.

[9]. M. Prudente, L. L. Pfitscher, G. mmendoerfer, E. F. Romaneli, and R. Gules, “Voltage multiplier cells applied to non-

isolated DC–DC converters,” IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887, Mar. 2008.

[10]. J. Xu, “Modeling and analysis of switching DC–DC converter with coupled-inductor,” in Proc. IEEE Int. Conf. Circuits Syst. (CICC), May 12–15, 1991, pp. 717–720.

[11]. A. F. Witulski, “Introduction to modeling of transformers and coupled inductors” IEEE Trans. Power Electron., vol. 10, no. 3, pp. 349–357, May 1995.

[12]. F. S. Garcia, J. A. Pomilio, and G. Spiazzi, “Modeling and control design of the interleaved double dual boost converter,” IEEE Trans. Ind. Electron., vol. 60, no. 8, pp. 3283–3290, Aug. 2013.

[13]. P.W. Lee, Y. S. Lee, D. K.W. Cheng, and X. C. Liu, “Steady-state analysis of an interleaved boost converter with coupled inductors,” IEEE Trans. Ind. Electron., vol. 47, no. 4, pp. 787–795, Aug. 2000.

[14]. M. Kwon and B. H. Kwon, “High step-up active clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems,” IEEE Trans. Power Electron., vol. 24, no. 1, pp. 108–115, Jan. 2009.

[15]. K. C. Tseng and C. C. Huang, “High step-up high efficiency interleaved converter with voltage multiplier module for renewable energy system,” IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1311– 1319, Mar.2014.

## **AUTHORS PROFILE:**



**M.CHANDRA SHEKHAR** completed his B.Tech in Electrical and Electronics Engineering from PRRM Engineering College (JNTUH), Shabad in the year 2005 and received M.Tech in the stream of Power Electronics Engineering at Auroras Engineering college(JNTUH),Bhongir,

Nalgonda Dist, in the year 2012. Pursuing PhD in veltech Dr.RR& Dr.SR University Chennai. Currently working as a Assistant Professor in Annamacharya Inst of Tech & Sciences, Hyderabad, since 2012. And his areas of Interests are micro grid and renewable energy sources.



**G.RADHAKRISHNA** received B.Tech in Electrical and Electronics Engineering from Nalgonda Institute of Technology & Science(JNTUH) in the year 2013 and now pursuing M.Tech in the stream of Power Electronics Engineering at Annamacharya Inst. Of Tech.& Sciences,Hyderabad.

Department of EEE, Annamacharya Inst. Of Tech.& Sciences, Hyderabad, since 2012. His fields of interest are Power Systems and Power Electronics. So far, he has published 4 papers in International Journals and 1 paper in a National Journal.



**MR. JADAPALLI SREEDHAR** was born at Rajampet near kadpa(dist.),AP., India. He completed his B.Tech in Electrical and Electronics Engineering, from JNTU in the year 2002. He completed his M.Tech in Power Electronics from JNTU in the year 2006. Currently, he is pursuing PhD from GITAM University, Hyderabad campus on the topic 'Synchronous Buck Converter Applications'. He is working as Associate Professor in the