



## A 64-BIT FFT MULTIPLICATION USING VEDIC MULTIPLICATION

### SUTRA

K.SOWJANYA

Asst.Professor Department of ECE Anubose Institute of Technology,

K.S.P Road, New Paloncha, Khammam (Dist), Telangana, India-507115

sowjanya.kavuturu@gmail.com

**ABSTRACT:** Fast Fourier Transform is widely used in various fields like image and signal processing, Voice recognition systems etc. This paper “FFT using Vedic multiplication sutra” proposes a novel technique in order to improve speed and reduce the time delay in FFT Multiplication process. Vedic mathematics comprises of 16 sutras in that one of sutras namely UrdhwaTiryakbhyam sutra used here to improve the performance of FFT multiplier. Here, the proposed method “FFT using Vedic multiplication sutra” is compared with the one of the popular multiplier namely Array multiplier in terms of delay which shows better result.

**Keywords:** Fast Fourier Transform, Array multiplier, UrdhwaTiryakbhyam sutra, Vedic Mathematics.

### I. INTRODUCTION

FFT is a highly efficient procedure for computing the DFT of finite series and requires less number of computation than that of direct evaluation of the DFT. FFT reduces the computations that of direct the calculation of the coefficients of the DFT can be carried out iteratively. FFT reduces the computation time required to compute a Discrete Fourier Transform and improve the performance by a factor 100 or more over direct evaluation of the DFT. The complex multiplication in FFT algorithm is performed based on the Array algorithm. This algorithm is quite popular in modern VLSI design. A new approach to multiplier design based on ancient Vedic Mathematics is used to improve the speed of

multiplication. UrdhwaTiryakbhyam sutra in Vedic mathematics explores a novel method for implementation of 32-point FFT using array multiplier was replaced by Vedic mathematics in Radix-2 algorithm. By using this Vedic mathematics in FFT algorithm, it improves the Speed of FFT algorithm which is used to compute the discrete Fourier transform.

### II. FFT ALGORITHM

The Fast Fourier Transform is a highly efficient procedure for computing the Discrete Fourier Transform (DFT) of a finite series and requires less number of computations than that of direct evolution of DFT. The FFT is based on computation on

decomposition and breaking the transform into smaller transforms and combing them to get total transform. The DFT of a sequence can be evaluated using the formula

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-j2\pi nk/N} \quad 0 \leq k \leq N-1$$

Here FFT multiplication was implemented based on Radix-2 algorithm. In Radix-2 algorithm, two bits are taken as input and we get two output bits dependence upon the arrow operations. The basic block diagram of DIF-FFT was shown in Figure.2.1.

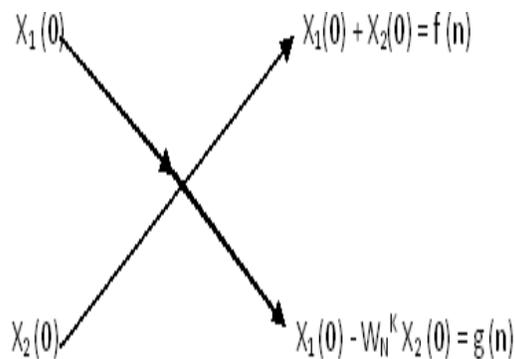


Figure.2.1: Basic butterfly structure of DIF-FFT using Radix-2 algorithm

### III. 64-POINT FFT

In 64-point FFT, there are five stages, which contain unique butterfly structure. Input is taken in normal order at first stage and the inputs for other stages dependence upon output generated by preceding stage butterfly structure. The output is taken in bit-reversal order at last stage. The block diagram for 64-point FFT is shown in Figure.2.2

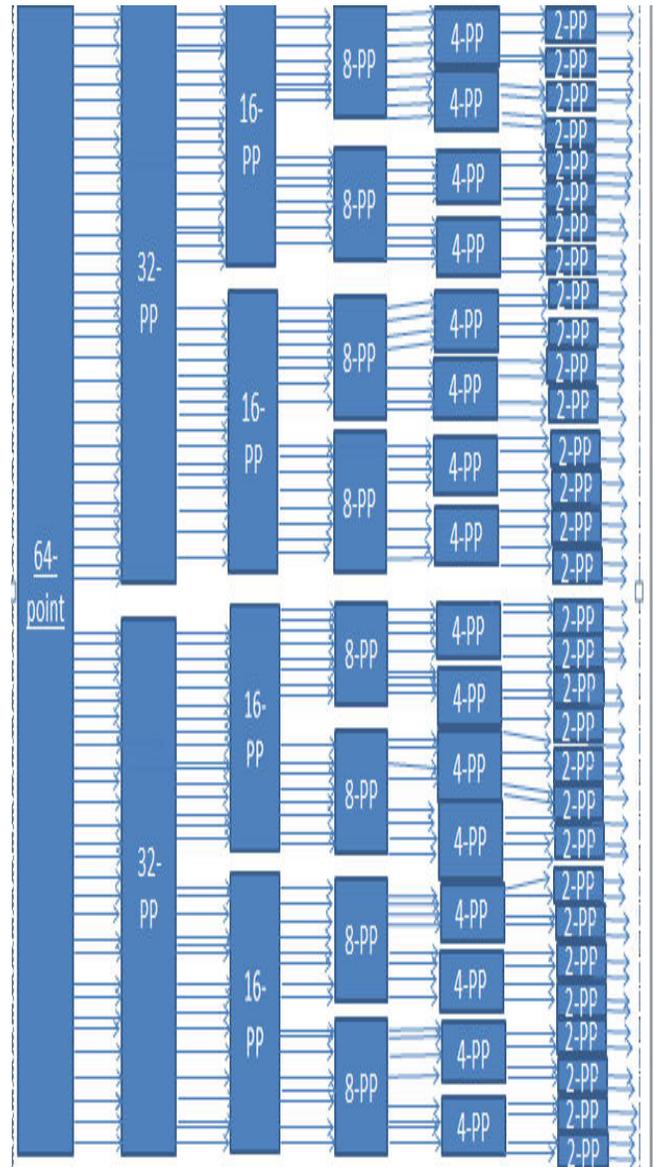


Figure 3.1:64-point FFT block diagram

### IV.ARRAY MULTIPLIER

Array multiplier is an electronic hardware device used in digital electronics or a computer or other electronic device to perform rapid multiplication of two numbers in binary representation. It is built using

binary adders. The rules for binary multiplication can be stated as follows

- 1) If the multiplier digit is a 1, the multiplicand is simply copied down
- 2) If the multiplier digit is a 0 the product is also 0.

For designing a multiplier circuit we should have circuitry to provide or do the following three things:

- 1) It should be capable identifying whether a bit 0 or 1 is.
- 2) It should be capable of shifting left partial products.
- 3) It should be able to add all the partial products to give the products
- 4) It should examine the sign bits. If they are alike, the sign of the product will be a Positive, if the sign bits are opposite product will be negative. The sign bit of the Product stored with above criteria should be displayed along with the product.

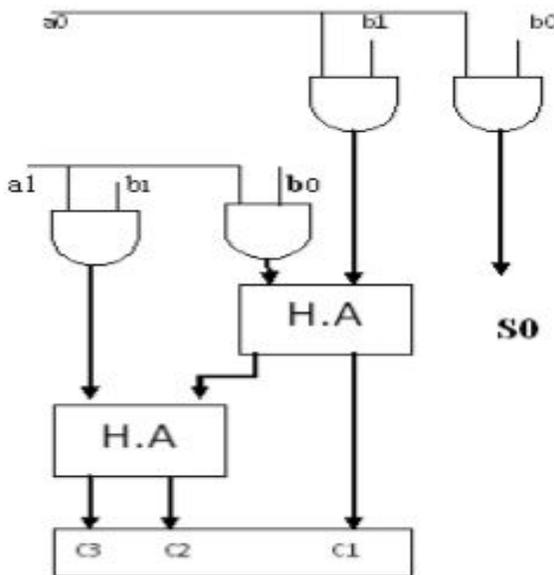


Figure.4.1 General Binary Multiplier

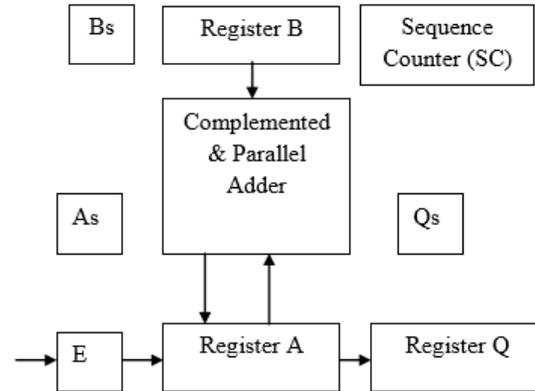


Figure.4.2 Hardware for General Binary Multiplier

## V. PROPOSED VEDIC MATHEMATICS

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The multiplier is based on an algorithm UrdhvaTiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. UrdhvaTiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using UrdhvaTiryakbhyam explained in figure below. The algorithm can be generalized for  $n \times n$  bit number.

The proposed 8\*8 Vedic multiplier produces was explained in Figure 4.1..

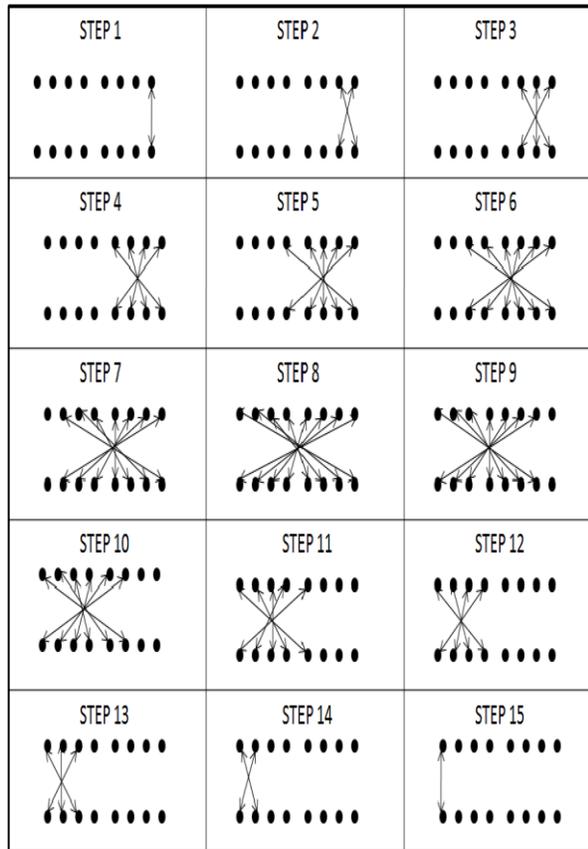


Figure 5.1: Multiplication Process in UrdhvaTiryakbhyam

Equations obtained in Vedic multiplier based on UrdhavaTiryakbhyam sutra are

$$\begin{aligned}
 P_0 &= A_0 * B_0 \\
 C_1P_1 &= (A_1 * B_0) + (A_0 * B_1) \\
 C_5C_4P_3 &= (A_3 * B_0) + (A_2 * B_1) + (A_1 * B_2) + (A_0 * B_3) + C_2 \\
 C_7C_6P_4 &= (A_4 * B_0) + (A_3 * B_1) + (A_2 * B_2) + (A_1 * B_3) + (A_0 * B_4) + C_3 + C_4 \\
 C_{10}C_9C_8P_5 &= (A_5 * B_0) + (A_4 * B_1) + (A_3 * B_2) + (A_2 * B_3) + (A_1 * B_4) + (A_0 * B_5) + C_5 \\
 C_{13}C_{12}C_{11}P_6 &= (A_6 * B_0) + (A_5 * B_1) + (A_4 * B_2) + (A_3 * B_3) + (A_2 * B_4) + (A_1 * B_5) + (A_0 * B_6) + C_7 + C_8 \\
 C_{16}C_{15}C_{14}P_7 &= (A_7 * B_0) + (A_6 * B_1) + (A_5 * B_2) + (A_4 * B_3) + (A_3 * B_4) + (A_2 * B_5) + (A_1 * B_6) + (A_0 * B_7) + C_9 + C_{11}
 \end{aligned}$$

$$\begin{aligned}
 C_{19}C_{18}C_{17}P_8 &= (A_7 * B_1) + (A_6 * B_2) + (A_5 * B_3) + (A_4 * B_4) + (A_3 * B_5) + (A_2 * B_6) + (A_1 * B_7) + C_{10} + C_{12} + C_{14} \\
 C_{22}C_{21}C_{20}P_9 &= (A_7 * B_2) + (A_6 * B_3) + (A_5 * B_4) + (A_4 * B_5) + (A_3 * B_6) + (A_2 * B_7) + C_{13} + C_{15} + C_{17} \\
 C_{25}C_{24}C_{23}P_{10} &= (A_7 * B_3) + (A_6 * B_4) + (A_5 * B_5) + (A_4 * B_6) + (A_3 * B_7) + C_{16} + C_{18} + C_{20} \\
 C_{27}C_{26}P_{11} &= (A_7 * B_4) + (A_6 * B_5) + (A_5 * B_6) + (A_4 * B_7) + C_{19} + C_{21} + C_{23} \\
 C_{29}C_{28}P_{12} &= (A_7 * B_5) + (A_5 * B_6) + (A_5 * B_7) + C_{22} + C_{24} + C_{26} \\
 C_{30}P_{13} &= (A_7 * B_6) + (A_6 * B_7) + C_{25} + C_{27} + C_{28} \\
 P_{14} &= (A_7 * B_7) + C_{29} + C_{30}
 \end{aligned}$$

## VI.RESULTS&CONCLUSION

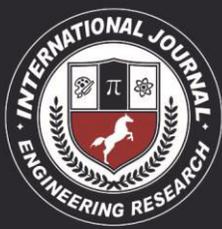
Here the proposed method “FFT using Vedic mathematics” is compared with existing multipliers in terms of delay with different families of Xilinx10.1 shows that the proposed method has a better result shown in below table.

Families	Radix-2 modified booth algorithm	Proposed Urdha tiryabhyam
On Spartan-3	52.754	47.85
On Spartan-3A & Spartan-3AN	47.178	38.72
On Spartan-3E	46.406	36.66
On Virtex-2	34.924	30.42
On Virtex-4	29.51	25.876
On Virtex-5	23.59	15.75

Table.1: Time delay (ns) results of the FFT algorithm implementation on xilinx 10.1

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