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DESIGN METHODOLOGY FOR VOLTAGE SCALED CLOCK DISTRIBUTION NETWORKS

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ABSTRACT
An improved positive edge triggered flip flop (M-PETFF) is proposedfor Low power application with simpler structure, clock load and also compared with different flip flop designs with same size of transistor including of both input and output. The proposed work implemented in CMOS-90nm technology, gives 32% of power optimization and high performance of PDP.
Keywords: flip-flops, low power and power optimization.

1. INTRODUCTION
The millions of transistors are integrating on one chip called Soc (system on chip) technology, while the covering and cooling have a partial capacity to eradicate the overload heat. All account of these the power consumption is key part to achieve the high performance stated in ITRS 2008 and also it is listed as one of the top three challenges in VLSI system. From that Clock system is the one of the most power consuming components in a system which consists of the Flip Flops and latches [1], [2]. The 30% to 60%of total power dissipates in an entire clocking system [1]. As a result, if the power consumption of flip flop is reduced which leads major impact on the total power consumption. A huge section of the power consumption is carried by the clock drivers.The Survey of the Flip flops stated [1]-[19], from that the single-edge triggered Flip flop are avoiding the node transition and minimize the power dissipation. But further reductions of power consumption, the double edgetriggered flip flop design are anticipated. In general the pulse triggered flip flop design, the speed is increased by minimizing the transistor during discharge path and also AND gate removed from the critical path because of reduction of complexity of the circuit and speed-up the discharge operation [3]-[7].The clock swing tree synthesis methodology is

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implemented with a tradition clock swing D flip-flop design is to protect the performance of IC. Another two schemes are used for design of low power FF: reduced swing and multiple-supply voltages. A Reduced swing methodology are proposed to decrease the RC delay of a long RC interconnects and power reduction [9]-[13].Consideration of all the drawbacks, we proposed an improved positive edge triggered Flip flop (M-PETFF) design for low power VLSI systems. The design manages the propagation delay in all the node while giving the input signal and it increases the speed of data transition and also reduces the circuit complexity. Moreover this entire latch design is implemented by introducing a sleep node and sleep bar node in the circuit for extra signal driving and to reduce the leakage power.

2. PROPOSED FLIP FLOP DESIGN

A. Conventional type Flip Flop design

Recent few years massive number of flip-flops and latches where designed under static and dynamic styles. The some of the existing flip flop designs are going to review. First flip flop shows in the Figure-1 PFF design, it contain explicit pulse generator for clocking system. If the data input and Q node are at the same position during the clock pulse occurs, the data transition and current does not reaches through the pass transistor MNx, Then the input and output data feedback may be consider pull down path of X node and opposite signal levels. So, for some internal nodes signal switching not take place. The data transition from 0 to 1, X node is discharged to revolve on transistor MP2 to make node Q is high. By the signal feed through scheme to get the better performance, the input source directly feed through the pass transistor MNx and the propagation delay can be concise. Hence the PFF design seems to be difficult for charging or discharging process that is common disadvantage for all the pass transistor logic [8].

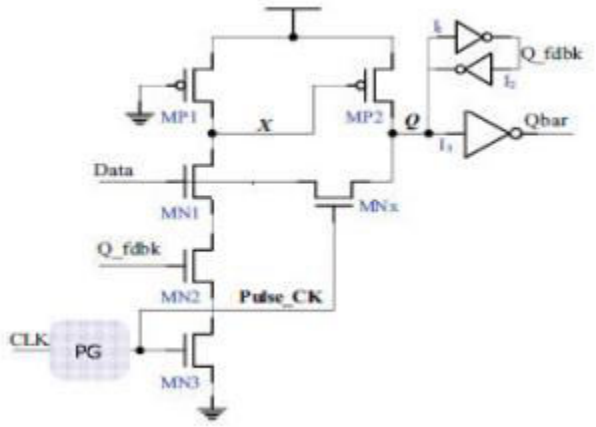

Figure-1: PFF design.

The Second comparative Flip flop design shows in Figure-2 [15], which is based on the frequently used static DFF. Still, pass gates with N1, N2, N5, and N6 (nMOS transistors) are used as the switches in master latches and slave latches. Accordingly, when the clock swing signal is 1, the nMOS transistor N1 and N6 can entirely switch OFF because the pass gates cannot leads voltage to the output. This problem is critical because the arriving input data signal works at FS. Therefore, A node cannot arrive at a full VDD, thus raising the outflow current and short circuit in the subsequent stages and the clock to output delay is increased. Moreover for the process variation, the pass transistors are not as much of strong. To improve this critical

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issue, two pMOS transistors with a pull-up network are supplementary to master and slave latches. The M node transitions to logic 0, transistor p1 switch ON. If the data signal is also at logic 0, then node A is pulled to full VDD throughout P1 and P2. During that master and slave latch are complementary to avoid leakage current and minimize power consumption.

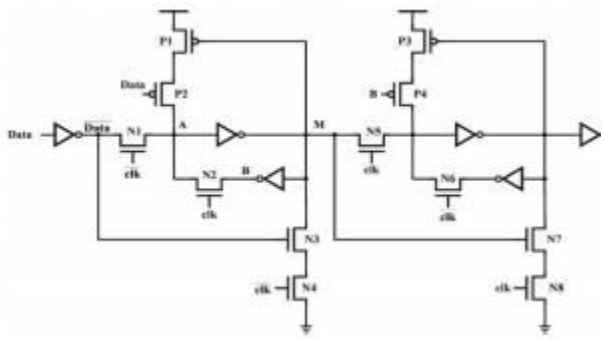

Figure-2: DFF design.

The third comparative Flip flop design shows in Figure-3 M-SBFF [19], which is used to recognize a low power and high speed FF design. The M-SBFF design reduces the load capacitance and generates the fast signal. It consists of a storage latch and inverter instead of XOR gate in order to speed up the charge and discharge of signal X. Moreover, the transistor M0 discharge the current to ground which gives the storage latch speed will be more. Additionally, two AND gates and signal X which enable the data and data bar. When CLK=0, X=1 the data and data bar are enabled and the signal X pass throughgates of M1 and M4.Consequently,the data and data bar are the function of the storage latch. The impact of gates (AND1 and AND2) does not reduce the speed of the FF design.

Due to delay of the inverter the storage latch holds the preceding data when the M0 switch is closed. When M0 is open, signal X= 1 and CLK transition from 0 to 1.Finally this design provides an increased speed and reduced power consumption.

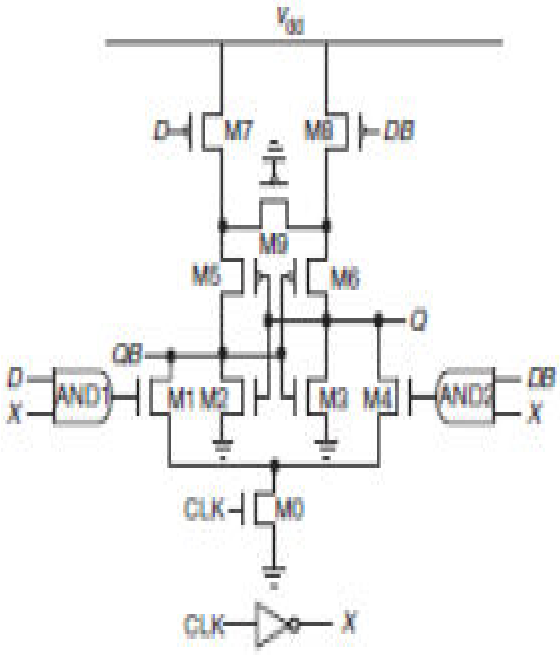

Figure-3: M-SBFF design.

B. An improved positive edge triggering Flip flop design

From the background work the following methods P-FF, DFF and M-SBFF are used which divide dynamic node to minimize the pre-charge capacitance and consumes power in most of the conventional designs. To rectify the large power dissipation in the existing architecture, the data holding time, removal of complex logic functions and increases the Delay in the flip-flops design which turns the huge power dissipation. The drawback has been overcome by the improved Positive Edge triggering (M-PETFF) Flip flop Design.

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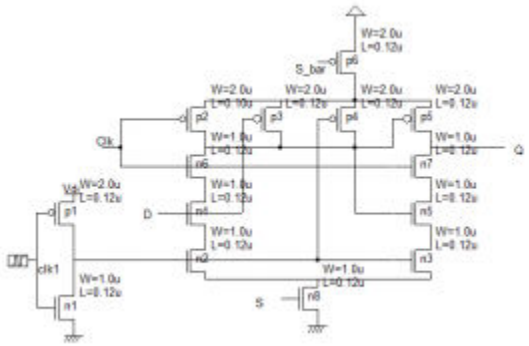

Figure-4: M-PETFF.

In M-PETFF is constructed by totally 14 numbers of transistors. In existing method clock activity is based on Pulse generator and it is controlled through four inverter, AND gate, Mnx and Mn3 transistor as shown in the Figure-1[8].Apart from that it also depends on the input data which is passed on to Mn1 transistor and through Mnx transistor. Although requires M-PETFF two transistors for clock activity. Hence the proposed design has less clock activity than P-FF.A typical M-PETFF structure is shows in Figure4. The Clock activity is based on the CMOS inverter n1 and p1. During the clock activity, NMOS transistor n2, n3, n6, n7 are open. At the same time, if D = 1 then n4 also open, immediately the X node pulled down the voltage to ground due to sleep bar as low in transistor p6 then p5 is open and pulling Q=1. if D = 0 then p3 will be open, immediately the X node is pulled up Vdd, which turns n5 will be open then Q=0. The propagation delay for the Q node high is n2, n3, n4 and p5 and the propagation delay for the Q node low is n5, n6, n7.The transistor p2 is used for precharing when node X = 1.if D=1, p2 is used to keep X=1 and to keep X=0. When CLK=1, P3 is used for pre charging node X=1,in order to avoid Q node from toggling. Hence conclude that, when a CLK=1, D=1 thenthe flip-flop stores as 1. If CLK=0,D=0 then flip-flop stores as 0. Additionally, n8 and p6 transistors are operated with high threshold voltages to reduce the leakage power. This facilitates the power dissipation lesser then the conventional FF.

3. PERFORMANCE ANALYSIS AND RESULTS COMPARISON

The proposed system is implemented by using micro wind simulation tool for the performance analysis. The supply voltage is 1 V and 2.5V for I/O supply voltage at27 degree. The Average power is found as the variation in proposed flip-flop design than the existing design. From that CMOS-90nm technology are simulated under similar conditions to extract the average power dissipation. This is calculated using

$$p = vdd.f \int_0^T Idd$$

Where, Vdd is the supply voltage, Idd is the supply current, t is the period, and f indicates the frequency of Power dissipation. Comparison on Average power, number of transistor used, Power delay product (PDP), Maximum Idd current, and power dissipation conventional flip-flop methodologies with M-PETFF using CMOS 90nm the technology

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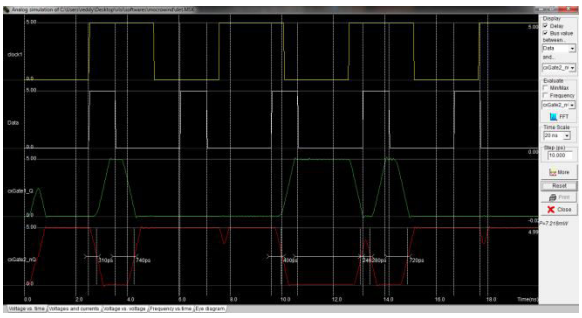

Figure-5: Simulation output results of M-PETFF using CMOS-90nm technology.

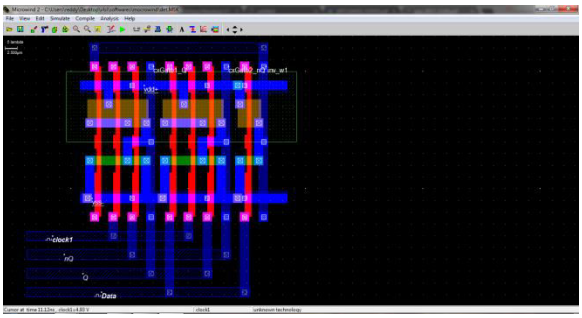

Figure-6: Layout diagram of M-PETFF Design

The simulation results both output and layout diagram shows in Figure-5 and Figure-6, M-PETFF has the lowest power consumption than the existing FF. The power dissipation is depends on the switching activity of the transistor. For example, when clock rate is 0.5 and data for single end flip-flop (FF) is same as for the positive edge of the clock input and unequal at the negative edge. The data activity increases further the M-SBFF design dissipates higher power.

4. CONCLUSION

In this work, a novel low power M-PETFF is proposed. An analysis of the entire work is done by Microwind tool. The proposed M-PETFF design which works efficiently in terms of switching activity of clock and data which results low power dissipation than DFF, PFF and M-SBFF. A comparison shows that lower power dissipation and Idd current along with comparable high performances by reducing number of transistor count. The layout simulation results shows reduced Power consumption and improved PDP. Furthermore by reducing the unwanted switching activity the revised structure of M-PETFF flip-flop, is efficiently utilizing complex logic in to the flip-flop.

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