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DESIGN A NOVEL BUILT IN SELF TEST USING MULTIPLE MEMORY INSTRUCTIONS

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ABSTRACT:

Basically at the time of system on chip era, the embedded flash memories are most widely used. This flash memories are another type of memories which is non volatile on floating gate transistors. In the test procedure the flash memory is used as an ad hoc to develop the specific design. But in flash memories large number of failure modes are occurred. Because of this the automatic test equipment becomes more complicated to test. In SRAM there is an production of row and column address bit cell. This might occurs sa0 and sa1 faults in chip design. Now this faults will be reduced by using separate row and column address cells. This row and column address cells gives perfect location to store the data. By extending the memory of an array we can verify the memory location. This memory location can be chosen by column address buffer and row address buffer. This process in system gives perfect location to check all cell operation's.

I.INTRODUCTION

The important role play of SRAM increased in Soc (System-on-Chip) applications. Statistics shows that on average the total area of the chip exceeded 50% by SRAM. In reported by us on the development of the smallest high-density 6T-SRAM cells for SOC using standard CMOS processes (3.87um2 for 0.18um technology node and 1.87 um2 for 0.13um technology node).And these particular cells are the most suitable in the applications of SOC to meet the demand for high-density and high-performance and are vastly manufacturable.

To make sure their manufacturability, robustness and reliability, ordinary PCM (Process Control and Monitoring) structures of test aren't adequate to monitor the process for the high density
RAM, due to specific interactions between the SRAM design and the process. PCMs of ordinary are more generic in nature and are aimed at supporting the process module of robust development characteristics and robust generic design rules (rules that can be used in any possible combinations and design environments). Therefore, these structures may not always allow us to test for the robustness of the chosen design of SRAM rules of their environment of the specific SRAM array. For example, a structure of conventional poly bridging is designed that the robustness of the minimum poly-to-to-poly spacing design rule to be proved for very long and parallel poly lines. This structure may not be suitable for providing feedback for our SRAM, as typically the poly layer features of SRAM are more complex.

The metal bridging also may be applied same, where the SRAM pattern is more complex in nature than that of a simple collection of metal lines of parallel and spacing of uniform. A conceptual change in designing and using electrical test structures for SRAM-driven process development is thus needed: test structures need to be process-development driven as well as product driven. The set of the structures of the test is used for

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developing and characterizing the process needs to be complemented with a set of suitable structures that prove the robustness of the high density SRAM design and help quickly be identified and related yield issues to corrected the process and to be designed in SRAM during the development phase.

II.DESCRIPTIONS OF THE STRUCTURES OF THE TEST

The parameters of the electrical used to prove the robustness of our SRAM designs include Measurement of leakage current the bridging of inter- and intra-layer, Resistance measurement to detect integrity of connections, SRAM transistor characterization to monitor any possible deviations from targets and beta ratio and evaluation of static noise margin to the design of SRAM's functional robustness.

The designed test structures must be sensitive enough to allow monitoring of both systematic and random occurrences of any possible weakness of the memory cell. We also need to characterize the transistors of SRAM in accuracy, static noise margins and beta ratios within the SRAM array environment. Hence, in our test chip of SRAM qualification, SRAM test structures have been designed by us to ensure SRAM cell robustness and characterize SRAM devices.

To ensure the manufacturability of our SRAM cells, we designed a series of test cells which are target based SRAM cell. Each cell modification enables us to test one specific robustness requirement in the SRAM cell. We use these modified SRAM cells to build larger arrays (~10,000 to cells of 100,000) the SRAM cells repeated just like in an SRAM array. The parameter of interest (resistance, leakage current, etc.) is after that the entire array would be measured. Hence, statistical information is gathered from a huge number of cells, hence the confidence levels will be increased of the quality of robustness for each individual design rule or feature. The particular structures of array helps us to determine any additional SRAM cell design modifications that further improve its manufacturability, give feedback on the sensitivity of chosen critical design rules to process variations, and ultimately be able to use to quick test of the proposed process impact modifications to the SRAM design.

Compared to traditional structure designs of PCM test, this innovative concept has the advantages as follows. Test structures are more SRAM-cell-oriented, hence dedicated to prove the robustness of the cell design. The data is collected from the true SRAM array environment; hence captures process to design interactions, as is usually observed in real products. Finally, these structures allow evaluation of all the cell of SRAM rules of specific design as it is used in the SRAM array environment. Another way to determine the critical design robustness rules is by split design rather than process split. In this method we apply a constant bias to a layer of critical and followed by study inter-layer and intra-layer effects. For example, we size the poly layer by 10% of its minimum feature size, and then study effects such as poly to poly bridging or contact to poly bridging, or monitoring of the overall impact on cell leakage as that of function of this bias. Typically, the same information could be collected by a split lot experiment at photo or etch. This method however, enables us to study the robustness of the rule of specific design over a massive amount of lots and to be allowed us to the study the additional margin of the design rule of choice when a process split has been applied. This operation

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of biasing had been applied by us on all critical layers, e.g. poly, contact and metal 1.
Read Only Memory (ROM). The instruction address is the address of particular instruction Stored in the Memory. For the particular address respective instruction is saved in the ROM. It just reads the particular instructions from the required address. Hence this part in this work is replaced by an ROM.
Instruction Decoder Unit: This unit generally takes input as a 32-bit instruction and outputs all the required instructions and these specified values are input to next part of circuit. The block diagram of Instruction Decoder unit is shown here.

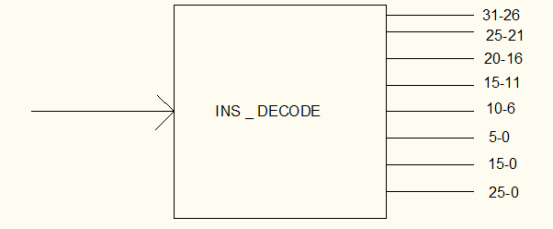

Fig 1 Instruction Decoder

Data Memory:This is the second memory of the MIPS. This memory can be used for both Read and Write applications. Hence this circuit can be replaced by a Random Access Memory. The input is the address and if read signal is enable it reads the data from the inputs memory location. If write signal is enable it writes the data into the input's memory location.

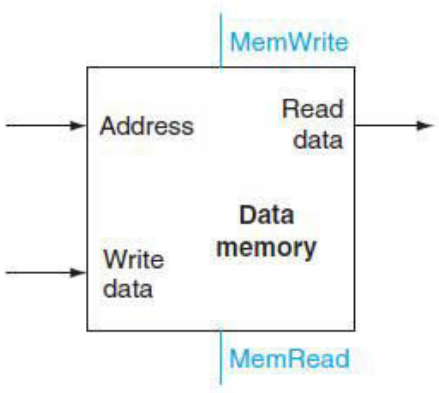

Fig 2 Data Memory

III.PROPOSED DESIGN

In exiting system there is no cell checking operation so it may not verifying the memory location twice. There is single memory cell array to send the data in single phase. There are the two problems in existing system, to overcome these problem we are proposing a new architecture.

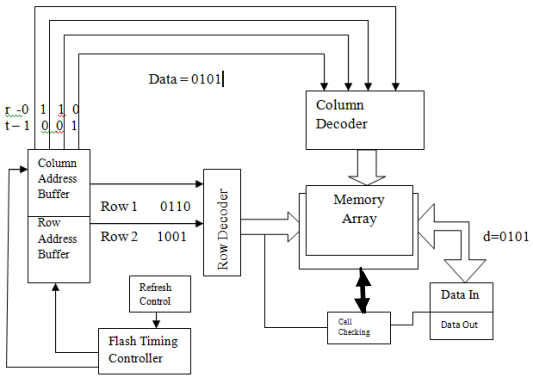

Fig 3 Proposed system

The proposed system consisting of refresh control, flash timing controller, column address buffer, row address buffer, column decoder, row decoder, memory array, cell checking, data in/data out.

The refresh controller and flash controller will refresh all the data in memory array location. The row address buffer and column address buffer will send the buffer of address it may column or row. The address buffer is taken by their respective decoder, means column address buffer is given to column decoder and the buffer of address is decoded. Similarly row address buffer is given to row decoder to decode the buffer of address.

The output of row decoder and column decoder will select the memory location in memory array. As per the changing of row or column address buffer the decoder will change the memory location. The total memory location will call it as memory array.

The cell checking block will check either to select the memory location array i.e. S=0 or 1. If S=0 the memory location array one will select, and the data is impend in that array

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memory location. Else S=1 the second array memory location will select and the data impend in second memory array location.

The date-in used to write the data and data-out is used to read the data memory array. By using this proposed system we overcome checking the memory array and to array of two memory locations.

IV.RESULTS

The below figure 4 shows the RTL Schematic of proposed system

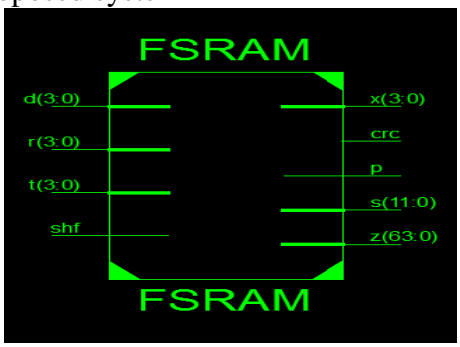

Fig 4 RTL Schematic

The developed proposed system with technology schematic is shown in below figure 5.

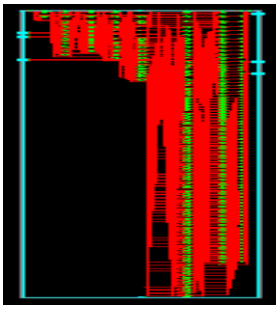

Fig 5 Technology Schematic

The total output is shown in below figure 6 as per the address of column and row the data is stored in that respective memory location

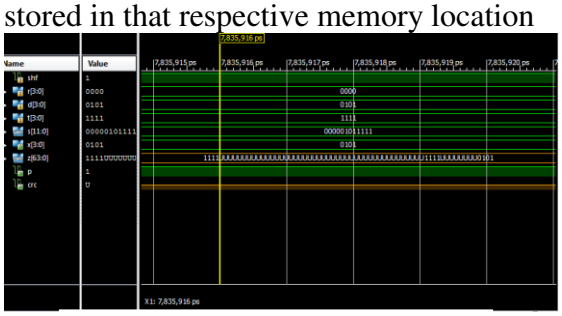

Fig 6 Technology Schematic

V.CONCLUSION

As studied earlier that in flash memory there will be large number of failure modes. The SRAM cell produces row and column address bit cells. This row and column address bit cells might gives sa0and sa1 faults. Now this can be reduced by using separate row and column address cells which gives perfect location to store the data. We can verify the memory location by extending the memory array. The memory arrays can be row or column address buffers. This system gives perfect memory location for cell checking operations.

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