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DESIGN AND ANALYSIS OF OPERATIONAL AMPLIFIER USING 180NM TECHNOLOGY FOR DATA COVERTER APPLICATION

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ABSTRACT:This paper presents 1.8 V, two stages operational amplifier for Biomedical applications. To achieve a proper performance with given supply, a low power, high gain operational amplifier is introduced. The operational amplifier is designed in a standard TSMC 180nm CMOS process. The two-stage cascaded op-amp achieves 72.2dB of gain, 58.70° phase margin while consuming power less than 3mW. Also, it achieves a good voltage swing, it gives 82.3 dB common mode rejection ratio and 22.3 V/uS slew rate. Also, it is designed for ICMR of 0.6V to 1.6V. Miller compensation is used to achieve a good stability. Simulation is done using Cadence and Tanner tools. This operational amplifier is used in various applications like signal processing, bio medical and communication as per the required specifications.

Key Words: Data converter; op-amp; cadence; tanner; low power; High gain; High speed.

1. INTRODUCTION

In today's world, a great amount of analog, digital and mixed signal processing systems consider data converters in order to produce analog or digital outputs for various applications. In these types of applications, an off-chip data converter is normally employed. Analog to digital converter and Digital to Analog converters are largely used in the digital world e.g. latest audio signals are stored in digital form converted into analog form in order to be provided to speaker. Thus, DACs are used in MP3 players, MP4 players and CD players [1]. Also video signals from digital sources. Here the general diagram of an application is discussed in Fig.1

In analog and mixed-signal systems, an operational amplifier is versatile building block.

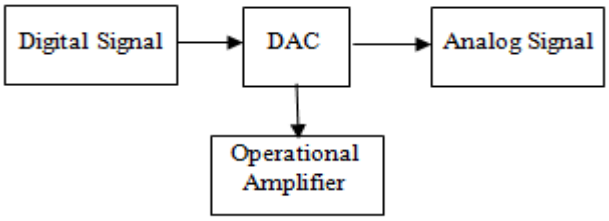

Fig 1 Basic block diagram

It is generally used to amplify weak or small signals, to perform differentmathematical operations on electrical signals, and in active filtering. It must have parameters like low power, high gain, high input resistance, good output swing, high common mode rejection and should function over a variety of frequencies for the data converter.

2. OPERATION AND ARCHITECTURE

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In this section, the architecture of digital to analog converter and operational amplifier are going to be discussed.

➢ OP-Amp Architecture

The two-stage CMOS operational amplifier includes four major circuits - a bias circuit, an input differential amplifier, a common source amplifier as a second gain stage, a compensation circuit. The Input differential amplifier block considers the differential input of the op-amp and produces a good part of the total gain toimprove noise and other performances. The second gain circuit block is generally configured as a common-source stage so as to provide a good output swings with single ended output voltage [1]. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. Generally current mirror topology is used for biasing purpose. The role of the compensation circuit is to provide stability when the type of negative feedback is given to the op-amp. Also it provides a good phase margin. Fig.2 shows the block diagram of the op-amp circuit [4].

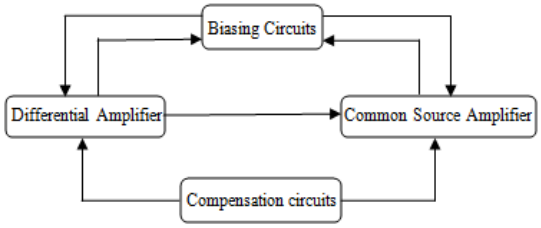

Figure-2 Block diagram of Op-amp

As shown in proposed circuit diagram, two stage op-amp is discussed. The first stage is considered as an input differential stage which consists of transistors – M1 and M2. The use of differential pair is to provide the single ended output from the differential inputs. For this differential pair, the biasing current is provided by the current mirror circuit- M3 and M4.The current from the differential pair is multiplied by first stage output resistance and by doing this single ended output can be achieved. This single ended output will be considered as the input of the second stage [10-3]. Below the general circuit diagram is shown.

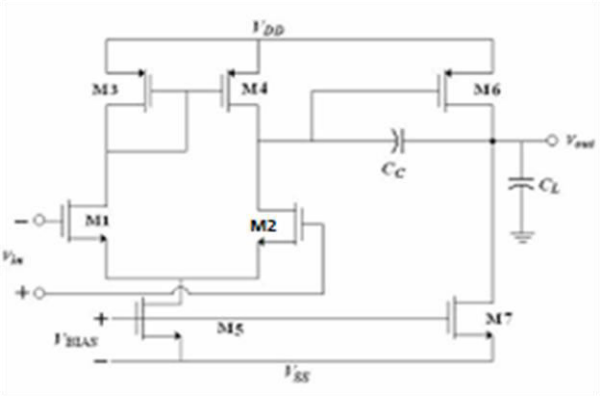

Figure 3 Op-amp circuits

3. DESIGN AND MODELLING

In this section, basic design methodology for op-amp design is going to be discussed. The basic block diagram for design flow is shown in Fig-4.

As per the design flow, the first stage is expected as proper specifications with precise form [1]. In the next stages, the optimized topology selection and as per that schematic design is carried out. Than As per the requirement of the performance parameters, biasing current and device sizing are carried out.

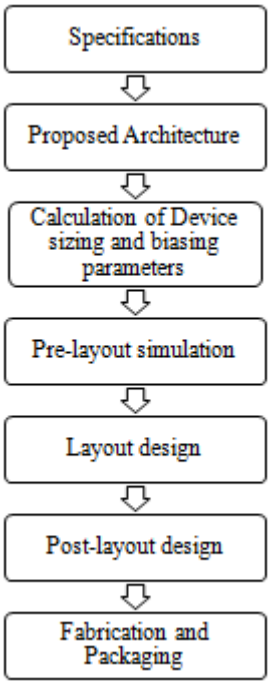

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Figure 4 Design flow

4. IMPLEMENTATION AND RESULTS

In this section, implementation of the two-stage op-amp (with TSMC CMOS 180nm technology) and current steering DAC are carried out. For two stage CMOS operational amplifier design, different analysis likes DC, transient and AC is carried out. Also, the different parameters of an op-amp are simulated to match with required specifications.

➢ Implementation of two stage CMOS op-amp

In this part, the specifications for the op-amp design are mentioned. Also the steps for op-amp design are mention to find device sizes as well as the other required values. Then the different analysis is carried out. Also the result of different performance parameters like DC gain, phase margin, output swing, CMRR, ICMR etc. is mentioned here.

In given table, specifications of an op-amp are shown.

Table 1 Op-amp Specifications

Parameters	Values
Supply Voltage	1.8V
DC gain	>70dB
GB	30MHz
PM	>55°
Slew Rate	20V/µS
CMRR	>80dB
C_L	2pF
P_{diss}	<3mW

➢ Steps for design

In this section, the important steps for op-amp design is mentioned.

As per the specification of C_L and phase margin, find out C_C.

•From slew rate requirements, biasing current from M5 is found.

•Transconductance for M1 is found and from this, W/L ratios of M1 and M2 are obtained.

•From the range of ICMR, W/L ratios of M3, M4 and M5 are obtained.

•From the requirement of zero and transconductance, W/l ratios of M6 and M7 are obtained.

In the table, the calculated values for W/L ratios are mention. These values are for standard TSMC 180nm CMOS technology. The assumed value of C_L is 2pF and calculated biasing current is 10uA. In this design the consider value of L is 500nm to reduce the effect of channel length modulation.

➢ DC Analysis

Here, result of DC analysis of proposed design is discussed in Fig.5

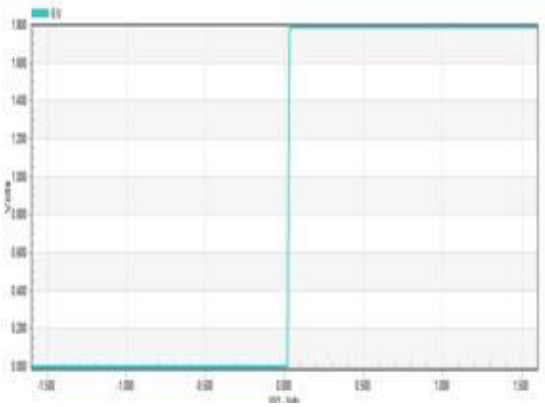

Figure 5 DC analysis

➢ Transient Analysis

Here, result of transient analysis proposed design is discussed in Fig.6

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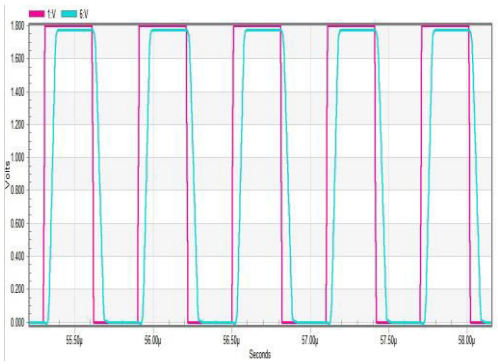

Figure 6 Transient analysis

➢ AC Analysis

Here, result of AC analysis of proposed design is discussed in Fig.7 The diagram represents the gain in dB and also the phase response. Also, the compensation effect is shown.

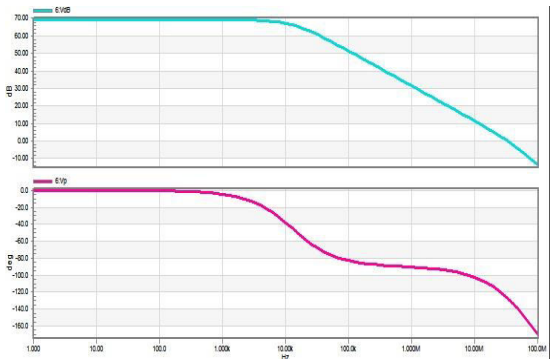

Figure 7 AC analysis

➢ Simulation for CMRR

Here, the result of CMRR is shown in Fig. 8

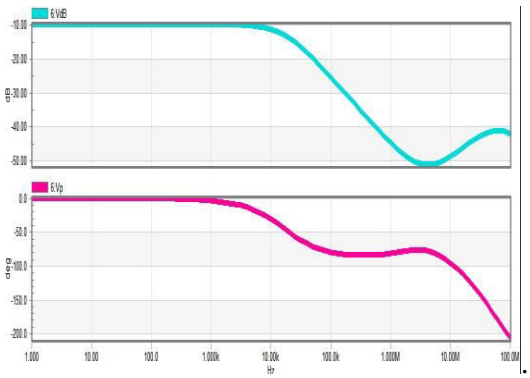

Figure 8 CMRR Simulation

➢ Simulation for Output swing

Here, the result of output swing is shown.

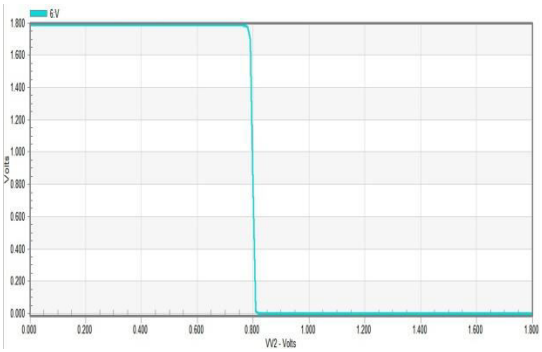

Figure 9 output swing simulation

➢ Result Summary

In this part, the final simulated results are going to be discussed. As shown in specifications, the different parameters of two stage CMOS op-amp are simulated using CMOS180nm TSMC technology. For simulation purpose, different methodologies to find different parameters are adopted. Here, different parameters like DC gain, CMRR, GB, Slew rate etc. are measured by considering the load capacitance of 2pF.

In table 2, simulated results operational amplifier with two stages is shown.

Table 2 Simulated results

Parameters	Values
Supply Voltage	1.8V
DC gain	72.2dB
GB	29.9MHz
PM	58.70°
Slew Rate	22.3V/µS
CMRR	82.3dB
C_L	2pF
P_{diss}	2.86mW

5. CONCLUSION

This paper presents a novel design of the two-stage operational amplifier using TSMC CMOS 180nm technology. With the supply voltage of 1.8V, two stage operational amplifier gives

72.2dB DC gain, 29.9 MHz GB, 58.30° phase margin, 22.3V/µS slew rate, 82.3dB CMRR. This simulation is carried out for 2pF load. In future, further improvement in various parameters is also possible. And also different optimized architecture of an op-amp with specific optimized parameters can be implemented.

REFERANCES

[1] "Defense Science Board (DSB) study on High Performance Microchip Supply," http://www.acq.osd.mil/dsb/reports/ADA435563.pdf, 2005.

[2] Veronica ErnitaKristianti, Hamzah Afandi, EriPrasetyoWibowo, BrahmantyoHeruseto,shintaKisriani, "Designing of a 8-bits DAC in 0.35 µ m CMOS Technology For High Speed Communication Systems Application".

[3] Xueqing Li, Qi Wei, Zhen Xu, Jianan Liu, Hui Wang, and Huazhong Yang, "A 14 bit 500 MS/s CMOS DAC using complementary switched current sources and Time Relaxed Interleaving DRRZ" IEEE transactions On Circuits and Systems-I : regular papers ,vol.61, no. 8, pp 2337-2347, Aug 2014.

[4] E. Srinivas, Dr. N. Balaji, Dr. L. Padma Sree, "design of low-voltage, high-gain operational amplifier for data converters", Progress In Science and Engineering Research Journal.

[5] Si-Nai Kim, Ba- Ro-saim Sung, Hyun-Wook Kang, Min- Hyung Cho, and Seung-TakRyu , "A SUC-Based Full-Binary 6-bit 3.1 –GS/s 17.7 mW current steering DAC in 0.038 mm2", IEEE Transcations on Very Large Scale Integration (VLSI) Systems, Vol. 24, no. 2, pp. 794-798, Feb 2016.

[6] Geunyeong Park and Minkyu Song, "A CMOS Current –Steering D/A Converter With Full- Swing Output Voltage and a Quaternary Driver" IEEE transactions On Circuits and Systems-II ,vol.62, no. 5, pp 441-445, May 2015.

[7] TriptiKackar, Shruti Suman, P. K. Ghosh. "Design of high gain low power operational amplifier", 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), 2016

[8] CHEN Mei-na, DAI Qing-yuan, ZHU Hong-wei and JIANG Shen-fei, "A Sample/Hold circuit for 10-Bit 100MS/s Pipelined A/D converters," Microelectronics, Feb.2007

[9] Biao Li,"A High DC Gain Op-Amp for Sample and Hold Circuits block of ADC" proceedings of the 2 nd International Conference on Computer Science and Electronics Engineering (ICCSEE 2013)

[10] Steven R. Norsworthy and Ronald E. Crochiere,"Decimation and Interpolation for ΣΔ conversion", in Delta-Sigma Data Converters,edited by S.R. Norsworthy, R.Schreier and G.C. Temes, IEEE Press, 1997.

[11] Amana Yadav, "Design of Two-Stage CMOS Op-Amp and Analyze the Effect of Scaling", International Journal of Engineering Research and Applications, 2012

[12] Brandon R. Greeizleyt, Uiz-Ku Moon, Raymond Veitht. "A 1.8 V CMOS DAC CellL With Ultra High Gain Op-amp in 0.0143 mm2", IEEE, 2001