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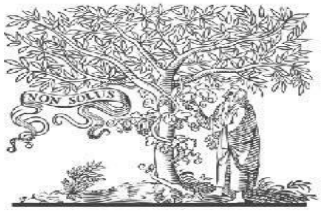

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DESIGN AND OF MULTIPLIER USING APPROXIMATE 15-4 COMPRESSOR

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ABSTRACT

The formation of a simple module for a approximately 15-4 compressor using a 5-3 compressor. Different kinds of approximately 5-3 compressors are employed in 15-4 compressors for their low power requirements and high pass rates. We will examinate the outcomes in each situation. The proposed 15-4 compressor simulates the 16x16 bit multiplier. According to the detection of the simulation, the multipliers with the propective approximate compressors significantly outperform the multipliers with the accurate 15-4 compressor in terms of power. In an imageprocessing application where the peak signal-to-noise ratio of the image is determined, the proposed multiplier is then employed. When the image quality is differentiate to the correct multiplier, the detection demonstrate that our suggested multiplier is effective.

Keywords: Approximate 5-3 compressor, Approximate 15-4 compressor, Multiplier, Image Processing, Higher order compressor

I.INTRODUCTION

The complication of a digital signal is handled in large part by microprocessors and digital signal processors (DSP). A digital signal is the foundation for about 95% of the processors now available. Filtering, correlation, and convolution of digital signals are handled by digital signal processors. For the most part, multipliers, shifters, and adders are utilized in this process. The multiplier module is the most complicated of the three. In comparison to the other two modules, multipliers require more time and power. Multipliers havethree stages: the formation of partial products, their reduction, and their ultimate addition. The multiplier uses a lot of time and energy to reduce partial products. Many different techniques were put out to shorten the multiplier's critical path. The use of compressors is one of them. Only when the multiplier is tiny are these useful. Multipliers that are 16 by 16 and 32 by 32 require huge compressors. In terms of power, speed, and area, high- order compressors outperform low-order compressors. All of these techniques carry out the exact calculation, and the modules deliver the right outcome. In accurate computing, the module's accuracy is always 100%. Exact computation, however, has one significant flaw. Exact computing cannot be used to optimize allof the circuit's parameters. Exact computing isn't necessary for every application, though. Some programs, including image processing and multimedia, can handle mistakes and still construct useful outcomes. Because they use less power and have a lower level of complication, approximation (inexact) computing approaches have gained popularity. Inaccurate calculations resultin Accuracy is defined as the distance between the central point and the most significant bit (MSB), and The erroneous part of adders is referred to as the least significant bit (LSB). A significant mistake is produced by inaccurate calculations onthe MSB side. The accurate part, however, employs the standard addition rule. In the erroneous part, adding is done using a unique technique. The "sum" value of theoutput is computed. normally wheneverany one of the adder's operand values is "0." From that bit position through the least significant bit, the value can be fixedas "1" when both operands are "1" or "sum". This method is used to reduce the adder's error distance. The output of the adder must be calculated using both XORand XNOR gates. There were three distinct approximations suggested. The "sum" and

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"carry" output formulas are approximations. One XNOR gate has been used to calculate the "sum" rather thantwo XOR gates. Similar to this, two AND gates, one OR gate, and one XOR gate are used for "carry." Methodologies of approximation were used to create the partial product phase. The reduction tree was released with a number of erroneous compressors. More inputs can be handled by compressors than by half-adders and full adders. Many researchers employ the 4-2 compressor, which divides the four partial products into two partial products. The approximation 4-2 compressor's error probability is 0.003, which is extremely low compared to any damaged adder circuit. used in the 16-bit Vedic multiplier, as suggested, and many approximation compressors. Further optimization of the 4-2 compressor is made to obtain the best power and minimize delay without sacrificing precision. In this study, two ideas for a roughly 4-to-2 compressor are suggested. The best compressor nowadays is the roughly 4-2-1 compressor in Design 2.The effectiveness of different multipliers was compared. It was discovered that adding compressors to the partial production tree produced the circuit metrics with the best circuit metrics, the lowest error rate, and the smallest normalized error distance. The higher-order compressor for a 16-bit multiplier that has been proposed A significant mistake results from the usage of numerous approximately 4-2 compressors in a large size multiplier. A minimum inaccuracy and respectable circuit performance are required.

II. Prototype of approximate 5-3 compressors

A. Prototype 1

Fig. 1 depicts the typical 5-3 compressor construction. A typical 5-3 compressor has three outputs and five inputs. Five incomplete products will be condensed into three outputs. There are two MUX gates, one AND gate, and five XOR gates. Three XOR gates are necessary to produce O0. More important delays occur at the XOR gate than at any other gate. so traditional The 5-3 compressor uses more power and has a longer delay. It is feasible to improve this compressor still further. The proposed design outperforms traditional structures in terms of performance.

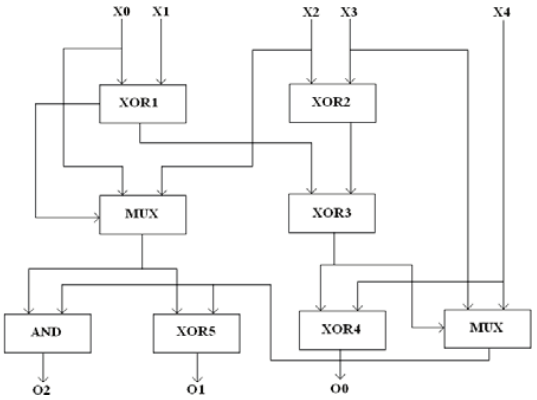

Figure 1: Circuit diagram of 5-3 compressor

B. Prototype 2

To significantly minimize energy usage with a very low mistake rate, we suggest a unique approximate adder architecture. The applied carry prediction technique, which utilizes the data from less significant input bits in a parallel way, is what accounts for the greatly reduced error rate and critical path time. To further minimize the aggregate of mistakes after they have been recognized at a minimal cost, an error magnitude reduction strategy is proposed. The suggested adder is demonstrated to be up to 2.4 times quicker and 43% more energy efficientthan conventional adders, with an error rate of only 0.18%, when implemented in a commercial 90 nm CMOS process. Unsupervised learning has been used to include the suggested adder into a VLSI-based neuromorphic character recognition circuit. It has been demonstrated that the suggested adder's approximation errors have no effect on training. Additionally, a scaled supply level allows for energy savings for the neuromorphic circuit of up to 48.5% over conventional adders. Finally, by using low-overhead error-correcting circuitry, we obtain error-free operations.

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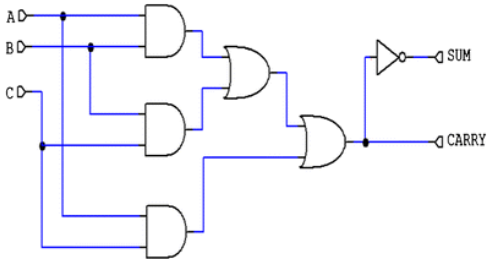

Figure 2: Approximate Adder

C. Prototype 3

Booth encoding is thought to produce multiplier designs that are faster but consume more energy. Under a variety of restrictions, 16x16-bit booth and non-booth multipliers are estimated in energy and delay space. It is demonstrated that with strict delay targets, non-booth multipliers begin to become more energy efficient. Novel 3:2 and 4:2 compressors are also provided in order to conserve energy while maintaining the same desired delay. Depending on the target delay at 65nm CMOS technology, the proposed compressors can reduce energy by up to 20%. The proposed compressors offer a performance gain as the voltage is scaled from its nominal value thanks to a non-Booth multiplier implementation. Additionally, we looked at every design at the CMOS technology nodes of 45nm, 32nm, and 22nm.

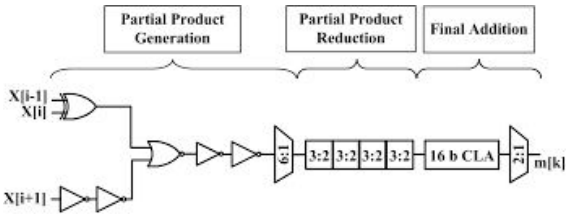

Figure 3: Circuit diagram of Booth Coding

III. PROSPECTIVE SYSTEM

A. Prototype of 5-3 compressor

Five XOR gates are used in a traditional 5-3 compressor to provide the output. The circuit has been redesigned to make less use of XOR gates. Three 4-1 MUX are used to design the prospective 5-3 compressor. Two partial products are provided as control signals for the multiplexer, and three partial products from the partial product array are provided as input. As readily available control signals, D and E are provided. The production of output (O1, O2, and O3) is hence quicker. Because only one input is ever active based on control signals (D&E), multiplexers are known to operate faster and with less power. The suggested 5-3-2 compressor is designed based on this concept. The following equation describes the proposed 5-3 compressor. A new 5-3-2 architecture is suggested based on the updated equation. 5-3 compressor proposal

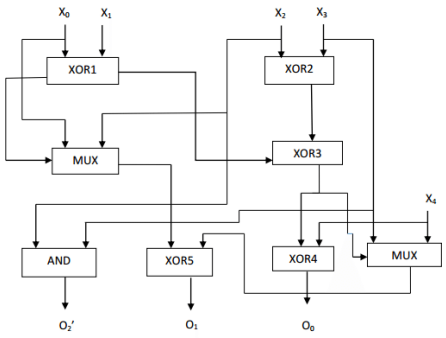

Figure 4: Circuit diagram of 5-3 compressor

B. Prototype of 15-4 compressor

The design of a 15-4 compressor employing roughly 5-3 compressors is discussed in this section. Figure 4 illustrates the 15-4 compressor, which was proposed in [12]. This compressor generates four outputs (O0-O3) from its fifteen inputs (X0-X14). This compressor has two 5-3 compressors in the second stage, a parallel adder in the final stage, and five complete adders in the first stage. Each full adder produces "sum" and "carry" from three major inputs. The 5-3 compressor receives the "sum" of each of the complete adders. Another 5-3 compressor is given the "carry" of all complete adders in a similar manner. To feed the parallel adder are the outputs from the 5-3 compressors. The output is generated by a parallel adder. Instead of employing precise 5-3 compressors in the estimated 15-4 compressor, we used the suggested approximate 5-3 compressors. In the suggested 15-4 compressor, full adders and parallel adders are retained as original adders. The proposed 15-4 compressor has four rough designs. The planned approximate 5-3 compressor's

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prototypes 1, 2, and 3 are employed in the first three designs of the approximately 15-4 compressor. The planned approximate 5-3 compressor is used in designs 1 and 4 of design 4 of the 15-4 compressor. The output "carry" signals are handled by Design 1's approximate 5-3 compressor since they carry greater weight than the output "sum". Additionally, the design 1 compressor has a higher pass rate than the design 4 compressor. Sum signals are handled by a roughly 5-3 compressor in Design 4.

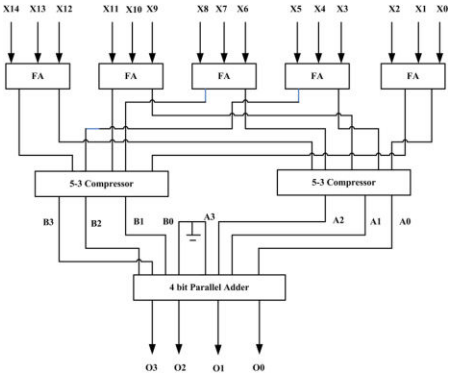

Figure 5: Circuit diagram of 15-4 compressor

C. Prototype of multiplier

The prototype of the 16 x 16 multiplier is described in this section. Utilizing the proposed four 15-4 compressors, four approximative multipliers are created. This is followed by the consideration of four approximative multipliers and oneaccurate multiplier. The proposed approximate 15-4 compressors are used to create approximate multipliers, which are then compared to accurate 16-16 multipliers and other multipliers created using other approximate compressors. Each dot in Figure 5 represents one partial product and depicts the architecture of a 16-bit multiplier utilizing a 15-4 compressor. In the partial product reduction, one multiplier is constructed using six 15-4 compressors, followed by the prototype of four multipliers. Rectangular boxes in the figure denote the multiplier's utilization of the 15-4 and 4-2 compressors. From the 13th column on, 15-4 compressors are employed in the multiplier. There are only thirteen incomplete products in the multiplier's thirteenth column. For that column to utilize the 15-4 compressor, two zeros are added. In a similar vein, the 14th column gains one "0" as well. Other precise compressors, like 4-2 and half-full adders, are utilized for partial product reduction in addition to the 15-4 compressors in the multiplier. In the multiplier's 13th, 14th, and 15th columns, approximatecompressors are employed. The biggest section would have a higher error rate if approximation compressors were used. In multiplier 1, design 1 of the roughly 15-4 compressor is employed. Comparably, multipliers 2, 3, and 4 use designs 2, 3, and 4 of 15-4 approximation compressors. All exact 15-4 compressors are used in an accurate multiplier, as well as accurate 3-2 and 4-2 compressors. The second and third stages of the partial product reduction tree employ precise 4-2 compressors as well as half and full adders. In the final step, the result is computed using parallel adders.

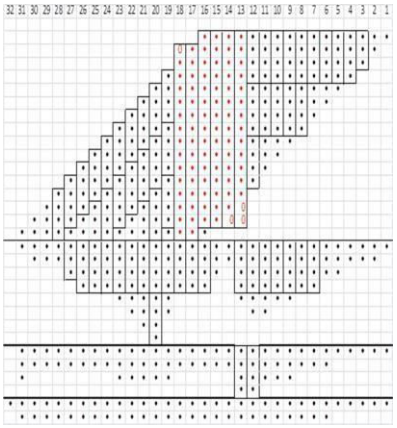

Figure 6: Multiplication Process of 16*16 Multiplier

IV. SIMULATION RESULTS

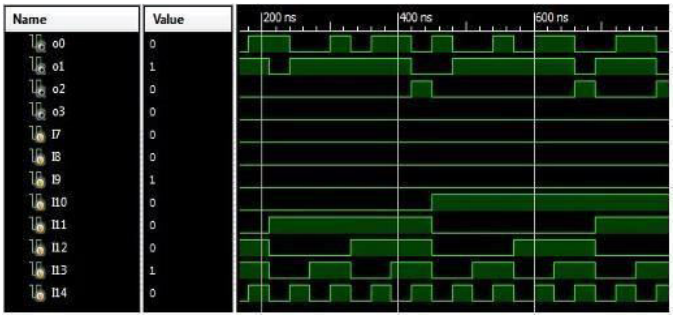

Figure 8: Simulation results of 16*16 multiplier

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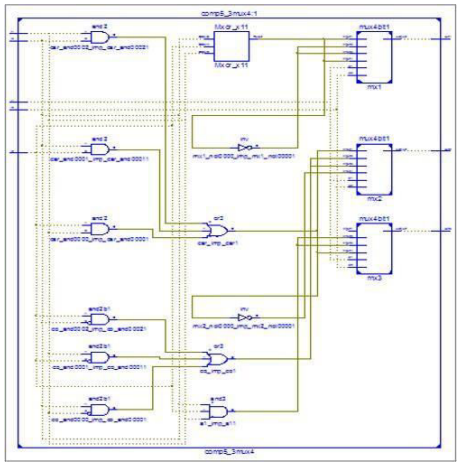

Figure 9: Schematic diagram of 16*16 multiplier

V. APPLICATIONS

This section discusses the use of our multipliers, which were created using approximative compressors. With the proposed multiplier's assistance, image contrast is achieved. To process the image, MATLAB is used. Out of the database, we've picked one color image. Our input image is 512 by 512 pixels in size. The pixels in this picture are RGB. An input image has 512 512 3 pixels, which is 786432 pixels overall. Each pixel has an 8- bit resolution. An integer between 0 and 255 represents each pixel. Our multipliers are sixteen sixteen-bit devices. Each value of a pixel must be transformed into 16 bits. From (0-255) to (0-65535), all input image pixel values are transferred. With the aid of image contrast,

F = (input picture) 65535

Contrast Image = (1 − cos(F) ÷ 2

VI. CONCLUSION

The four compressor prototypes for approximately 15-4 are presented in this study. These suggested 15-4 compressors are used to construct around 16 16-bit multipliers. With a compromise in error rate, approximate multipliers perform better than accurate multipliers. Additionally, we have a high pass rate and a very low normalized error distance value for multipliers created with the suggested 15-4 compressor. When compared to accurate multipliers, the proposed multiplier almost has the same latency.The prospective multiplier was used to perform picture contrast in order to validate our work. The quality of the processed image demonstrates the effectiveness of the multipliers we suggested. Other approximate multipliers' PSNR values are less than 10 dB; however, our prospective multiplier offers more than 30 dB, which is adequate for the majority of image processing applications. The suggested multipliers (3) through (6) are appropriate for applications involvingimage processing, whereas multipliers (7)through (9) can be employed in cases where circuit performance is complex. Depending on their uses, researchers can select the multipliers. Finally, compared to existing approximation multipliers, oursuggested multipliers have a littleoverhead and are capable of producing good results in terms of pass rate and error distance. In the future, researchers canseek to reduce the approximation multipliers' area and pass rate.

VII. FUTURE SCOPE

our proposed multipliers consume low power and capable of giving the good result in terms of pass rate and error distance with the slight overhead of area as compared to other approximate multipliers. In future, researchers can work towards minimizing the area and pass rate of approximate multipliers

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