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Paper Authors

K.THEJESWI, MRS.B.SHOBA RANI
chaitanya Institute of Technology and Science

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ACHIEVEING REDUCED AREA BY MULTI-BIT FLIP FLOP DESIGN

K.THEJESWI, MRS.B.SHOBA RANI
[1]Student, chaitanya Institute of Technology and Science
[2]Associate Professor, chaitanya Institute of Technology and Science

Abstract: Timing Optimization is one of the most important objectives of the designer in the Modern VLSI world. Memory elements play a vital role on Digital World. The basic memory elements of designer considerations are Latch and flip flop. In this paper, we analyze the design of Single-bit Flipflop (SBFF) and made performance comparison over the Multi-bit Flip-flop (MBFF). For improving Flip flop performance one of the promising way is to merge the clock pulse. The Multi-bit Flip-flop is designed by single clock pulse and achieves same functionality like two single-bit Flip-flop. A shift register is designed using both Single-Bit Flip-Flop (SBFF) and Multi-Bit Flip-Flop (MBFF). This paper analyzes the timing performance of both SBFF and MBFF in Xilinx Virtex-5 family (XC5VLX50). These results in favor of Multi-Bit Flip-Flop as reduction of Clock network such as clock buffer and gate delay.

Keyword: Flip-flop, Latch, Clock buffer, Clock network, Gate delay, Single bit flip flop, Multi bit flip flop

I. Introduction

Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed).Area optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partition, Floor planning, Placement, and routing are perform in back-end of the design which is done by CAD tool .The CAD tool have a specific algorithm for each process to produce an area efficient design similar to Power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency, and switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors. Timing optimization refers to meeting the user constraints in efficient manner without any violation otherwise, improving performance of the design. High performance designs are achieved by proper placement, routing and sizing the element. The word optimization is approached in different ways by merging, instead of sizing the memory element. Some of the basic ideas of timing optimization approach are (a) Circuit re- synthesis (b) gate resizing and (c) Circuit reposition as discussed in paper [1]. In this paper timing optimizations are discussed as making the

optimized memory element which suits for high performance application. The memory element requires more time than the logic gates. Moreover the number of memory elements used in the design has also been increased and are proved in present application such as audio and video decoder.

II. Related Work

The idea of designing the multi-bit flipflop arises for power considerations and placement rout-ability effectiveness. Some of them are discussed here: Minimization of dynamic clock power leads the way to merge the single-bit flipflops and constructed Multi-Bit Flip-Flops. This merging process also has to satisfy the certain area constraint which decreases the total flip-flop area in synchronous design as given in paper [2]. In paper [3], it discusses the clock power by congested constraints of unallocated bins and the length of constraints of the input and output signals of all the 1-bit flip-flop. Here redundant inverters in merging of single-bit flip-flop are eliminated. The multi-bit flip-flops are mostly viewed as low power design technique, MBFFs with larger bit numbers as possible to gain more clock power saving but larger bit number may lead to severe crosstalk's due to close interconnecting wires as in paper [4]. To address this problem step by step procedure those are creating crosstalk model of MBFF, next coupling Capacitance Generation from these derive Flip-Flop and Intersection Graph [5] are considered. A clustering and Placement is done by reducing the interconnect wire length. Merging of Flip-Flop is done through library that perform a coordinate transformation to identify those flip-flops that can be merged and their legal regions. This approach reduces the wire length considerably [6]. The Digital design uses the single-bit Flip Flop for memory applications and controller design. D flipflops are implemented in two ways which are Master-Slave latch pair and pulse-triggered latches. Most of the design involving standard cell follows Master-Slave approach because of the restricted timing constraints of pulse triggered latches. In master-slave approach, two latches are connected in serial manner with complementary clock signal [8].

III. Proposed system

This proposed method is based on paper [6] which gives the idea of merging clock pulse. The working of single-bit D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low) and delays it by one clock cycle. That's why, it is commonly known as delay flips flop. The D Flip-Flop can be interpreted as a delay line or zero order hold. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. From the timing diagram in fig 1 it is clear that the output Q changes only at the positive edge [9]. At each positive edge the output Q becomes equal to the input D at that instant and this value of Q is held until the next positive edge.

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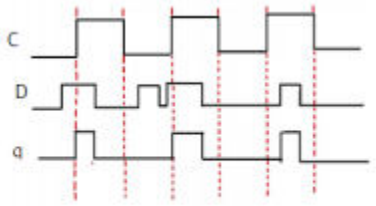

Fig 1: Timing diagram for SBFF

Multi-bit Flip Flop which takes multiple data input and results in multiple data output. The working of multi-bit flip flop is same as single-bit flip flop, whenever the clock gets active state flip flop latches all input to output. For inactive state the flip flop holds the data. The basic structure of multi-bit flip flop is given in fig 2 and its corresponding waveform is given in fig 3.

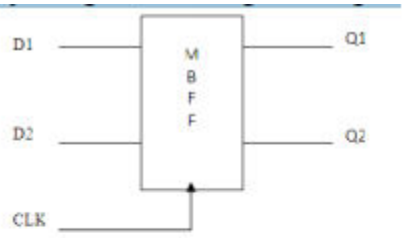

Fig 2: MBFF

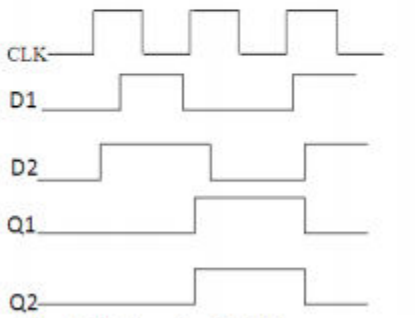

Fig 3: Timing for MBFF

This paper experimented the proposed technique by designing the Serial-In Serial-Out using SBFF and MBFF separately. Designing of SISO has two reasons:- SISO is basic sequential device and easy to analyze. Another one is pipelining, SISO of n-bit register is nothing n-stage pipeline worked for many application such as Serial Bit Communication [7]. We analyze both existing and proposed design using basic sequential circuit of SISO. For existing system, Serial in serial out circuits are constructed by SBFF and MBFF which shown in fig 4 and fig 5. The operation described as arrival of a clock pulse, data at the D input of each flip-flop is transferred to its Q output. At the star, the contents of the register can be set to zero by means of the CLEAR line. If a 1 is to the input of the first flip flop. Then upon the arrival of the fist clock pulse, this 1 is transferred to the output of flip-flop 1. After four clock pulses this 1will be at the output of flip-flop 4. In this manner, a four bit number can be stored in the register. After four more clock pulses, this data will be shifted out of the register.

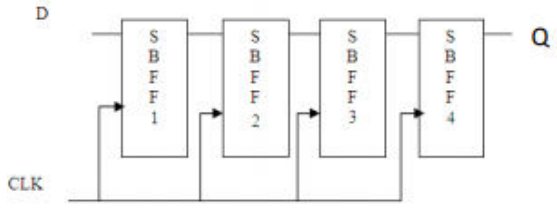

Fig 4: SISO using SBFF

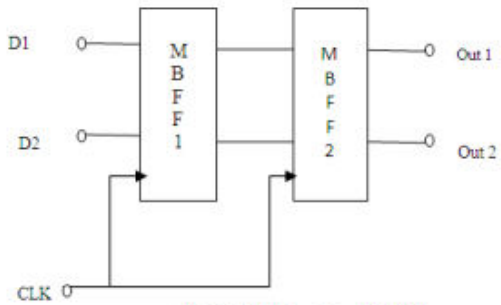

Fig 5: SISO using MBFF

SISO has five major I/O ports CLOCK, two data port as DATA 1 and DATA 2 respectively, and two output port as OUTPUT 1 and OUTPUT 2.In the proposed

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system the bits to store the multi-bit flip flop is doubled with existing single bit Flip flop. MBFFs have advantage over SBFF as smaller design area, controllable clock, less delay on clock network and efficient utilization of routing resources. Power analyze are already made in MBFF [5].

V. Experimental Results

The analysis of SISO designed using MBFF is targeted and verified on Xilinx FPGA of family virtex-5 (XC5VLX50 – FF676 package). The experimental results are tabulated which shown below. In the table, Roman literals I represents SISO using SBFF and II represents SISO using MBFF. TABLE 1 summary the report of our proposed techniques and same compared with existing SBFF. Table 2 gives experimental results of various size of shift register. The constraints taken to considerations are number of flip-flops used, clock buffer count and period analysis as Gate delay and net delay. The number of flip-flops in SISO using SBFF is about half a number in SISO using MBFF. The strategies are to minimizing the clock network having been done using proposed technique by means of reducing the clock drivers.

	Existing system (SBFF)	Proposed system (MBFF)
LUT with REG	32	23
Logic Control	0	2
Memory	0	2
SRL	0	2
Drive strength	12	24

Table 1 Logic Utilization Comparison of SBFF and MBFF

Our proposed technique reduces the designer's difficulty for analyzing all the flipflops for meeting the timing requirements. MBFF, bypass two bit of same timing constraints so that much of the timing path which repeated to the single MBFF reduces calculation. Some of the default parameter of FPGA such as default offset after out for clock , default period analysis are most probably fixed and those are not have much variation. Fig 6shows the graphical representation for comparing flip-flop counts on SISO between existing and proposed techniques. The first bar represents the flip-flop count of SISO using existing techniques and the second bar represents the flip-flop count of SISO using proposed techniques.

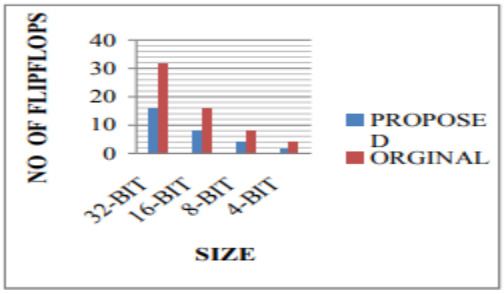

Fig .6 .Flip flop count

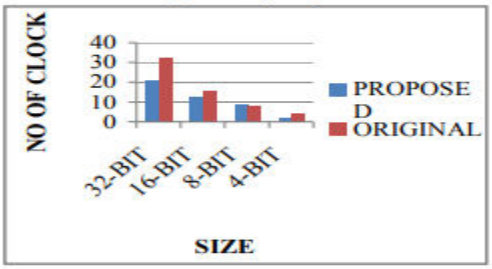

Fig 7: Clock buffer

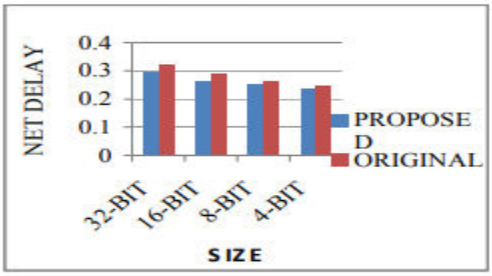

Fig 8: Results for net delay

Fig 7 and fig 8 shows that our proposed techniques reduced clock network and net delay. The size of clock network is auxiliary parameter for low power designs, without making any variation on timing parameter. If clock networks get minimized the power dissipation of High speed designs more efficient than previous, this make the design more reliable.

V.Conclusion

In present VLSI design area is one of the important issues to be addressed. To achieve reduced area various types of flip flops and shift register are discussed. Single bit flip flop and Multi bit flip flop are implemented to achieve less usage of area. Various size of shift register is implemented with Multi bit flip flop. This proposed method is implemented in Xilinx Virtex 5 FPGA family. Experimental results are targeted to number of flip flop usage, delay and clock buffer. Flip flop area usage is minimized approximately to 50%. Thus this proposed method is more suitable for reduction of hardware.

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