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VLSI DESIGN FOR CONVOLUTIVE BLIND SOURCE SEPARATION ¹B VINOD KUMAR, ²V ANITHA, ³B HARI KUMAR, ⁴BOLLU VINAY ¹²³ASSISTANCT PROFESSOR, BRILLIANT INSTITUTE OF ENGINEERING & TECHNOLOGY, ABDULLAPURMET(V&M) RANGA REDDY DIST-501505 ⁴UG SCHOLAR, DEPARTMENT OF CSE, BRILLIANT INSTITUTE OF ENGINEERING & TECHNOLOGY, ABDULLAPURMET(V&M) RANGA REDDY DIST-501505

ABSTRACT:

Blind source separation (BSS) is a crucial method in signal processing widely used across various fields, including imaging, audio, and biological signals. Among its challenges, convolutive BSS stands out, as it deals with separating mixed sources where the mixing is defined by convolution. This project introduces an innovative VLSI (Very Large Scale Integration) design tailored for convolutive blind source separation, targeting the needs for real-time, efficient processing in applications like echo cancellation, audio source separation, and speech enhancement.

The proposed VLSI architecture leverages cutting-edge algorithms and hardware advancements to deliver high-precision convolutive BSS with minimal latency. It features multiple processing elements, each tasked with isolating and separating distinct source signals from the observed mixture. These elements employ advanced signal processing techniques and adaptive filtering methods to iteratively enhance source estimations, boosting separation success even amidst fluctuating mixture conditions.

Key aspects of the VLSI design encompass parallel processing units, adaptive parameter tuning, and memory-efficient data structures, making it versatile for various real-world scenarios. The architecture adeptly handles different input volumes and adjusts to diverse computational requirements. Experimental results validate the effectiveness and efficiency of this VLSI framework in convolutive BSS environments, showcasing its ability for real-time separation of mixed sources while maintaining superior signal quality. Thanks to its scalability and robustness, this hardware design serves as a powerful asset for signal processing systems that aim to extract meaningful source information from intricate mixes.

Keywords: BSS, VLSI, memory, and high efficiency.

I. INTRODUCTION

Blind source separation (BSS) is a crucial technique in signal processing that finds its use across various domains, including audio processing, telecommunications, and biomedical engineering. Essentially, BSS tackles the challenge of separating mixed signals when the exact mixing process is unknown. A more complex branch of BSS is convolutive blind source separation, which deals with sources mixed via convolution. This approach mirrors real-world situations, such as environments with multiple sound sources and reflections. Convolutive BSS is particularly relevant in areas like speech enhancement, audio source separation, and acoustic echo cancellation. However, it comes with distinct hurdles due to the dynamic nature of the mixing process. This variability necessitates the use of advanced algorithms and robust hardware solutions for effective real-time signal separation.

This paper aims to tackle the challenges related to convolutive BSS by introducing a specialized Very Large Scale Integration (VLSI) architecture. VLSI technology is key to



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performing intricate signal processing tasks efficiently, making it an excellent choice for systems requiring both precision and real-time processing capabilities. Our focus is on presenting an innovative VLSI design specifically crafted for convolutive BSS scenarios.

This design includes advanced signal processing algorithms, parallel processing components, memory-efficient data structures, and adaptive parameter tuning, all aimed at enhancing the separation of mixed signals. By integrating these elements, we aim to facilitate real-time source separation from convoluted mixtures, addressing the growing need for high-performance BSS solutions in various applications. In the following sections, we will explore the architecture, algorithmic methods, and experimental findings of our VLSI design for convolutive blind source separation. By the conclusion of this paper, readers will have a thorough insight into the capabilities and potential benefits of this VLSI solution in improving signal processing systems, particularly in scenarios where convolution-based mixing is involved.

Blind source separation is a filtering technique aimed at disentangling different sources from mixed signals, often with limited knowledge about the sources and the mixtures themselves. This lack of information makes the task quite complex. Nonetheless, blind source separation has become a crucial research area across various fields, including audio signal processing, biomedical signal processing, communication systems, and image processing. The simplest mixing process involves instantaneous mixing without any filtering effects. For audio sources that travel through a filtering environment before reaching microphones, a convolutive mixing process occurs. To retrieve the original audio source, convolutive blind source separation must be applied. One commonly used approach for addressing the convolutive blind source separation problem is Independent Component Analysis (ICA). However, a significant drawback of implementing this technique in software is its high computational demands, which can be time-consuming. This has led to increased interest in hardware solutions for ICA-based blind source separation, as these can achieve optimal parallel processing. An analog BSS chip can be developed using above- and sub-threshold CMOS circuit techniques, integrating an input/output interface with analog weight coefficients and adaptation blocks.

II. LITERATURE SURVEY

Maximizing the autocorrelation of brain imaging signals plays a crucial role in blind source separation (BSS). One of the prominent techniques in BSS, known as canonical correlation analysis (CCA), is widely utilized for analyzing optical imaging (OI) and functional magnetic resonance imaging (fMRI) data. However, CCA often encounters challenges when it comes to separating temporal signal sources due to the necessity of reducing dimensionality and overlooking spatial autocorrelation. To address these challenges, a new approach called "straightforward image projection" (SIP) has been integrated into temporal BSS. This innovative method, termed low-dimensional canonical correlation analysis (LD-CCA), leverages the spatial and temporal autocorrelations of the signals of interest. By incorporating both spatial and temporal information, we present a technique known as "generalized timecourse," where data is reorganized prior to separation. This allows for a clearer definition of the combined spatial and temporal autocorrelations.

LD-CCA maximizes these autocorrelations, enabling the extraction of the expected "real" signal sources. The generalized timecourses are designed to be low-dimensional, thereby



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eliminating the need for dimensionality reduction and minimizing the risk of losing valuable information. We have compared LD-CCA with temporal CCA and temporal independent component analysis (tICA), and results from simulated data indicate that LD-CCA is more effective in recovering signal sources. Additionally, tests using real intrinsic OI and fMRI data further validate LD-CCA's effectiveness. Furthermore, to tackle the high computational costs associated with traditional batch BSS algorithms, we propose an online BSS approach. Current online methods primarily focus on separating independent or uncorrelated sources, paving the way for more practical applications in this field.

Recently, nonnegative matrix factorization (NMF) has emerged as a promising technique for separating correlated sources. To address the challenge of non-uniqueness in factorization, various constraints are often applied. In this paper, we introduce an incremental NMF method with a volume constraint to tackle online blind source separation (BSS). The volume constraint applied to the mixing matrix improves the identifiability of the sources, while the incremental learning approach significantly lowers computational expenses. By utilizing a natural gradient-based multiplication updating rule, our method excels particularly in recovering dependent sources.

We conducted simulations across diverse applications, including dual-energy X-ray images, online encrypted speech signals, and highly correlated face images, all of which demonstrate the effectiveness of our proposed method. Furthermore, this work presents an efficient very large-scale integration (VLSI) design for convolutive blind source separation (CBSS). We adopted a CBSS separation network based on the Information Maximization (Infomax) approach. Our CBSS chip design primarily comprises Infomax filtering modules and scaling factor computation modules. Within the Infomax filtering module, input samples are processed using an Infomax filter, with weights updated according to Infomax-driven stochastic learning rules. Meanwhile, the scaling factor computation module integrates all operations, including the logistic sigmoid function, into a circuit design utilizing a piecewise linear approximation scheme.

III. PROPOSED SYSTEM

A proposed system for VLSI Design aimed at Convolutive Blind Source Separation would focus on creating a tailored hardware architecture designed to efficiently and accurately isolate mixed sources in real-time. This is particularly relevant in cases where the mixing involves convolution. Below is an outline of the essential components and features that such a system might encompass:

1. Hardware Architecture: The core of the proposed system is a custom-designed VLSI architecture optimized for convolutive blind source separation. This architecture would consist of dedicated hardware modules and processing units tailored to perform the necessary signal processing tasks efficiently.

2. Parallel Processing: To handle the computational demands of convolutive BSS in real-time, the VLSI system would incorporate parallel processing units. These units would enable simultaneous processing of multiple data streams, accelerating the separation process.

3. Adaptive Filtering: Advanced adaptive filtering algorithms would be implemented in hardware to estimate and separate the individual source signals. These algorithms should be capable of adapting to changing mixing conditions, making the system robust in real-world scenarios.



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4. Memory Management: Efficient memory management is essential to store intermediate results and filter coefficients. The system should include memory units optimized for low-latency access to data.

5. Parameter Tuning: The architecture may incorporate adaptive parameter tuning mechanisms that automatically adjust filter coefficients and other parameters based on the characteristics of the input signals and the mixing environment.

6. Real-Time Processing: Real-time performance is crucial for applications like audio source separation and speech enhancement. The proposed system should be capable of processing incoming data streams with low latency.

7. Scalability: The system's architecture should be scalable to accommodate different numbers of sources and adapt to varying computational requirements.

8. Noise Reduction: To enhance the quality of separated signals, noise reduction techniques may be integrated into the system, especially in noisy environments.

9. Evaluation and Testing: The proposed system would undergo extensive testing and evaluation to validate its performance in various scenarios. Metrics such as Signal-to-Noise Ratio (SNR) and Separation Quality Metrics may be used for evaluation.

10. Integration: The VLSI system should be designed for easy integration into larger signal processing systems or devices, such as audio processors, medical equipment, or communication systems.

11. Energy Efficiency: To make the system suitable for portable and battery-powered devices, energy-efficient hardware design should be a consideration.

12. Algorithm Flexibility: While the focus is on convolutive BSS, the system may be designed to accommodate different blind source separation algorithms, offering flexibility for various applications.

The proposed system aims to provide an efficient and versatile solution for convolutive blind source separation, addressing the challenges posed by real-time processing, changing mixing conditions, and the need for high-quality source separation. It has the potential to enhance various applications, including speech enhancement, audio source separation, biomedical signal processing, and more.

IV METHODOLOGY

The proposed CBSS system is shown in the FIG. The CBSS chip mainly consists of two functional cores: Infomax filtering module and scaling factor computation module. Additionally, the Infomax filtering outputs are added with the help of two small carry-save adders (CSAs). The current prototype chip is used for two sources and two sensors by utilizing four Infomax filtering modules along with two scaling factor computation modules.

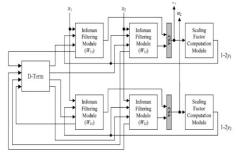


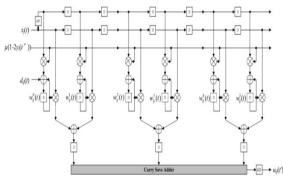
Fig.1. Proposed model.



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The Infomax filtering module for the proposed system is shown in fig.3. In the fig. 1, the CBSS separation network contains four causal FIR filters. These filters are adaptive because stochastic learning rules which are derived from the Infomax approach will alter the tap coefficients and are thus referred to herein as the Infomax adaptive filter or the Infomax filter. The Infomax filtering module is exemplified with six taps. In the Infomax filtering module, an input sample passes through lower and upper register chains. These samples are multiplied with filter weights and scaling factors, respectively. The multiplication results of all of the taps are accumulated by a two-stage summation. The first stage adopts carry lookahead adders to generate the intermediate addition results for multiplication of every two successive taps. The above intermediate addition results are summed up by using a carry save addition scheme. A CSA(carry save adder) can accept more than two data inputs.

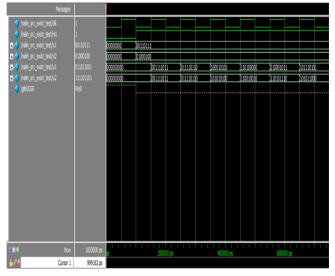


According to our numerical analysis, five line segments are sufficient to approximate with a negligible error. Let lsi, i = 1, 2, ..., 5 denote the ith line segment, and ci represent the connected point between two consecutive line segments. To implement the line-segment approximation, the circuit design for scaling factor computation is to calculate single variable linear equations. For the equation of lsi which corresponding to mi(n) = ai n + bi, i = 1, 2, ..., 5, where n = ui(t). As the slopes of ls1 and ls5 are the same, these two line segments share the equation parameters a1. In the same manner, line segments ls2 and ls4 share the equation parameters a2. Furthermore, according to the symmetry in Fig. 5, the bias used for line segments ls4 and ls2 use biases -b2 and b2, respectively .As for the d0 ij(t), this study designs a Dterm unit to execute dij(t) = cofactor(wij)(detW0) -1. The architecture of the D-term unit is shown in Fig. The Dterm unit consists of a determinant circuit to find.



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CONCLUSION

This expeditious VLSI design process for CBSS has been around for some time. CBSS separation networks are computed using scaling aspect computation modules and a design based on the Info-max filtering system. With a die size of roughly 0.54 mm2 by 0.54 mm2, the suggested ASIC device makes use of TSMC's cutting-edge 90-nm CMOS technology. The optimal operating voltage for a 1.8-V power supply is 100 MHz, which consumes just 54.86 mW of power. The proposed CBSS ASIC chip can be combined with other sound processing chips and ancillary components to construct a complete sound processing system, in addition to being used for reprocessing.

REFERANCES

[1] G. Zhou, Z. Yang, S. Xie, and J. M. Yang, "Online blind source separation using incremental nonnegative matrix factorization with volume constraint," IEEE Trans. Neural Netw., vol. 22, no. 4, pp. 550–560, Apr. 2011.

[2] M. Li, Y. Liu, G. Feng, Z. Zhou, and D. Hu, "OI and fMRI signal separation using both temporal and spatial autocorrelations," IEEE Trans. Biomed. Eng., vol. 57, no. 8, pp. 1917–1926, Aug. 2010.

[3] A. Tonazzini, I. Gerace, and F. Martinelli, "Multichannel blind separation and deconvolution of images for document analysis," IEEE Trans. Image Process., vol. 19, no. 4, pp. 912–925, Apr. 2010.

[4] H. L. N. Thi and C. Jutte, "Blind source separation for convolutive mixtures," Signal Process., vol. 45, no. 2, pp. 209–229, Aug. 1995.

[5] A. J. Bell and T. J. Sejnowski, "Blind separation and blind deconvolution: An informationtheoretic approach," in Proc. Int. Conf. Acoust., Speech, Signal Process., May 1995, vol. 5, pp. 3415–3418.

[6] A. Hyvärinen and E. Oja, "Independent component analysis: Algorithms and applications," Neural Netw., vol. 13, no. 4/5, pp. 411–430, May/Jun. 2000.

[7] M. H. Cohen and A. G. Andreou, "Analog CMOS integration and experimentation with an autoadaptive independent component analyzer," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 42, no. 2, pp. 65–77, Feb. 1995.



PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL

www.ijiemr.org

[8] K. S. Cho and S. Y. Lee, "Implementation of InfoMax ICA algorithm with analog CMOS circuits," in Proc. Int. Workshop Independent Compon. Anal. Blind Signal Separation, Dec. 2001, pp. 70–73.

[9] Z. Li and Q. Lin, "FPGA implementation of Infomax BSS algorithm with fixed-point number representation," in Proc. Int. Conf. Neural Netw. Brain, 2005, vol. 2, pp. 889–892.

[10] H. Du and H. Qi, "An FPGA implementation of parallel ICA for dimensionality reduction in hyperspectral images," in Proc. IEEE Int. Geosci. Remote Sens.Symp., Sep. 2004, pp. 3257– 3260.

[11] M. Ounas, R. Touhami, and M. C. E. Yagoub, "Low cost architecture of digital circuit for FPGA implementation based ICA training algorithm of blind signal separation," in Proc. Int. Symp. Signals, Syst. Electron., 2007, pp. 135–138.

[12] K. K. Shyu, M. H. Lee, Y. T. Wu, and P. L. Lee, "Implementation of pipelined FastICA on FPGA for real-time blind source separation," IEEE Trans. Neural Netw., vol. 19, no. 6, pp. 958–970, Jun. 2008.