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Design of Low Power Voltage Level Shifter for IoT Applications

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Abstract-- Contemporary System-on-Chip (SoC) designs encompass various integrated blocks operating at distinct supply voltage levels, necessitating the use of signal voltage level conversion for their interconnection. Voltage level shifters (LS) are employed to transform low logic levels, including those existing in the sub-threshold voltage range, into higher voltage levels suitable for subsequent blocks. Given the potential requirement for a multitude of level shifters within a system, the design must emphasize power efficiency, signal propagation speed, and efficient utilization of silicon real estate. Consequently, this thesis introduces a low-power voltage level shifter designed to adeptly convert extremely low input voltages, specifically those within the deep sub-threshold region (approximately 100 mV), into the standard supply voltage level (1.2 V).

The provided circuit effectively drives the split-input inverting buffer, which functions as the output stage. It accomplishes this by employing a self-biased cascode current mirror featuring diode-connected PMOS and NMOS transistors, leading to highly efficient energy usage. Moreover, to achieve superior power efficiency, the suggested circuit makes use of a multi-threshold method. The level shifter architecture implemented in this thesis effectively addresses the common contention problem often encountered in traditional voltage level shifters.

When utilizing gpdk 45nm CMOS technology, the proposed circuit can convert a 0.4 V input pulse with a frequency of 100 kHz to 1.2 V. This conversion is achieved with an average switching delay of 40 ns and an average power consumption of just 98.87 picoWatts.

I. Introduction

Cutting-edge System-on-Chip (SoC) designs incorporate a multitude of diverse intellectual property (IP) blocks, each functioning at varying supply voltage levels, contingent upon their specific timing requirements [1]. Blocks with time-sensitive tasks operate at elevated supply voltages (VDDH) to attain the desired performance levels, while less critical blocks operate at lower supply voltages (VDDL), even entering the sub-threshold region, in order to conserve energy. In these multi-VDD systems, dependable level shifter circuits are imperative for enabling seamless communication between distinct voltage domains while upholding the overall robustness and reliability of the design

In the realm of prior art, level shifters can be classified into two main categories: cross-coupled (CC) and current mirror (CM) based topologies. CC-based level shifters excel in minimizing standby power consumption due to the presence of complementary pull-up networks (PUNs) and pull-down networks (PDNs). However, they come with a drawback of encountering current contention issues between the PUNs and PDNs during switching, which negatively impacts both speed and energy efficiency. This problem becomes more pronounced when dealing with the up-conversion of sub-threshold voltages, necessitating impractical increases in the size of the PDNs.

Conversely, CM-based architectures mitigate the contention between PUNs and PDNs, resulting in improved speed and energy efficiency, especially when performing

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wide-range up-conversions (such as transitioning from the deep sub-threshold regime to significantly higher voltage levels). Nevertheless, CM-based designs tend to suffer from higher static power consumption, which can be a trade-off to consider.

Recent literature has introduced various solutions to address the limitations of both CC-based and CM-based level shifter topologies. These solutions aim to enhance switching speed, energy efficiency, and robustness. Here are some examples of these proposed solutions:

Adaptive/Regulated PUNs: In [4] and [5], adaptive or regulated PUNs are suggested for CC-based designs. These modifications reduce current contention, improving switching speed and energy efficiency, especially for up-conversions from extremely low-voltage domains. Additionally, a split-input inverting buffer is incorporated as the output stage to further enhance energy efficiency.Revised Wilson CM: In [8], a revised Wilson CM architecture is proposed to overcome voltage drop and non-optimal feedback limitations in conventional CM-based level shifters. This approach leverages mixed-threshold voltage (VTH) devices to achieve better performance.Reduced-Swing Output Buffer: [9] introduces a reduced-swing output buffer design, which lowers standby power consumption. A pass transistor-based circuitry is also used to improve switching speed.Self-Controlled Current Limiter: [10] explores a self-controlled current limiter scheme for voltage shifting from deep sub-threshold to above-threshold domains. This scheme enhances delay, energy efficiency, and reduces static power consumption.Split-Input Inverting Buffer: The use of a split-input inverting buffer is adopted in CM-based topologies as well, as seen in [11] and [12]. This reduces static current in the output stage.

In this brief, an ultra-low voltage level shifter is introduced based on a self-biased low-voltage cascode CM scheme and a split-input inverting output buffer. This novel CM topology is validated through silicon measurements, marking the first such proposal for a level shifter design. The driving scheme of the split-input inverting output buffer incorporates an additional diode-connected NMOS device and a PDN boosting device to achieve high energy efficiency and fast switching and it also uses the mixed-threshold voltage (VTH) devices to achieve better performance and lower power consumption.

The proposed circuit was designed using 45-nm CMOS technology.The results demonstrate the robustness of the design for extremely low-voltage inputs (ranging from 100 mV up to the nominal voltage of 1.2 V). For instance, for a 0.4-V 100-kHz input pulse, the circuit exhibited an average delay of 40 ns and an average power consumption of 98.87 pW.

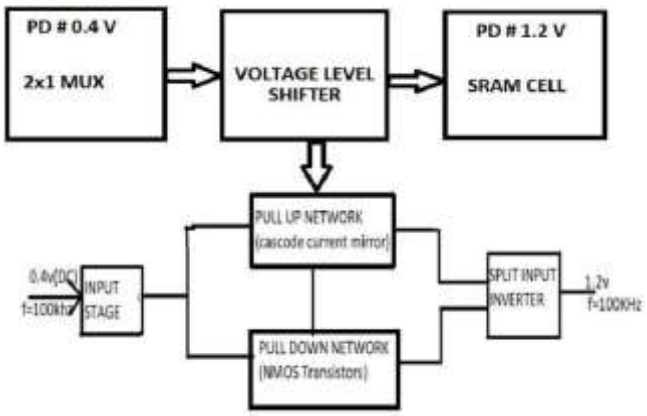

Figure 1 Block Diagram of Proposed Level Shifter

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The rest of this brief is structured as follows,Section II: This section provides a detailed description of the proposed level shifter, explaining its architecture, key components, and design principles.Section III: Here, you will find the simulation results of the proposed level shifter. The section discusses the performance and characteristics observed during simulations.Section IV: This part presents a comparison of the proposed level shifter against state-of-the-art designs. It evaluates how the new design stacks up in terms of various criteria and discusses any advantages or disadvantages.Section V: In the concluding section, the brief summarizes the key findings and conclusions drawn from the research on the ultra-low voltage level shifter.

II. Proposed Design

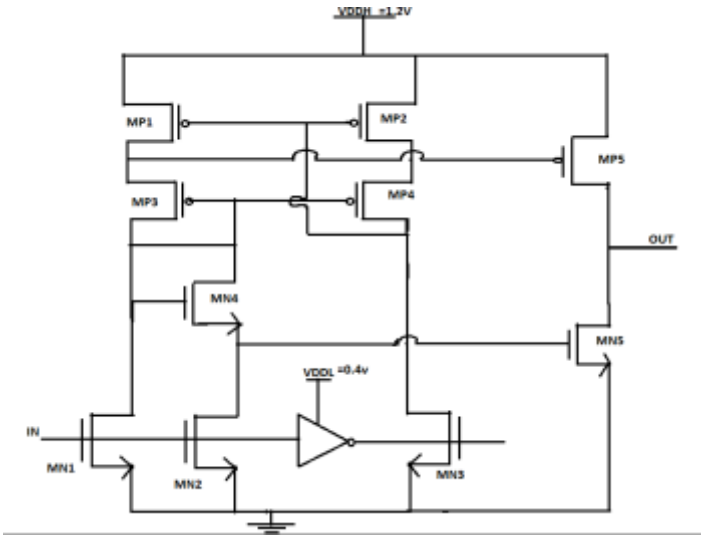

Figure 2:- Schematic of Proposed Level Shifter

As depicted in Figure 2, our proposed level shifter is primarily built around a PMOS-based self-biased low-voltage cascode CM (Complementary Metal-Oxide-Semiconductor) design, consisting of transistors Mp1 to Mp4. Mp1 is bias-controlled through the use of a diode-connected Mp3, following a strategy employed in similar solutions found in prior research [4], [5], [11], [12]. Additionally, our circuit takes advantage of a split-input inverting buffer (comprising transistors Mn5 to Mp5) as the output stage, a technique commonly used to reduce power consumption.

However, there's a notable distinction in the driving scheme of our output stage compared to previous designs. We incorporate an extra diode-connected NMOS device, denoted as Mn4, in addition to a PDN (Pull-Down Network) boosting device, known as Mn2. Consequently, the output buffer in our design is driven by two distinct nodes, NDP and NDN, each having voltage values that differ from the voltage drop (VD) across Mp3 and Mn4 (VD = |VGSp3|+VGSn4). This voltage difference is more pronounced than what's typically found in previous designs utilizing a split-input inverting output buffer.

The significance of this difference becomes apparent in Figs. 2(a)–(f), which portray the transient behavior of our proposed level shifter in the context of voltage up-

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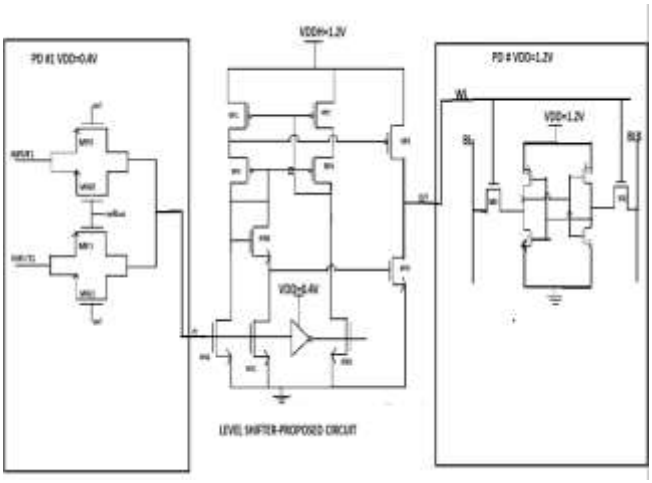
conversion. Specifically, it showcases the transformation of an input pulse amplitude from 200 mV to 1.8 V for both output transitions. Notably, in Fig. 2(c) and (d), one can observe that during the transition from low to high (L → H) or high to low (H → L), the NDN (NDP) node effectively disables the NMOS (PMOS) components of the output stage well before their complementary devices begin to weakly activate. This strategic approach helps alleviate contention at the output node and results in reduced short-circuit power consumption. This is particularly advantageous for voltage up-conversion from the sub-threshold regime, contributing to enhanced energy efficiency.As illustrated in Figure 2, when the input signal A (or its complement AN) is in a low (high) state, the transistors Mn1 and Mn2 are in the OFF state, while Mn3 remains ON. Consequently, the voltage at node NP is at a low level (0 V), while the voltage at the NDP node is high (VDDH) because Mp1 is in the ON state. Simultaneously, the voltage at the NN and NDN nodes is VDDH−|VGSp3| and VDDH−|VGSp3|−VGSn4, respectively.

During the transition from low to high (L → H) of the input signal A, Mn1 and Mn2 are turned ON, while Mn3 switches OFF. This action initiates the discharge of the NN and NDN nodes. As the voltage at node NN rises, it turns on Mp4, allowing current IR to flow in the right branch, charging node NP. Consequently, Mp1's strength is reduced, alleviating the current contention at the NDP node. This enables the NDP node to discharge, switching on Mp5, while the NN and NDN nodes are fully discharged to 0 V, completely turning off Mn5. Figure 2 also depicts the signals of the proposed level shifter during the high-to-low (H → L) input transition.



When signal A (or AN) transitions from high to low (H → L), Mn1 and Mn2 are turned OFF, while Mn3 is turned ON to pull down node NP. The discharging current IR is mirrored as IL on the left branch, charging nodes NDP and NDN to voltage levels of VDDH and VDDH − |VGSp3| − VGSn4, respectively. As a result, MP5 is completely turned OFF, while MN5 is turned ON to discharge the output node.

The proposed level shifter was meticulously designed using a commercial 1.8-V 180-nm CMOS technology, with sizing details provided in Table I. A dual-threshold voltage (VTH) design approach was employed, utilizing low VTH (LVT) devices for Mn1–Mn3 and regular VTH (RVT) devices for the remaining transistors. This strategy was adopted to enhance switching characteristics while ensuring a compact footprint and robustness at the lower supply voltage domain (VDDL) through appropriate transistor sizing. It's noteworthy that the voltage conversion range of this

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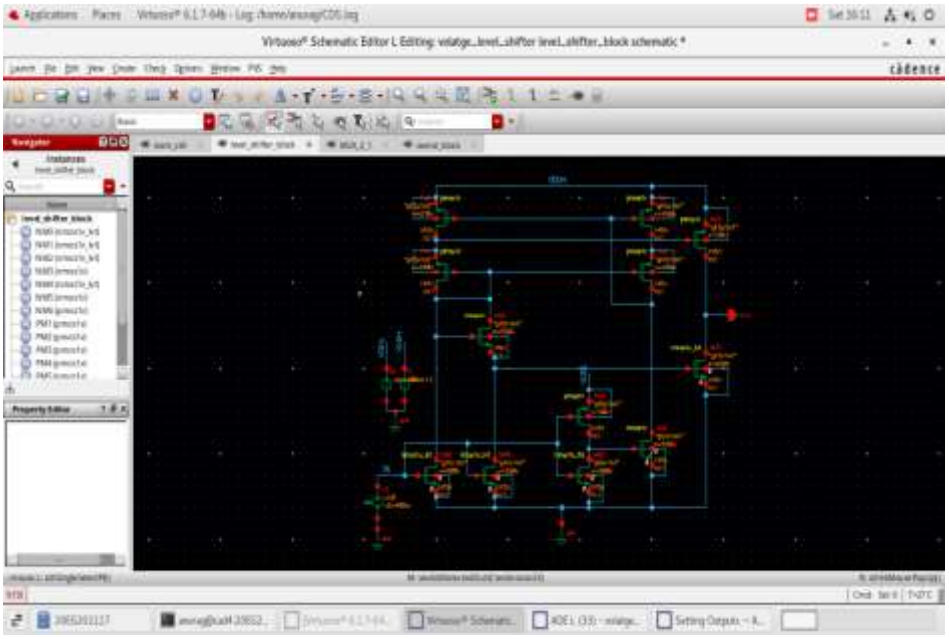
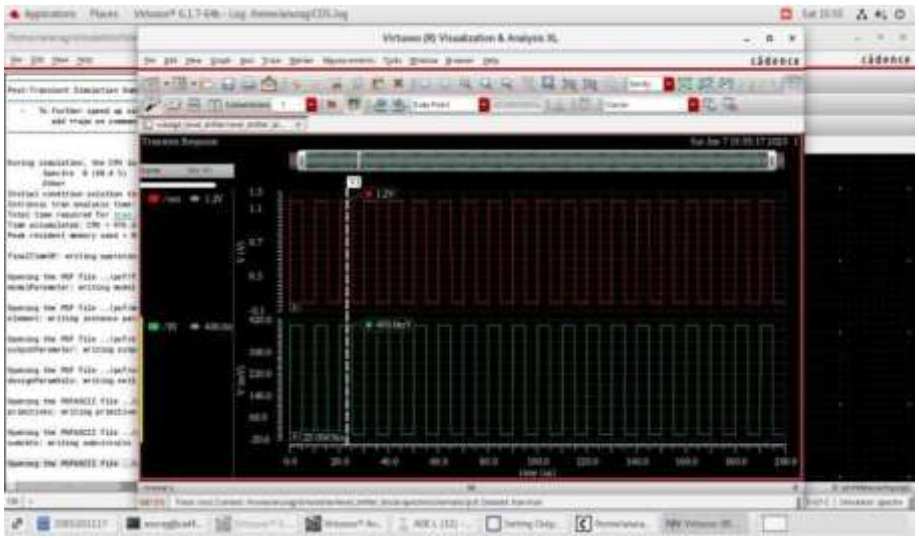
level shifter can be further extended upward by incorporating thicker-oxide (e.g., 3.3-V) I/O PMOS devices, as demonstrated in [8]

III. **Results and comparison**



The designed level shifter was created using a standard 1.2-V 45-nm CMOS technology, and it was sized according to the specified requirements. To optimize its switching performance while maintaining a compact size and ensuring robustness at the lower supply voltage domain (VDDL), a dual-threshold voltage (VTH) design approach was employed. Specifically, low VTH (LVT) devices were utilized for Mn1–Mn3 transistors, whereas regular VTH (RVT) devices were used for the remaining transistors. This approach allowed for improved switching characteristics while also optimizing transistor sizing to ensure the circuit's suitability for the VDDL domain.



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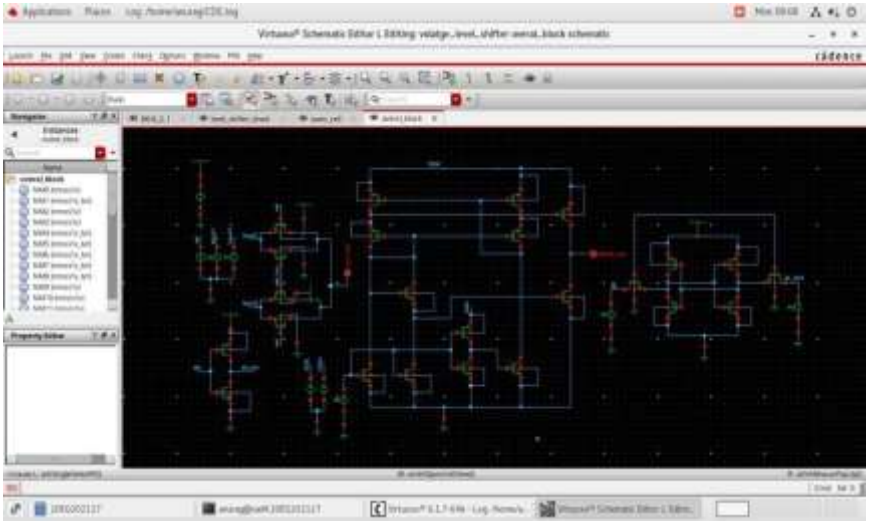

In the depicted schematic, a predicament arises when integrating a multiplexer (MUX) functioning at a lower supply voltage with an SRAM cell operating at a higher supply voltage. The issue stems from a voltage disparity: specifically, the output signals emitted by the MUX may lack the requisite voltage amplitude to robustly propel the inputs of the SRAM cell. This predicament arises due to the inherent limitation imposed on the MUX's output signal levels by the lower supply voltage. Furthermore, the threshold voltage of the transistors within the MUX, which operates under the constraint of a lower supply voltage, may not suffice to deliver the requisite driving force for the inputs of the SRAM cell functioning at an elevated supply voltage. Consequently, this circumstance can engender quandaries related to signal fidelity and temporal margins.

To redress this quandary, a bespoke level shifter circuit was meticulously contrived to effectuate the transformation of voltage levels between these two discrete domains. The design of this level shifter circuit was meticulously conceived, employing multi-threshold voltage (multi-Vt) transistors as a means to not only curtail power consumption but also augment the overall efficiency of the circuit. With the level shifter circuit duly deployed, the MUX is empowered to generate output signals conforming to the higher supply voltage requisites stipulated by the SRAM cell. In essence, this level shifter functions as an intermediary, ensuring dependable communication and harmonization between the MUX and the SRAM cell.

To encapsulate, when confronted with the conundrum of interfacing a MUX operating at a lower supply voltage with an SRAM cell functioning at a higher supply voltage, a voltage disparity issue emerges, posing potential challenges to signal integrity and temporal margins. The solution takes the form of an intricately engineered level shifter circuit, incorporating multi-threshold voltage transistors, which serves to bridge the voltage chasm between these two domains and thus enable steadfast communication between the two circuit components.

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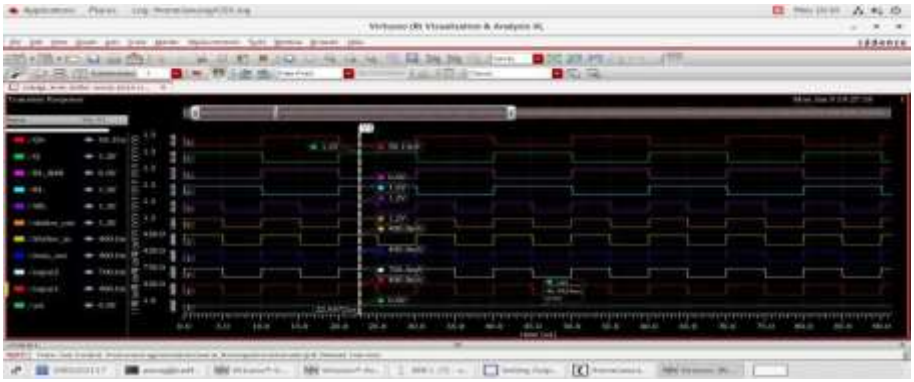

Comparison

PARAMETER	Multi-Vt Technique	Regular-Vt Technique
TECHNOLOGY	45nm	45nm
CONVERSION RANGE	0.4v-1.2v	0.8v-1.2v
POWER CONSUMPTION	98.7pw	295.027nw

IV. Conclusion

In summary, the utilization of a low-power level shifter with a multi-threshold voltage (multi-VT) technique proves to be a highly effective approach for reducing power consumption in Internet of Things (IoT) applications. By incorporating multiple threshold voltage options for transistors within the level shifter, it becomes possible to optimize power usage without compromising circuit speed and overall performance. This technique not only contributes to lower power consumption but also facilitates the design of IoT devices that are both energy-efficient and high-performing. Such devices can operate for extended periods without the need for frequent battery replacements or recharging, making them highly practical and sustainable solutions. Consequently, the low-power level shifter with a multi-VT technique plays a crucial role in advancing the development of power-efficient IoT devices, which are essential for a wide range of applications across various industries.

REFERENCES

1. Kabirpour, Saeideh, and Mohsen Jalali. "A low-power and high-speed voltage level shifter based on a regulated cross-coupled pull-up network." IEEE Transactions on Circuits and Systems II: Express Briefs 66, no. 6 (2018): 909-913.

2. Lanuzza, Marco, Felice Crupi, Sandro Rao, Raffaele De Rose, Sebastiano Strangio, and Giuseppe Iannaccone. "An ultralow-voltage energy-efficient level shifter." IEEE Transactions on Circuits and Systems II: Express Briefs 64, no. 1 (2016): 61-65.

3. Yong, Zhenqiang, Xiaoyan Xiang, Chen Chen, and Jianyi Meng. "An energy-efficient and wide-range voltage level shifter with dual current mirror." IEEE transactions on very large scale integration (VLSI) systems 25, no. 12 (2017)

4. R. Saleh et al., "System-on-chip: Reuse and integration," Proc. IEEE, vol. 94, no. 6, pp. 1050–1069, Jun. 2006.

5. [2] M. Lanuzza, P. Corsonello, and S. Perri, "Fast and wide range voltage conversion in multisupply voltage designs," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 2, pp. 388–391, Feb. 2015.

6. W. Zhao, A. B. Alvarez, and Y. Ha, "A 65-nm 25.1-ns 30.7-fJ robust subthreshold level shifter with wide conversion range," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 62, no. 7, pp. 671–675, Jul. 2015.

7. M. Lanuzza, F. Crupi, S. Rao, R. De Rose, S. Strangio, and G. Iannaccone, "An ultralow-voltage energy-efficient level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 64, no. 1, pp. 61–65, Jan. 2017.

8. S. Kabirpour and M. Jalali, "A low-power and high-speed voltage level shifter based on a regulated cross-coupled pull-up network," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 66, no. 6, pp. 909–913, Jun. 2019.

9. E. Låte, T. Ytterdal, and S. Aunet, "An energy efficient level shifter capable of logic conversion from sub-15 mV to 1.2 V," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 11, pp. 2687–2691, Nov. 2020.

10. R. Matsuzuka, T. Hirose, Y. Shizuku, K. Shinonaga, N. Kuroki, and M. Numa, "An 80-mV-to-1.8-V conversion-range low-energy level shifter for extremely low-voltage VLSIs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 8, pp. 2026–2035, Aug. 2017.

11. J. Zhou, C. Wang, X. Liu, X. Zhang, and M. Je, "An ultra-low voltage level shifter using revised wilson current mirror for fast and energy-efficient wide-range voltage conversion from sub-threshold to I/O voltage," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 3,50 pp. 697–706, Mar. 2015.

12. V. L. Le and T. T.-H. Kim, "An area and energy efficient ultra-low voltage level shifter with pass transistor and reduced-swing output buffer in 65-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 5, pp. 607–611, May 2018. [10] L. Wen, X. Cheng, S. Tian,
H. Wen, and X. Zeng, "Subthreshold level shifter with self-controlled current limiter by detecting output error," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 4, pp. 346–350, Apr. 2016.

13. S. Kabirpour and M. Jalali, "A power-delay and area efficient voltage level shifter

based on a reflected-output Wilson current mirror level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 2, pp. 250–254, Feb. 2020.

14. R. Lotfi, M. Saberi, S. R. Hosseini, A. R. Ahmadi-Mehr, and R. B. Staszewski, "Energy-efficient wide-range voltage level shifters reaching 4.2 fJ/transition," IEEE Solid- State Circuits Lett., vol. 1, no. 2, pp. 34–37, Feb. 2018.

15. E. Maghsoudloo, M. Rezaei, M. Sawan, and B. Gosselin, "A highspeed and ultra low- power subthreshold signal level shifter," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 5, pp. 1164–1172, May 2017.

16. R. Luzzi, M. Bucci, and A. Trifiletti, "Self-biased cascode current mirror," U.S. Patent 0 160 557 A1, Jun. 25, 2009.

17. F. Ishihara, F. Sheikh, and B. Nikolic, "Level conversion for dual-supply systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 2, pp. 185–195, Feb. 2004.

B. Halak, V. Tenentes, and D. Rossi, "The impact of BTI aging on the reliability of level shifters in nano-scale CMOS technology," Microelectron. Rel., vol. 67, pp. 74–81, Dec. 2016.51