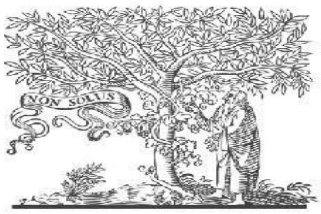
International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT



ELSEVIER
SSRN

IJIEMR Transactions, online available on 30th Dec 2018. Link :

http://www.ijiemr.org/main/index.php?vol=Volume-07&issue=ISSUE-13

Title: A NOVEL APPROACH FOR IMPLEMENTATION OF THREE LEVEL ISOLATED SINGLE STAGE POWER FACTOR CORRECTED CONVERTER

Volume 07, Issue 13, Pages: 677–681.

Paper Authors

LALJODI MAHABOOB BASHA, MD.FIROZ ALI

Nimra College of Engineering & Technology, A.P., India.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

A NOVEL APPROACH FOR IMPLEMENTATION OF THREE LEVEL ISOLATED SINGLE STAGE POWER FACTOR CORRECTED CONVERTER

LALJODI MAHABOOB BASHA[1], MD.FIROZ ALI[2]

[1]Student, M.Tech (POWER ELECTRONICS), Nimra College of Engineering & Technology, A.P., India.

[2]Associate Professor and Head, Dept. of Electrical & Electronics Engineering, Nimra College of Engineering & Technology, A.P., India.

Abstract— For improvement of grid quality and full capacity utilization in transmission lines, an Ac or Dc power converter is used. These converters operate with high power factor (PF) and low Total Harmonic Distortion (THD).By achieving high PF with high efficiency, inductive and capacitive filters followed by a diode bridge are used in Passive PF correction (PFC) circuits. In ac/dc power converters are required to operate with high power factor (PF) and low total harmonic distortion (THD) for improved grid quality and full capacity utilization of the transmission lines. Passive PF correction (PFC) circuits consist of inductive and capacitive filters followed by a diode bridge provide the simplest way of achieving high PF with high efficiency; however, they require low line frequency filters which are bulky and heavy. In order to operate at high frequency and reduce the size of the circuit, high frequency two -stage active PFC converters have been proposed. A high PF is achieved by this topology. Fuzzy controller is used which has the advantage of fast response. proposed converter exhibits high PF with less number of switches/diodes, operated at constant duty ratio. An inductor and a diode bridge are added to the conventional three-level isolated dc/dc converter, with a modified switching scheme and fuzzy based controller. The input current ripple frequency is twice of the switching frequency contributing to using smaller PFC inductor. Moreover, output current and voltage ripples are very less.

Keywords:
Power Factor (PF), Three Level Isolated, Stage Power Factor Corrected Converter, Fuzzy Controller.

INTRODUCTION

In order to operate at high frequency and reduce the size of the circuit, high frequency two-stage active PFC converters have been proposed . In this architecture, a front-end ac/dc PFC converter is operated with a switching frequency in the order of tenths to several hundred kHz for converters with Si semiconductor devices, and from several hundreds of kHz to tenths of MHz with wide-band gap devices, to shape the input current close to sinusoidal waveform in phase with the grid voltage. The second stage dc/dc converter provides the galvanic isolation and output voltage regulation. The controllers of the two stages are completely independent.The flexibility in control allows optimizing power stages, fast output voltage regulation and operating with high PF and low THD. However, this method comes with the expense of more components and larger size. Moreover, the constant switching losses such as parasitic capacitance losses associated with power switches reduce the efficiency of the converter at light load condition.A cost-effective approach to reduce the number of switches is to use single-stage ac/dc converters. In single-stage PFC converters, the front-end PFC stage and dc/dc stages are integrated and their operations are performed in a single-stage, basically, by sharing some of the switches and control scheme. An energy storage unit, capacitor or inductor, is located in between two stages, acting as a power

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

buffer and providing sufficient hold up time. Numerous PFC ac/dc single-stage topologies have been proposed in literature, particularly, operating in discontinuous conduction mode (DCM) for simple yet effective PF control.Majority of the proposed single-stage converters are proposed for low-power applications, where a flyback or forward converter derived topologies are used to achieve input current shaping and output voltage regulation. These converters offer cost-effective solution for low-power applications; however, they suffer from excessive voltage/current stresses on the switches, and are suitable for power levels lower than 200 W.For medium to high power applications, the research efforts have focused on ac/dc single-stage full-bridge (SSFB) converters. Current-fed SSFB converters deploy a current shaping inductor connected to the input of the diode-bridge achieving high PF; however, due to the lack of dc bus capacitor on the primary side of the transformer, the dc bus voltage is subjected to excessive overshoots and ringing. Furthermore, the output voltage contains high amplitude second-order harmonic oscillating with twice the line frequency, which restricts their operation. Voltage-fed SSFB converters do not exhibit the drawbacks of current-fed SSFB converters, where a large capacitor is located on the primary side dc bus. However, the dc bus voltage remains unregulated and it can be excessive at light load condition, as both input current shaping and output regulation are achieved with a single controller. In the literature, resonant converters adopting variable switching frequency have been proposed. In these converters, it is difficult to tune the resonant tank components over a wide load range, and optimize EMI filter. In majority of these aforementioned converters, the output current ripple becomes very large and the converter operation may transit to DCM mode.In two-level SSFB converters, the switches are exposed to high voltage stresses; thus, dc-link voltage is typically set close to 400V. In multilevel configurations, the voltage stresses across the switches are significantly reduced. Quite recently, single stage three-level (SSTL) converters have been studied, which allow a flexible dc-link voltage in the range of 400 to 800 V. In and a resonant SSTL converter is proposed to alleviate the drawbacks associated with SSFB converters, while reducing the voltage stress on the switches. In a recent publication, a three-level converter is integrated with the PFC boost stage by sharing the bottom switch. It is aimed to decouple the dc bus voltage and output voltage controllers, while the input current is adjusted with a constant duty cycle in DCM mode. The duty cycle of the bottom switch shapes the input current as well as is used to transfer energy from dc bus to output, simultaneously. The required duty cycle is the sum of the values achieved from individual PI controllers. The output voltage regulator sets the base duty cycle, while the PI controller of dc bus voltage regulator extends the duty cycle for the bottom switch. This topology alleviates most of the problems associated with SSFB converters, operated at constant switching frequency with a flexible dc-link voltage. However, two auxiliary diodes are added to 1) prevent input current to flow through the midpoint of split dc bus capacitors, and 2) enable a freewheeling path for primary side current when the energy in the leakage inductance is transferred to the bottom capacitor. In addition, a third auxiliary diode is added to serve as a boost PFC diode.Although the converter proposed in has been proven to work, it can further be integrated for lower power applications by removing the auxiliary diodes and developing a phase shifted modulation scheme.

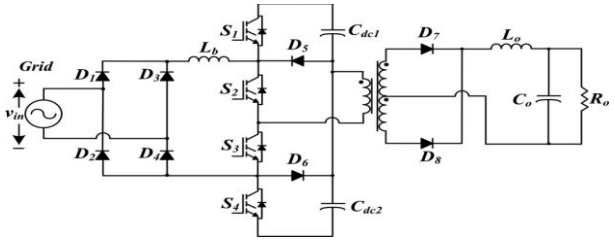


Fig. 1 Proposed three-level single-stage fully integrated PFC ac–dc converter

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

This study proposes a new SSTL isolated ac–dc PFC converter for high dc-link voltage and low-power applications, achieved with complete integration of two stages, where all of the switches are shared between input current shaping and output voltage regulation stages, as shown in Fig. 1. In comparison with the existing three-level single-stage topologies, the proposed converter offers minimum number of components as of three-level dc/dc converter, and does not require any auxiliary circuit other than a diode bridge and an inductor. The proposed topology can serve as a low cost power electronic interface intended for applications requiring high-voltage dc link.Two independent control algorithms, embedded in a single microcontroller, are used to achieve PFC and output voltage regulation. This feature allows having lower output current ripple and less distorted input current even at light load condition. In addition, the middle two switches are turned ON under zero current in DCM operation, and the upper and bottom switches are turned on under zero voltage, which increases the efficiency of the converter in comparison to hard-switched ac/dc single-stage converter. Furthermore, higher PF can be achieved at high line voltage due to the flexible dc-link voltage structure.

PROPOSED THREE-LEVEL SINGLE-STAGE PFC CONVERTER

The proposed converter is essentially an integrated version of a boost PFC circuit and three-level isolated dc–dc converter. Basically, a diode bridge and an inductor are added to the three-level isolated dc–dc converter topology as shown in Fig.4.1(a). Here, the inductor is charged when S2 and S3 are turned on simultaneously. Body diodes of S1 and S4 serve as the boost diode of the PFC boost converter. At the same time, S1 to S4 are switched to apply Vdc/2,−Vdc/2, and zero voltage across the primary side of the transformer. Thus, all of the switches are shared between the two-stages, which makes it fully integrated single-stage converter without any additional auxiliary switches. The switching scheme of the conventional three-level isolated dc/dc converter is given in Fig. 2(b). In this conventional scheme, the duty ratios of S2 and S3 are fixed close to 50% for simplicity in control and to ensure upper or lower three switches are not turned ON simultaneously as this would cause short-circuit through dc-link capacitors. Overlapping these two signals, as long as short-circuit condition is avoided, has no impact on the operation of the circuit. Similar to that in the conventional scheme, zero voltage is applied across the primary side of the transformer. This modified switching scheme is presented in Fig.4.1(c). When a boost inductor and a diode bridge is added to the nodes as in Fig.4.1(a), the overlap of gate signals of S2 and S3 enables applying input voltage across the boost inductor.

The switching scheme of the converter is given in Fig. 3. The switches S2–S3, and S1–S4 have 180° phase shift with respect to each other. The duty ratios of S2–S3 should be greater than 0.5 such that two signals overlap. Here, the circuit is explained considering that input inductor current is discontinuous and the switching scheme is as follows; S1 is turned on right after S3 is turned OFF, and similarly, S4 is turned on when S2 is turned OFF. A dead-time should be inserted in between the turning ON instant of S1 and turning OFF instant of S3, and likewise between switching of S2 and S4 to avoid short-circuit.

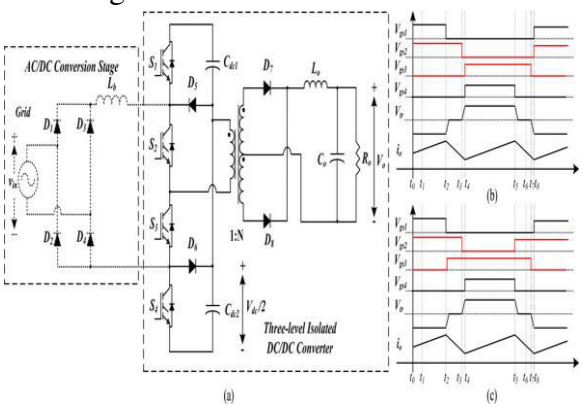


Fig. 2.1 Derivation of the proposed single-stage PFC converter; (a) topology, (b) switching scheme of the conventional three-level dc/dc converter, and (c) modified switching scheme

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

SIMULATION RESULTS

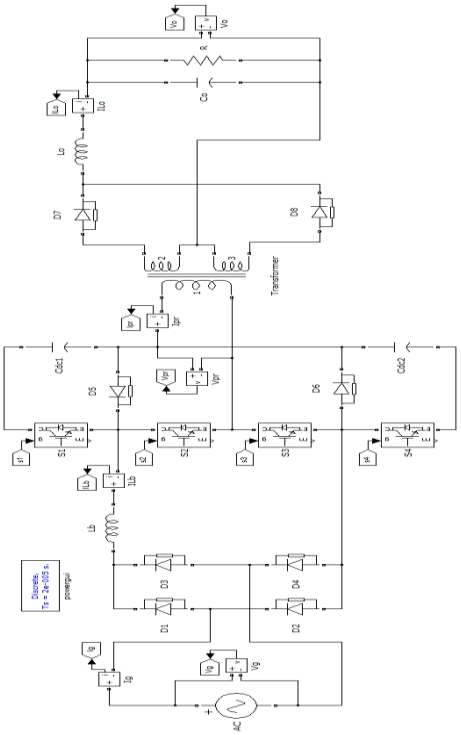


Fig. MATLAB simulation diagramm of proposed three-level single-stage fully integrated PFC ac–dc converter

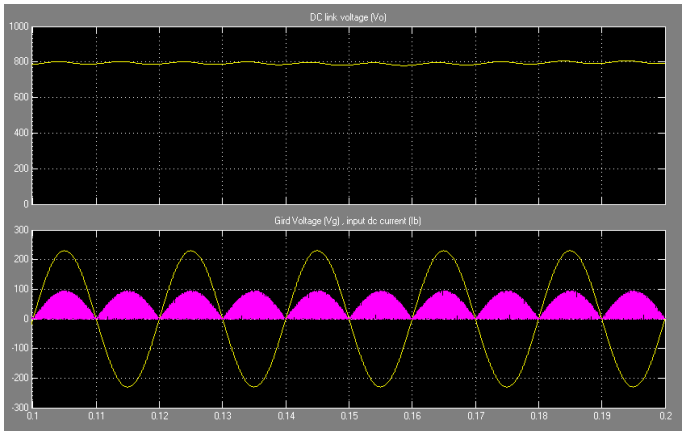


Fig. simulated waveforms: Input voltage, input current, dc-link voltage

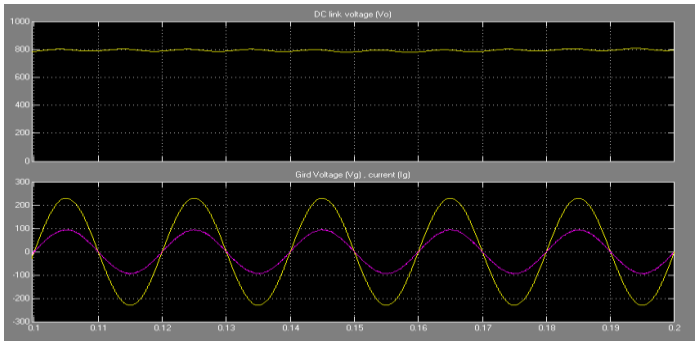


Fig. simulated waveforms: Input voltage , input current

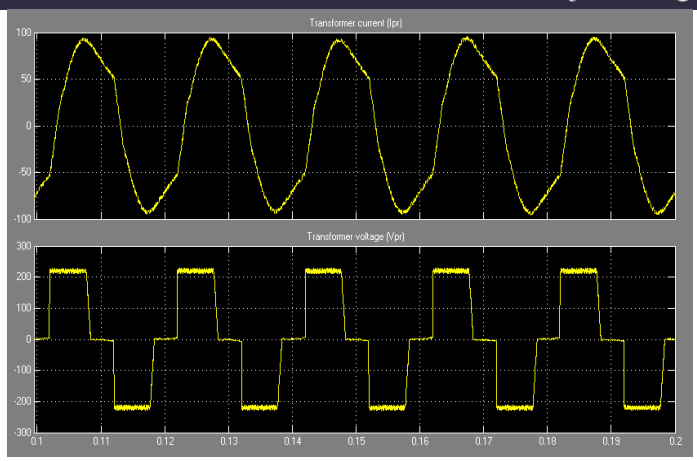


Fig. simulated waveforms: Transformer primary side voltage and current

CONCLUSION

The proposed converter exhibits high PF with less number of switches/diodes, operated at constant duty ratio. A PFC inductor and a diode bridge are added to the conventional three-level isolated dc/dc converter, while the switching scheme is modified to be compatible with single-stage operation. The input current ripple frequency is twice of the switching frequency contributing to using smaller PFC inductor. Two independent controllers, in favor of shaping the input current and regulating the output voltage, are adopted which simplifies the design and control of the circuit. The tradeoff between the PF and overall efficiency in the case of adopting a variable dc-link voltage is analyzed through developed loss model. The results of the analyses show that under 265 V line voltage, the PF can be increased to 0.99 from 0.88 by varying the dc-link voltage from 400 to 800 V. On the other hand, the efficiency of an 800 W/48 V converter can drop from 95.2% to 90% at full load. A 500W system has been designed to serve as a proof-of-concept achieving a peak efficiency of 90.8% at low input line voltage.

REFERENCES

[1] J. R. Morrison and M. G. Egan, “A new modulation strategy for a buckboost input AC/DC converter,” IEEE Trans. Power Electron., vol. 16, no. 1, pp. 34–45, Jan. 2001.

[2] H.Wang, S. Dusmez, andA.Khaligh, "Design and analysis of a full bridge LLC based PEV charger optimized for wide battery voltage range," IEEE Trans. Veh. Technol., vol. 63, no. 4, pp. 1603–1613, May 2014.

[3] J. Y. Lee and H. J. Chae, "6.6-kW on-board charger design using DCM PFC converter with harmonicmodulation technique and two-stageDC/DC converter," IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1243–1252, Mar. 2014.

[4] A. Khaligh and S. Dusmez, "Comprehensive topological analyses of conductive and inductive charging solutions for plug-In electric vehicles," IEEE Trans. Veh. Technol., vol. 61, no. 8, pp. 3475–3489, Oct. 2012.

[5] H. Ma, Y. Ji, and Y. Xu, "Design and analysis of single-stage power factor correction converter with a feedback winding," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1460–1470, Jun. 2010.

[6] S. Dusmez and A. Khaligh, "A charge-nonlinear-carrier-controlled reduced-part single-stage integrated power electronics interface for automotive applications," IEEE Trans. Veh. Technol., vol. 63, no. 3, pp. 1091– 1103, Mar. 2014.

[7] Y.W. Cho, J.-M. Kwon, and B.-H. Kwon, "Single power-conversion AC– DC converter with high power factor and high efficiency," IEEE Trans. Power Electron, vol. 29, no. 9, pp. 4797–4806, Mar. 2014.

[8] L. Rosseto and S. Buso, "Digitally-controlled single-phase single-stage ac/dc PWM converter," IEEE Trans. Power Electron., vol. 18, no. 1, pp. 326–333, Jan. 2003.

[9] S. Dusmez and A. Khaligh, "A compact and integrated multifunctional power electronic interface for plug-in electric vehicles," IEEE Trans. Power Electron., vol. 28, no. 12, pp. 5690–5701, Dec. 2013.

[10] D. D. C. Lu,H.H.C. Iu, andV. Pjevalica, "A single-stageAC/DC converter with high power factor, regulated bus voltage, and output voltage," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 218–228, Jan. 2008.

[11] H. J. Chiu, Y. K. Lo, H. C. Lee, S. J. Cheng, Y. C. Yan, C. Y. Lin, T. H. Wang, and S. C. Mou, "A single-stage soft-switching flyback converter for power-factor-correction applications," IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 2187–2190, Jun. 2011.

[12] H. Athab and D. Lu, "A single-switch ac/dc flyback converter using a CCM/DCM quasi-active power factor correction front-end," IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1517–1526, Mar. 2012.