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MODIFIED DESIGN OF TEST PATTERN GENERATOR FOR BUILT-IN SELF TEST APPLICATIONS

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Abstract —A low power Test Pattern Generator (TPG) designed by modifying Linear Feedback Shift Register is proposed to produce low power test vectors that are deployed on Circuit under Test (CUT) to slenderize the dynamic power consumption by CUT. The technique involved in generating low power test patterns is performed by increasing the correlativity between the successive vectors; the ambiguity in increasing the similarity between consecutive vectors is resolved b y reducing the number of bit flips between successive test patterns. Upon deploying the low power test patterns at the inputs of CUT, slenderizes the switching activities inside CUT that in turn reduces its dynamic power consumption. The resulted low power test vectors are deployed on CUT to obtain fault coverage. The experimental results demonstrate significant power reduction by low power TPG than compared to standard LFS R.

1. INTRODUCTION

An evolution of current microelectronics industry allows us to make complex digital systems on a single microchip. To design such a system is not an easy task anymore because the increasing density raises a whole set of different problems such as size, speed and power consumption of the chip. Nowadays, Complex VLSI testing problems such as BIST technique has been implemented and widely studied. In the BIST, the test vectors are generated by using LFSR (Linear feedback shift register) and applied to the device under test (DUT) which increases the area overhead therefore, reducing area which is a vital problem for the realization of Built-in-self test. As BIST technique requires high hardware overhead, this results in the memory required is more to store pre computed test pattern.The test vectors are generated by the random sequence test pattern which also known as LFSR. The LFSR is the sequential logic circuits used to create pseudorandom binary sequences (PRBSs). An LFSR circuit consists of a set of M registers and feedback taps that establish the sequence of states that the LFSR transitions through. The feedback taps are described by a modulo-2 polynomial. A primitive polynomial generates a maximal length of m-sequence, where the LFSR transitions through the 2m-1 state before repeat sequences, there is a single unused LFSR state. The PRBS is the binary output of the LFSR. The random binary sequence is described as pseudorandom, as the sequence is continuous in nature and that results from the correlation properties of a random sequence. Whereas in testing mode the power consumption increases due to following reasons: high switching activity between the two consecutive test pattern,

during test mode sequential activation of internal core, power utilized by extra circuitry during circuit under test and low relationship between the two test vector.

2. LFSR

A linear feedback shift register (LFSR) is commonly used as a test pattern generator (TPG) in the Low overhead Built-in Self Test (BIST). However, because a circuit under test (CUT) may contain many random pattern resistant faults, achieving high performance with pseudo-random patterns generated by an LFSR often requires unacceptably long test sequences. In BIST technology, it is an important issue to achieve high fault coverage and reduce test time. This paper focuses on a low power BIST scheme, another important concern in this field. Test patterns generated by an LFSR have fewer correlatives than those by normal operation. Therefore, when those patterns are applied to a scan chain, excessive switching activity due to low correlation between consecutive test patterns would dissipate more power. When the peak power exceeds the capability that can tolerate in a circuit, the circuit during test application would be permanently damaged due to excessive heat dissipation.A BIST strategy called dual-speed LFSR was proposed to reduce the circuit‟s overall switching activities. Having two different speed LFSRs, the proposed strategy applies some test patterns using a low-speed LFSR by connecting to some inputs that have elevated transition densities. However, this will increase test application time. In order to reduce the test length and average power simultaneously, Zhang and Roy proposed a low power random testing technique , in which both signal probabilities and activities at the primary inputs are optimized, and both the average power and the test length are reduced significantly. For ISCAS benchmark circuits, while the average of power reduction by using DS-LFSR is 19%, the average of power reduction by using the low power random testing technique in is as high as 78%. The previous techniques are unable to reduce the peak power, since the instantaneous power is not directly related to the average signal activities.A new weighted random pattern design for testability is described where the shift register latches distributed throughout the chip are modified so that they can generate biased pseudo-random patterns upon demand. A two-bit code is transmitted to each weighted random pattern shift register latches to determine its specific weight. The weighted random pattern test is then divided into groups, where each group is activated with a different set of weights. The weights are dynamically adjusted during the course of the test to "go after" the remaining untested faults. An accumulator-based 3-weight test pattern generation scheme is presented; the proposed scheme generates set of patterns with weights 0, 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of built in self test pattern generation, as well. Comparisons with previously presented schemes indicate that the proposed scheme compares favorably with respect to the required hardware.

3. ATPG

(Acronym for both **A**utomatic **T**est **P**attern **G**eneration and **A**utomatic **T**est **P**attern

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Generator) is an electronic design automation method/technology used to find an input (or test) sequence that, when applied to a digital circuit, enables automatic test equipment to distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects. The generated patterns are used to test semiconductor devices after manufacture, and in some cases to assist with determining the cause of failure (failure analysis.[1]) the effectiveness of ATPG is measured by the amount of modeled defects, or fault models, that are detected and the number of generated patterns. These metrics generally indicate test quality (higher with more fault detections) and test application time (higher with more patterns). ATPG efficiency is another important consideration. It is influenced by the fault model under consideration, the type of circuit under test (full scan, synchronous sequential, or asynchronous sequential), the level of abstraction used to represent the circuit under test (gate, register-transistor, switch), and the required test quality.The low power pattern generation technique is embedded onto an LFSR to create the proposed low power Test Pattern Generator (TPG). The design and power consumption report of the Conventional LFSR and proposed low power Test Patterns Generator (LP-TPG) is obtained using industry standard Cadence RTL compiler tool. The proposed low power Test Pattern Generator (TPG) design increases the correlation between test patterns to reduce the primary inputs (PIs) switching activities which eventually scale down the transitions inside the Circuit under Test (CUT), and hence power consumption.Thereafter the test pattern generated by both Conventional LFSR as well as low power Test Patterns Generator (TPG) designs are made to run on Circuit under Test (CUT) individually. C432 International symposium on Circuits and Systems (ISCAS 84) benchmark circuit is chosen as Circuit under Test (CUT) in order to obtain its power consumption during test mode. Further fault simulation is performed on Circuit under Test (CUT) upon deploying low power test patterns at its Primary Inputs (PIs); this process is again iterated on CUT with standard LFSR pattern to obtain desired fault coverage.

The low power pattern generation algorithm depicted in section 3 is coded using Hardware Descriptive Language (HDL) labeled Verilog with initial seed vector loaded as pre-initial stage to the TPG. Fig. 2 depicts 8-bit low power Test - Pattern Generator (TPG) composed of extrinsic XOR based Linear Feedback Shift Register (LFSR) along with an appended combinational logic to produce low power test vectors. Combinational logic consists of logic blocks and multiplexers (MUX) connected to the output of D – Flip flops in LFSR. The internal architecture of logic block is very simple as shown in fig. 3, it consists of an AND gate and an OR gate with their output connected to the inputs of MUX.

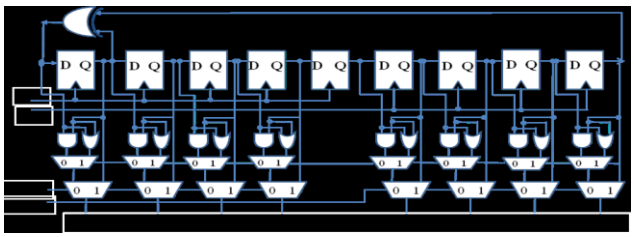

Fig 1 Modified design of lfsr with reduction circuit

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TPG to generate low power vectors are explained as follows:

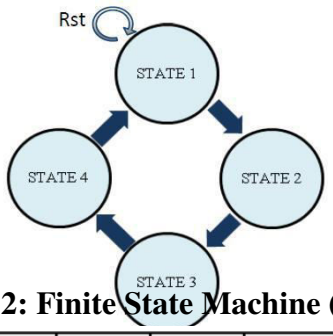

Figure 2: Finite State Machine (FSM)

STATE	en1	en2	sel1	sel2
1	1	0	1	1
2	0	0	1	0
3	0	1	1	1
4	0	0	0	1

Table 1: Control signals generated by FSM

The state machine depicted in fig 4 incorporates four states to produce control signals to drive generated by the above designed Finite State Machine (FSM).

State 1: In first state the FSM outputs control signals (en1 = 1, en2 = 0, sel1 = 1, sel2 = 1). The en1 enables the shift operation at the first half of LFSR whereas en2 signal disables second half of LFSR. The sel1 and sel2 in active high state tends MUX to fetch the output of D Flip Flops in Linear Feedback Shift Register (LFSR). Thus generating first test vector Pi at output of TPG.

State 2: At the second stage FSM produces (en1 = 0, en2 = 0, sel1 = 1, sel2 = 0). With en1 and en2 in active low state, the LFSR remains idle by outputting previous stored values. The sel1 signal outputs first half of Pi and sel2 signal tends MUX to compare the present bit value with the previous bit value; if the bits are similar, present bit value is outputted otherwise last bit of Pi is omitted to the output of TPG (Pi1 vector is produced).

State 3: The third FSM state generates (en1 = 0, en2 = 1, sel1 = 1, sel2 = 1). First half of LFSR remains idle with previous data at its output and the second half of it performs shift operation. Then the control signals sel1 and sel2 in active high state tends MUX to select the output of D-Flops. Thus generating third test vector Pi2 at output of TPG.

State 4: The final state produces (en1 = 0, en2 = 0, sel1 = 0, sel2 = 1). With active low en1 and en2 signal no shift operation is performed by LFSR thereby it remains in previous state. The active low sel1 signal tends MUX to compare the present bit value with the previous bit value; if bits are similar present bit value is outputted otherwise last bit of Pi is omitted to the first half output of TPG and second half is positioned by output of D-Flops. Hence this state produces test vector Pi3. The above process continues cyclically by going through STATE 1 to produce Pi+1.

Simulation Results

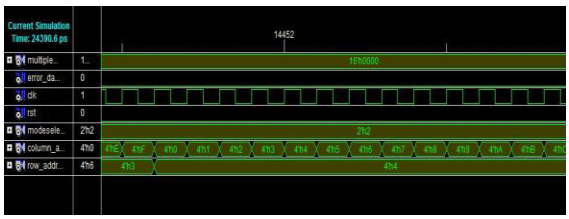

Fig3 :Results for no Faults

V. CONCLUSION

This paper shows an effective HDL implementation of low power utilization for test pattern generator using the Low

Transition LFSR technique. It also addresses a theory to express a test pattern creation by using Low Transition Linear Feedback Shift Register architecture. By using this technique; power consumption can be reduced as compared to the conventional LFSR technique. It shows that the total power consumed in low transition linear feedback shift register is 50.06% less than the conventional LFSR. From the results, it shows that Low Transition LFSR is very much constructive for power reduction techniques during testing mode.

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