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CHARGE RESTORATION USING ADIABATIC LOGIC IN LOW POWER DIGITAL CIRCUITS

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ABSTRACT

With the constant developing of circuit innovation in VLSI plan, one of the fundamental prime concentrations in research is moved to the ultra low power circuit's structures. Adiabatic rationale is contemplated and observed to be compelling in accomplishing the low power in VLSI circuits. The expression "adiabatic" alludes to the adjustment in the state without misfortune or addition of heat to the surrounding. The exchanging procedure lessens the power dispersal in adiabatic rationale amid the exchanging occasions. This paper explores the best adiabatic rationale among ECRL, PFAL, PAL. Every one of the circuits are planned and recreated utilizing the rhythm Virtuoso utilizing GPDK180nm innovation. We will compute the power scattering, delay, PDP (Power Delay Product) for every one of the circuits and contrasting them and the ordinary CMOS rationale. From the reenactment results we reason that the adiabatic rationale circuit expends less power and has less multifaceted nature contrasted with the ordinary CMOS circuits and PFAL devours less power and is more effective than other adiabatic rationales.

KEYWORDS

Adiabatic logic, Inverter, ECRL, PFAL, PAL, CMOS logic, Delay, PDP.

1. INTRODUCTION

The major trend of scaling in CMOS technology is the prime reason for today's design, capable of performing high speed computation. The MOSFET which inherently supports scaling, complexity is no longer an issue. The power dissipation in VLSI circuits has become major issue for modern portable devices [1]. The concern of low power is becoming important in non portable application as well. The interest in low energy computing is growing where adiabatic computing is exact approach in this point of view. We design low power circuits due to the increase in power consumption and complexity in design. Researchers have developed many design techniques to meet this scenario [2]. One way to deal with the problem of power consumption and circuit designing complexity is using adiabatic logic. Adiabatic logic is term given to electronic circuits with low-power which implement the reversible logic. The term adiabatic comes from the thermodynamics in fact where there is no energy transfer to the environment. The heat or the energy in the system remains constant. Adiabatic logic is broadly classified into two families:

1. Partially Adiabatic logic
2. Fully Adiabatic logic

Partially Adiabatic: In partially adiabatic, only some charge gets transferred to the ground that is some heat is dissipated. Consequently a piece of the vitality is just having the capacity to recoup, yet these circuits are anything but difficult to execute when contrasted with completely adiabatic rationale circuits.

Some mostly adiabatic rationale families are:-

1. Efficient Charge Recovery Logic (ECRL)
2. 2N-2N2P Adiabatic Logic
3. Positive Feedback Adiabatic Logic (PFAL)
4. Clocked Adiabatic Logic

Fully Adiabatic: In fully adiabatic circuits, the charges on the load capacitance get recouped and criticism to the power supply. Because of which completely adiabatic circuits become slower and mind boggling when contrasted with halfway adiabatic circuits.

Fully adiabatic logic families are:-

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1. Pass Transistor Adiabatic Logic (PAL)
2. Two Phase Adiabatic Static CMOS Logic (2PASCAL)
3. Split-Rail Charge Recovery Logic (SCRL)

Charge restoration in Adiabatic Logic Circuits

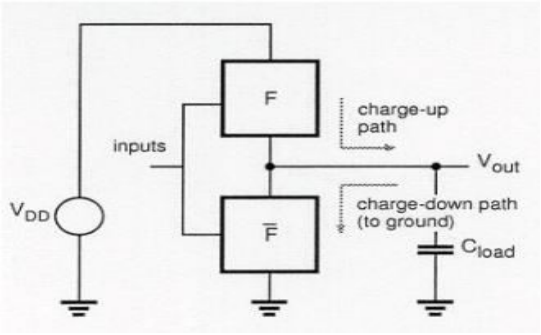

Fig. 1: Conventional CMOS circuit

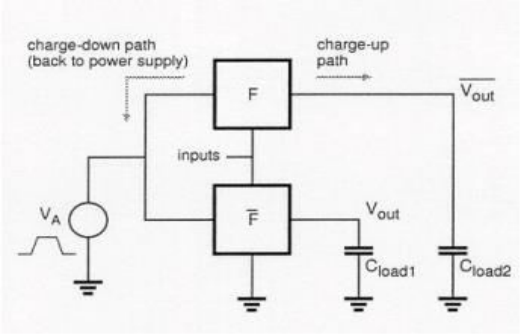

Fig. 2: Adiabatic logic structure

The contrast between a CMOS and Adiabatic structure is appeared in the above figures 1 and 2 individually. The CMOS utilizes steady voltage control supply, where as Adiabatic rationale utilizes control clock as supply. Not at all like CMOS, adiabatic logic will reuse the vitality disseminated and works in two stages. The two stages are precharge stage and recovery stage. In the precharge stage the adiabatic circuits convey vitality. In the recovery phase they recover their energy using diodes or diode like devices for precharge [4].

2. PREVIOUS WORK

The key impediment in a significant number of the electronic frameworks is Power utilization. The power utilization, being the constraint extending from versatile telecom to compact and work area frameworks. Applications like surrounding knowledge and sensor systems where the power is the significant concern. New structure strategies and philosophies are required to control and restrain the Power utilization. In light of scaling in the electronic circuits, circuits are winding up progressively fit, the usage of capacitances require extensive utilization of transistors and offer new applications to the clients. The utilization of increasingly number of transistors will prompt more power utilization. In few cases, low power configuration is required to keep away from over-heating. There are different applications like bioelectronics where the circuit would be embedded inside the body and needs to work either with little battery or utilizing power collecting strategies [2]. CMOS innovation is the most well known MOSFET innovation accessible today a likewise called integral MOS innovation. The power dissemination is the point at which the circuit switches. In the CMOS, the draw up and pull down transistors are planned utilizing the Boolean articulation. The entryway yield is associated with Vdd or Vss. Where CMOS isn't profitable as it isn't practicable for certain circuits it is hard to actualize. To beat these impediments of CMOS circuits, we execute low power computerized circuits utilizing adiabatic rationale.

3. PRESENT WORK

The CMOS innovation can be chiefly certify to normally low power dissipation and abnormal state coordination. The ECRL and PFAL will dissipate low power in contrast with CMOS and other rationale circuits [1]. When ECRL, PFAL and PAL logics are implemented there is gradual decrease in power consumption. These adiabatic logics are designed and tested. Adiabatic logic is basically implemented in order to reduce Power dissipation amid exchanging process: It further reuses a portion of the Power by reusing from burden capacitance. Adiabatic circuits utilize steady current source control supply for reusing and trapezoidal or sinusoidal power supply voltage for decreasing scattering [4]. The designing procedure of various adiabatic circuits is as follows.

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Efficient Charge Recovery Logic (ECRL)

ECRL comprises of circuits that are two transistors cross-coupled, for example m1 and m2 and NMOS in the N-trees. AC power supply i.e., the power check is utilized in ECRL, so to reuse the energy provided. The out and /out are produced with the goal that the power clock generator drives a consistent load capacitance which is autonomous of info flag. On account of the cross-coupled PMOS transistors full yield swing is gotten in both pre-charge and recuperation phases[3].

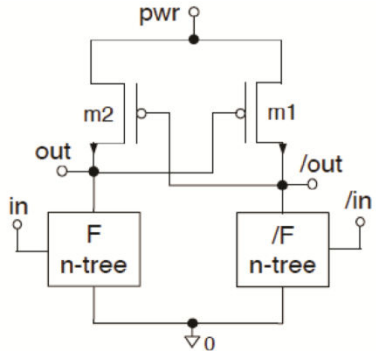

Fig. 3: Basic circuit of ECRL

Positive Feedback Adiabatic Logic (PFAL):

The PFAL comprises of the hook made of two PMOS and NMOS that the blocks are in parallel with the transmission PMOS. PFAL rationale amid the Recovery stage, the load capacitance gives back the energy to the power supply and consequently energy provided diminishes. The partial energy recovery circuit structure is so called [PFAL] Positive Feedback Adiabatic Logic [2].

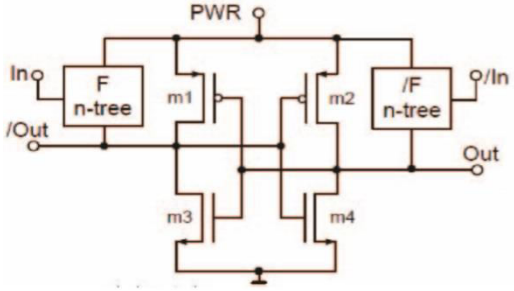

Fig. 4: Essential square of PFAL

Pass-transistor Adiabatic Logic (PAL):

PAL includes a certified and relating pass transistor NMOS true and moreover a cross coupled lock PMOS m1 and m2. The power input clock will slant down to zero, recovering the set away energy on the yield capacitance [2].

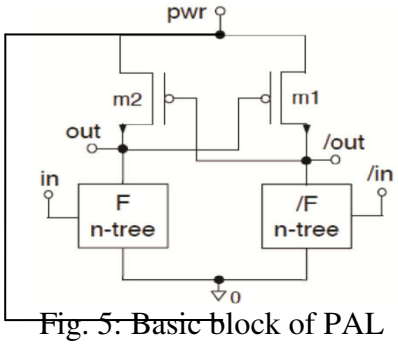

Fig. 5: Basic block of PAL

4. SIMULATION RESULT

For exploring which circuits perform better for sub-nanometer innovation, circuits are structured and tried. The circuits are being structured utilizing Cadence virtuoso tool with gpdk 180nm model library. This is done in virtuoso. In all of the plans for the adiabatic logic, the clock is considered with recurrence of 200 MHz. The structured circuits, recreated waveforms and watched results are given in following segments.

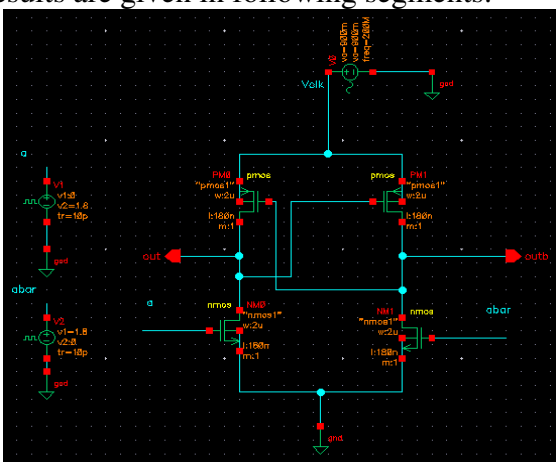

Fig. 6: ECRL Inverter

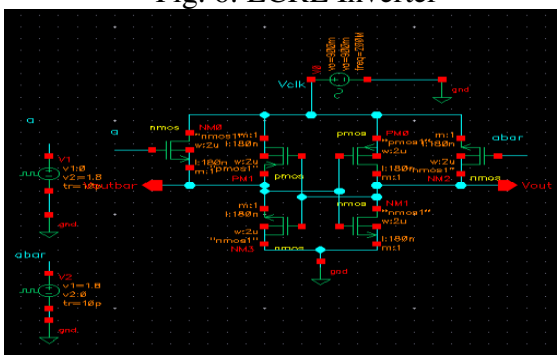

Fig. 7: PFAL Inverter

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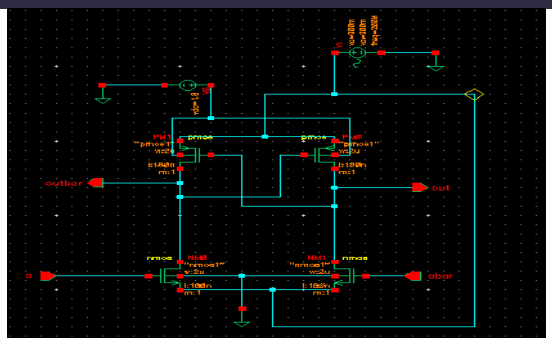

Fig. 8: PAL Inverter

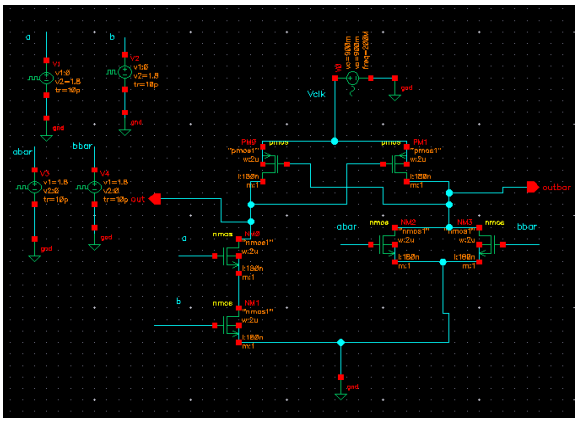

Fig. 9: ECRL NAND Gate

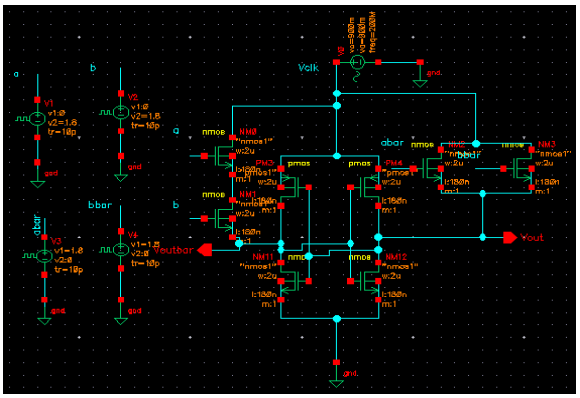

Fig. 10: PFAL NAND Gate

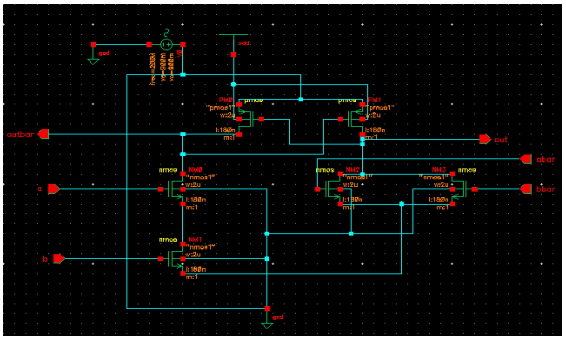

Fig. 11: PAL NAND Gate

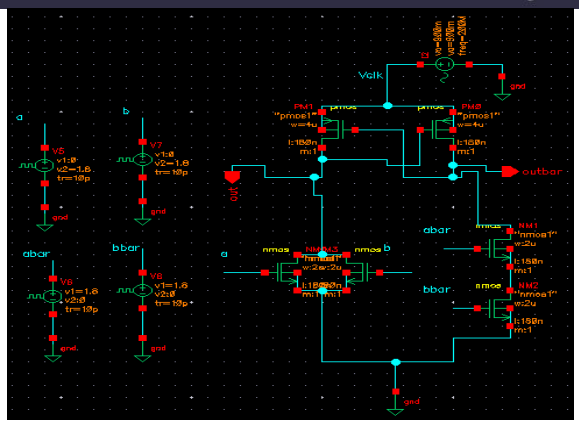

Fig. 12: ECRL NOR Gate

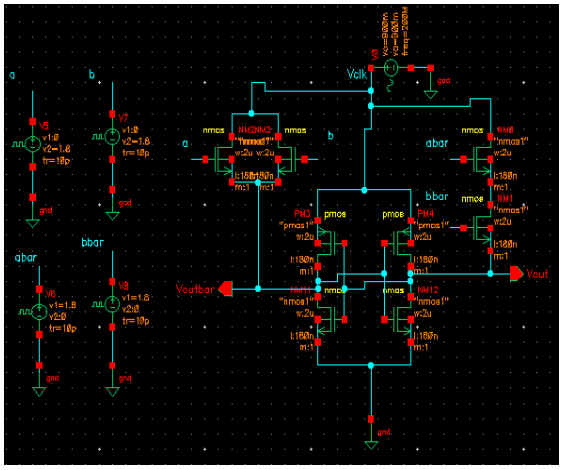

Fig. 13: PFAL NOR Gate

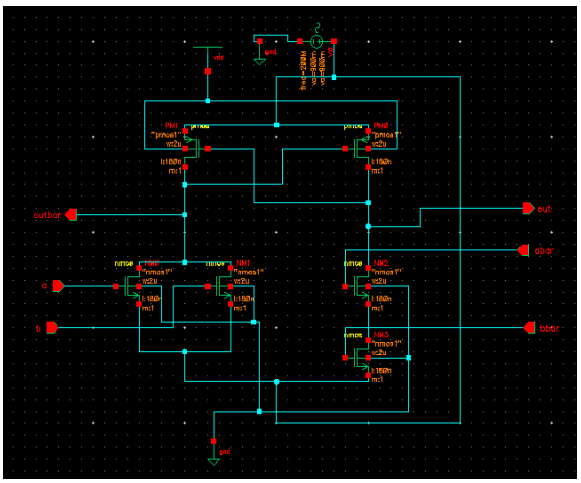

Fig.14: PAL NOR Gate

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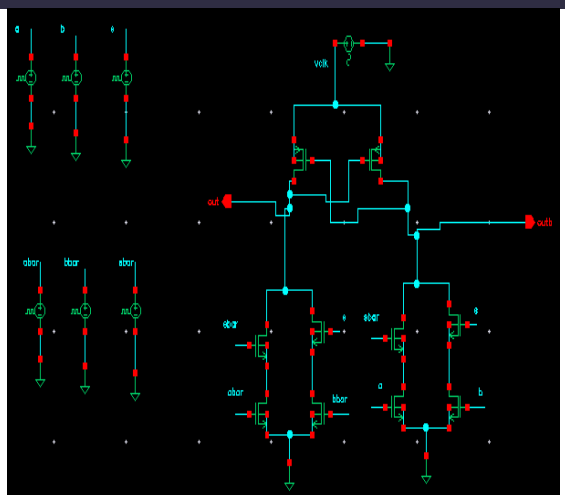

Fig. 15: ECRL MUX Gate

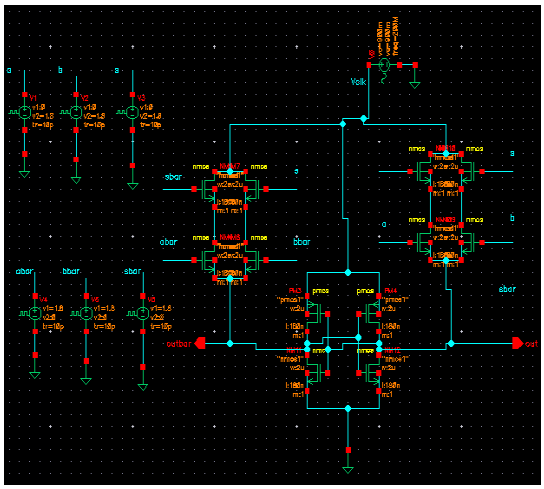

Fig. 16: PFAL MUX Gate

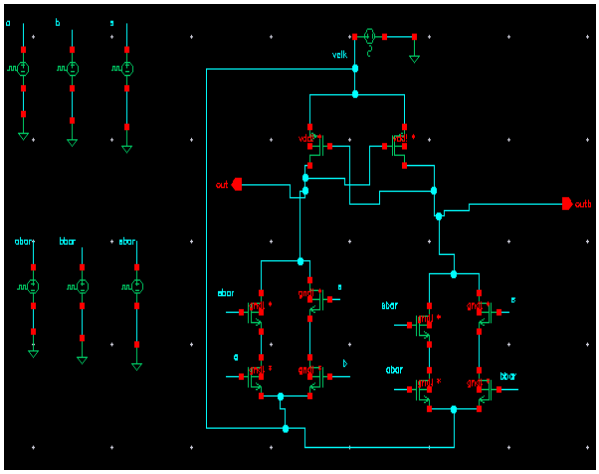

Fig.17: PAL MUX Gate

The Simulation waveforms of Inverter, NAND, NOR, MUX using PFAL Adiabatic logic are as follows:

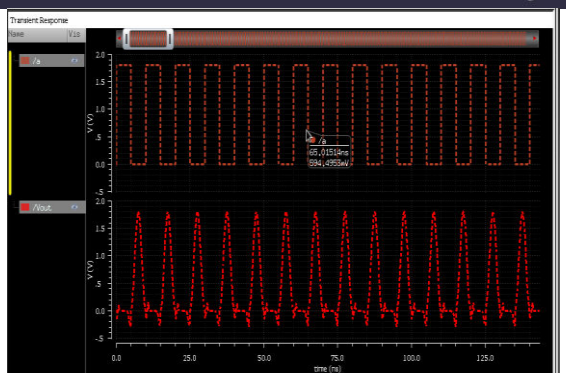

Fig. 18: Simulated output of PFAL Inverter Gate

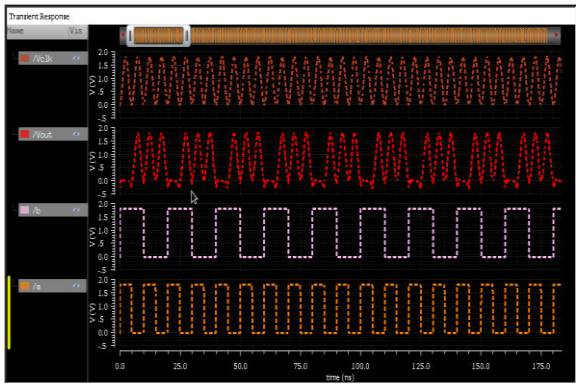

Fig. 19: Simulated output of PFAL AND Gate

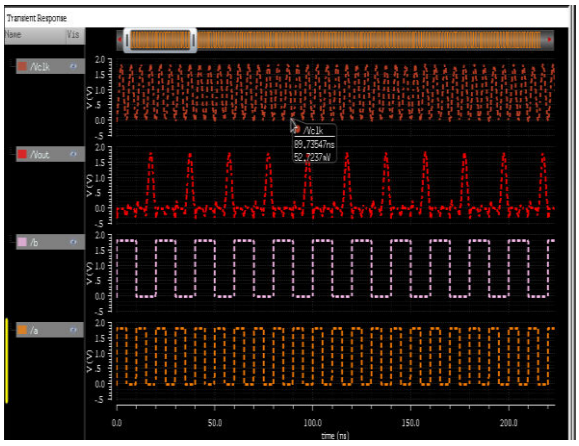

Fig. 20: Simulated output of PFAL NOR Gate

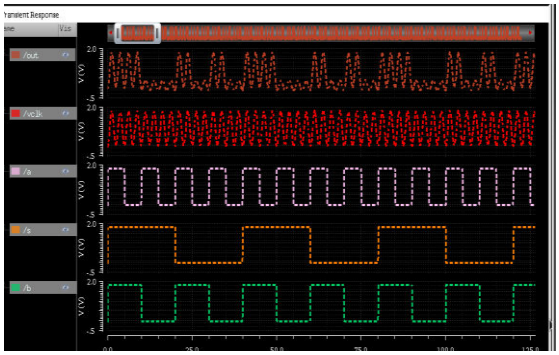

Fig. 21: simulated output of PFAL MUX

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Tab. 1. Simulation Result of Inverter at room temperature for 200 MHz clock frequency

Logic	Power (uW)	Delay (ns)	PDP
CMOS	3.16	0.01975	$6.241x10^{-17}$
ECRL	0.650	1.265	$8.222x10^{-16}$
PFAL	0.229	1.24	$2.868x10^{-14}$
PAL	0.9685	1.396	$1.353x10^{-14}$

Tab. 2.Simulation Results for the NAND at room temperature for 200 MHz clock frequency

Logic	Power (uW)	Delay (ns)	PDP
CMOS	3.814	0.01503	$5.7324x10^{-14}$
ECRL	0.9036	1.263	$1.4124x10^{-15}$
PFAL	0.2908	1.242	$3.62627x10^{-16}$
PAL	4.026	1.4	$5.8457x10^{-13}$

Tab. 3. Simulation Results for the NOR at room temperature for 200 MHz clock frequency

Logic	Power (uW)	Delay (ns)	PDP
CMOS	3.06	0.0423	$12.9438x10^{-14}$
ECRL	0.6954	1.239	$8.6160x10^{-14}$
PFAL	0.3559	1.243	$4.4238x10^{-15}$
PAL	0.6898	1.452	$10.0158x10^{-14}$

Tab. 4. Simulation Result of MUX at room temperature for 200 MHz clock frequency

Logic	Power (uW)	Delay (ns)	PDP
CMOS	9.23	10.05	$9.27615x10^{-14}$
ECRL	1.289	16.22	$2.0907x10^{-14}$
PFAL	0.995	16.24	$1.615x10^{-14}$
PAL	0.4524	16.31	$7.378x10^{-14}$

The Inverter, NAND, NOR, MUX in CMOS, ECRL, PFAL, PAL rationale styles and watched the power at 27^0C. We can infer that, PFAL devours less power and postponement contrasted with different logic styles. The proposed adiabatic logic style is better contrasted with CMOS style on the grounds that; the adiabatic rationale style uses the rule of adiabatic exchanging and energy recuperation. Where in the charging way, the diode is expelled and the high yield abundancy will be accomplished and subsequently the power utilization of the diode is disposed of. In spite of the fact that the CMOS innovation furnish circuits with low static power dissipation, amid the task of exchanging it creates flows, because of the release of load capacitances, they cause power dissipation which increments with clock recurrence.

PFAL is structured in such a way to devour less power. The transistor tally increments yet this rationale reuse energy. The essential square of PFAL shows that as opposed to scattering energy put away amid the way toward charging, it reuses the energy back to the power supply in this manner, diminishing power dissipation.

5. CONCLUSION

In this paper different digital circuits like Inverter, NAND, NOR, MUX are designed and simulated in conventional CMOS and adiabatic logic families like ECRL, PFAL, and PAL. The power dissipated, delay, and Power Delay Product are calculated. From the recreation results the perceptions made for all the adiabatic logics and table is being plotted for parameters. Adiabatic logic circuits are contrasted and that of traditional CMOS logic circuits and subsequently we infer that PFAL adiabatic rationale style is invaluable where power

decrease as a prime objective. The PFAL experiences huge exchanging time so it isn't appropriate where delay is basic. Adiabatic PFAL logic gives better performance over conventional CMOS logic.

ACKNOWLEDGEMENT

We would like to express our gratitude to our management of Rajarajeswari College of Engineering for providing us the lab and infrastructures for conducting this project.

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