International Journal for Innovative Engineering and Management Research
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LOW COMPLEXITY VLSI ARCHITECTURE FOR VARIABLE RATE DECODER

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Abstract

In this work, we examine the various post-processing strategies utilized after the iterative decoder has deciphered a product's unique identifier code. Adaptive variable-rate transceivers will be crucial for low-power transmission in a variety of scenarios. Designing flexible transceivers is difficult for high-bit-rate fiber-optic communication systems because the extra circuits required to coordinate the flexibility would increase size and reduce speed. Error-correcting codes, which can identify and fix faults, are a common method for dealing with error rates that fluctuate randomly. To prevent unnecessary overhead and minimize delay, these codes can be crafted to perform optimally at low mistake rates while degrading to a lesser degree as error rates rise. The computational cost is increased for most parameter selections, however the post-processing is rarely used unless the channel is excessively noisy. To avoid the error floor while yet maintaining a high data transmission rate, we present a new approach that integrates existing strategies. Long high-rate codes are another area where the algorithm should perform well, avoiding the error floor without any additional work.

Index Terms— Optical communication, forward error correction (FEC), BCH code, triple-error-correcting, lookup table

Introduction

Data transmission over noisy or error-prone channels can be made more reliable with the help of a technology called forward error correction (FEC). The goal of forward error correction (FEC) is to allow for the detection and correction of faults in the received data without necessitating retransmission of the original data [1]. Before sending data, an FEC system uses a mathematical formula to determine how many extra bits to add to the original data. These redundant bits are added to a transmission in order to compensate for a particular threshold of transmission mistakes that can be detected and fixed at the receiving end. The same procedure is then used by the receiver to detect and, if necessary, fix any problems. FEC is widely employed in digital communication and storage systems like hard drives and flash memory [2]. This includes satellite and wireless communications. Combining it with additional error detection and repair methods, including cyclic redundancy check (CRC) and automated repeat request (ARQ), is a common practice to further increase transmission dependability.

Digital communication and data storage systems frequently employ the error-detection method known as Cyclic Redundancy Check (CRC). The process involves adding a checksum, calculated by a mathematical formula, to the information before sending or storing it [3]-[4]. A fresh checksum is calculated using the same procedure at the receiving end and compared to the original. In the absence of a mismatch between the checksums, the data is considered to have been corrupted either during transmission or storage. The CRC algorithm accomplishes its task by viewing the information at hand as a binary polynomial, which is then divided by a different polynomial. The CRC, or remainder, of the division operation is added to the information. If the

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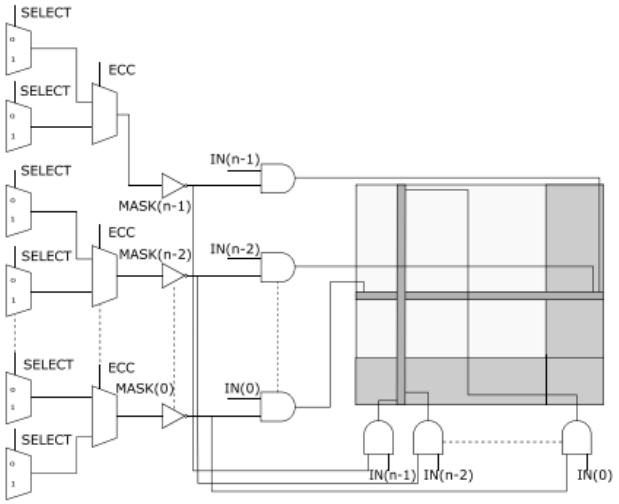
received CRC is the same as the transmission CRC, then the data was successfully received without corruption.

Single-bit errors, burst errors, and other typical forms of mistakes that can occur during transmission or storage are all detected by Cyclic Redundancy Check, making it a potent error detection approach [5]. The term "variable error rate" describes the situation where the likelihood of errors in a digital communication channel changes over time or as a function of other parameters like the signal strength, interference, or noise level, and is used in many different types of communication and storage systems. As a result, the error rate can take on a wide range of values, and the communication system must be built to accommodate this inconsistency. Using error-correcting codes that can detect and correct errors is a common method for dealing with varying error rates[6]. Codes of this type can be crafted to repair errors efficiently at low error rates, then scale back their efforts as the error rate rises, saving bandwidth while keeping delays to a minimum.

Adaptive modulation techniques are another option, as they can change the modulation scheme and transmission parameters depending on the state of the channel. A lower-order modulation technique can be used to mitigate the effects of errors if the error rate is large, whereas a higher-order modulation strategy can be used to transmit more data per symbol if the error rate is low. Error rate variability may also be reduced through the use of forward error correction, interleaving, and diversity. Adding redundant information to the transmitted data for the purpose of correcting errors at the receiver is known as forward error correction [7, 8]. Although diversity employs numerous transmission routes or antennas to boost the likelihood of successful transmission, interleaving reorganizes the transferred data to lessen the impact of burst faults. Error-correcting codes, modulation schemes, and transmission systems that are robust across a wide range of error rates are needed to handle the general case of variable error rates.

Existing work

The investigation into a variable-rate, variable-t architecture is detailed below (VRVTPD). Compared to the original VRPD design, which had a fixed t = 3, the VRVTPD architecture allows for a wider range of attainable coding benefits by allowing for the error-correction capability (t) to be varied. The amount of faults that a decoder is able to fix is equal to the error-correction capacity of the corresponding component code. Hence, t can be increased to improve coding gain. Increasing t, however, necessitates further hardware in the form of base modules for the product decoder and hardware to support the configurability, which in turn increases the required size and the power dissipation. The VRVTPD architecture allows for customization of the coding rate, decoding iteration count, and t between three and four. The base OH of component codes shifts when t varies, hence the OHs for the component codes are different when t = 4 compared to t = 3. More circuitry must be incorporated into the modules of the VRPD architecture to handle the difference in OHs between t = 3 and t = 4. To accommodate the variable t, adjustments must be made to the KES module of the VRPD design, which was previously indistinguishable from the standard fixed-rate decoder.



As can be seen in Fig. 1, the mask creation process for the VRVTPD's product code memory is very similar to that of the VRPD. Because the OHs that were chosen are different.

For the same reason that different OHs are chosen for t = 3 and t = 4, two different sets of multiplexers are employed to move the codeword to the MSB in each

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case [9]. As can be seen in Fig. 2, the output of the first set of multiplexers is connected to a second set of multiplexers that are used to pick the shifted codeword that corresponds to the t mode. The number of syndromes calculated by the module is proportional to (2m)t, where m and t are positive integers. This means that there are more symptoms found when t = 4 compared to t = 3. When t = 3, it is best to forgo computing additional syndromes in order to conserve energy and avoid unnecessary computations. Because of this, we add another multiplexer before the syndrome computation, which disables the input to the SYND module for the t = 4 syndromes. The modified codeword is then sent back to the system's primary syndrome calculator.

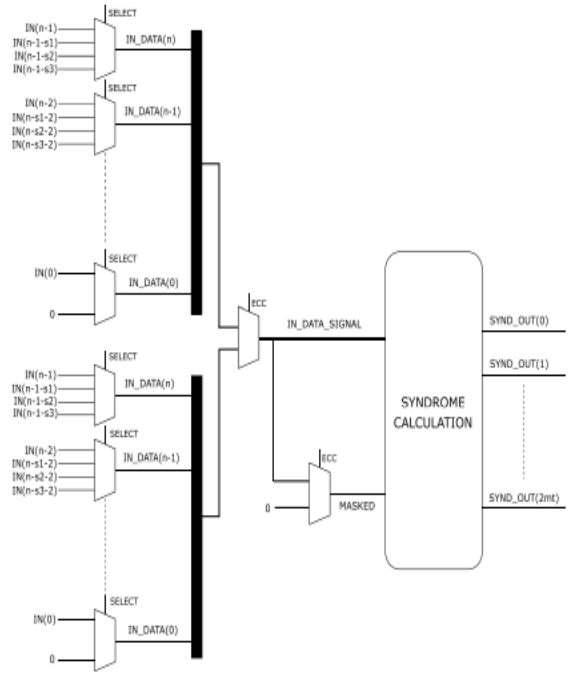

Fig. 2. VRVTPD Syndrome Module for Calculation

The CHIEN module of the VRVTPD design also needs supplementary hardware in order to function with alternative OHs while operating in the t = 3 and t = 4 modes. This is a high-level block diagram of the VRVTPD design's implementation of the CHIEN module. The KES module's supplied error-locator polynomial coefficients must be gated at the reduced bit locations. Unfortunately, the identical gating mechanism from VRPD design cannot be employed because the OHs for t = 3 and t = 4 are distinct. This results in different truncated bit positions. Gating is applied to the reduced bit rate in accordance with the OH chosen in the respective t mode via an additional set of multiplexers (MUXES) at the output of the generated gating signals. Switching from t = 3 in mode 2 of 25.0% OH to t = 4 in mode 2 of limit is a good illustration of how these muxes function. It is necessary to gate 28 bits shorter in the first case, but just 16 bits shorter in the second case [10]-[12]. When in t = 4 mode, GATED 2 is applied to the overlapping bits (17 to 28), and when in t = 3 mode, GATED 1 is applied. The error signals for both ts are then generated by the CHIEN module using the gated coefficients. At the CHIEN module's output, multiplexers shift the error signals to the LSB before selecting the final error signal using the ECC.

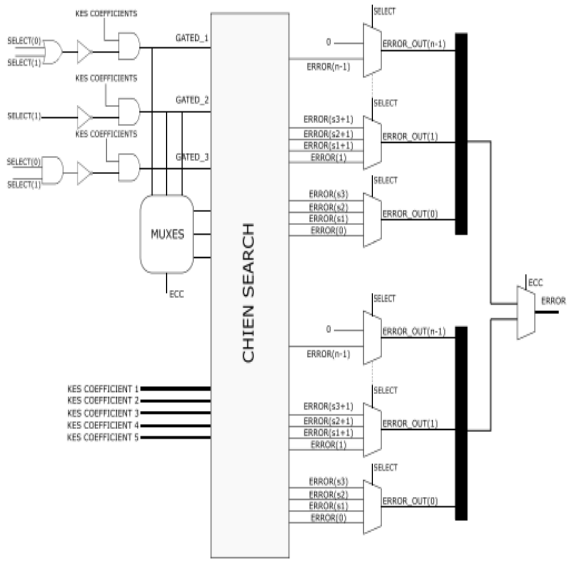

Fig 3. Chien Search block diagram

In artificial intelligence and computer science, the Chein Search Algorithm is a search algorithm used to efficiently explore huge state spaces in search of a desired state or set of states that meet a given set of criteria.

The approach is based on a constraint satisfaction problem (CSP), which is the search for a set of assignments to variables that satisfies a given set of constraints [11]. The Chein Search Algorithm is effective because it employs a systematic, depth-first exploration of the space of variable assignments while

making use of a set of heuristics to direct the search and selectively prune the search tree.

When there are many variables and constraints in a CSP, the Chein Search Algorithm excels. First, the algorithm chooses a variable and gives it a value determined by the satisfied requirements. The remaining variables' assignment spaces are then explored in a recursive fashion, with heuristics being used to choose which variables to assign next and in what order.

The primary benefit of the Chein Search Algorithm is its speed in locating and eliminating huge regions of the search area that are not likely to yield a solution. Because of this, it is able to swiftly identify a solution by effectively exploring the remaining space, unlike other search algorithms.

The Chein Search Algorithm may need a lot of processing resources for very large problem spaces, and it is not guaranteed to discover a solution for all CSPs.

Proposed work

In digital communication systems, error-correcting codes are decoded using a decoder called a hard decision product decoder. The algorithm determines which codeword is most likely to have been broadcast by multiplying the received signal by all possible codewords.

Technology known as very large-scale integration (VLSI) is used to create ICs with a huge number of transistors on a single chip. Several modern technologies, such as digital communication networks, rely on complex digital circuits made possible by VLSI technology.

The steps below outline the digital circuit architecture needed to create a hard decision product decoder utilizing VLSI technology.

Does a multiplication on the incoming signal using each code in the dictionary.

Adds the received signal to each codeword to get the product.

Finds the highest-product-generating codeword by comparing them.

The most likely codeword to have been communicated is returned.

Dedicated hardware or programmable logic devices can be used in a VLSI implementation of a hard decision product decoder's many comparators and multipliers (PLDs). Taking into account power usage, timing, and space constraints might be difficult when designing such a circuit.

While developing a hard decision product decoder with VLSI technology, it is also important to consider other parameters, such as latency, throughput, and error rate performance. The digital communication system's requirements and the required performance metrics will determine the balance between these competing aspects.

When used to the decoding of error-correcting codes in digital communication systems, a hard decision product decoder implemented using VLSI technology can offer a high-performance, low-power solution.

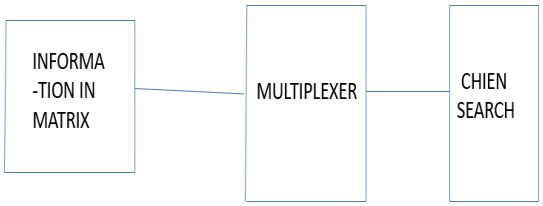

Fig 4. Proposed work block diagram

matrix To maximize the effectiveness of MIMO transmissions, multiplexing is employed in wireless communication systems. Depending on the channel conditions, the transmitting and receiving antennas are partitioned into numerous groups, or sub-matrices, and one is chosen for broadcast. The signal-to-noise ratio (SNR) and channel matrix are two pieces of data that are sent between the transmitter and receiver in SMM-based channel selection. The sender uses this data to determine which sub-matrix is ideal for transmission, while the receiver does the same for receiving. Often, a parameter like channel capacity or error-less decoding is maximized to determine the optimum sub-matrix to use. To do this, we first determine the channel conditions, and then evaluate the performance of each sub-matrix, choose the one that yields the best

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results. In MIMO systems with many antennas, selection is very helpful since it maximizes resource utilization. High data speeds and dependable communication are possible despite harsh channel circumstances thanks to the system's ability to sub-matrix the antennas. This method-based selection is widely employed in contemporary MIMO systems, such as 5G and beyond, and is crucial for enhancing the performance of wireless communication systems.

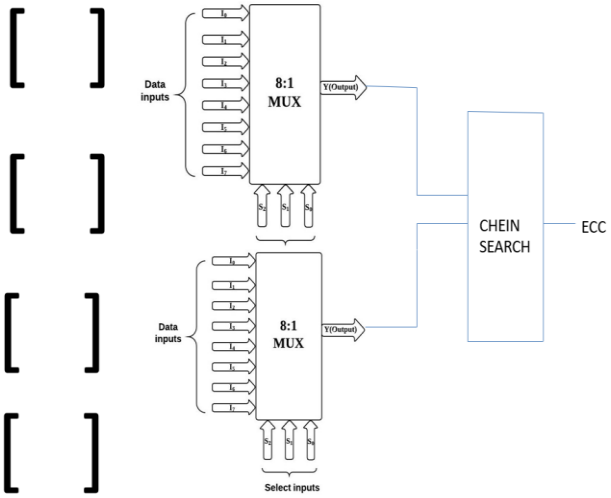

Fig 5. Maritx sub selection block diagram

The HDPC decoder is widely employed in low-cost communication systems with limited computational resources due to its simplicity and efficiency as a decoding method. It may not be well suited for high-performance communication systems, however, because it is not as accurate as alternative decoding algorithms like maximum likelihood decoding.

HDPC decoding is widely employed in many different kinds of communication systems, such as wireless networks, satellite communications, and storage systems, and is an essential approach for enhancing the reliability of data transfer over noisy channels.

Conclusion

An effective and economical error correcting system can be created by combining a Hard Decision Product Decoder (HDPC) with a refined Chein Search Algorithm. While the enhanced Chein Search Algorithm is able to efficiently explore the space of variable assignments in order to find a solution that satisfies the requirements of the problem, the HDPC provides a simple and efficient decoding technique that can fix faults in incoming data. These two methods, when combined, allow for efficient error correction to be performed with minimal computing overhead. Because of this, the system can be implemented in many contexts, such as wireless networks, satellite communications, and data storage. Together, HDPC and an enhanced Chein Search Algorithm are an important study topic in the fields of communication systems and signal processing because of their potential to increase the dependability of data transmission over noisy channels.

Results

Chip designers and engineers rely on the area report to examine potential layout flaws such improper component placement, clogged routing, and wasted space. The report can also be used to pinpoint underutilized or overutilized regions of the chip and offer design enhancement recommendations. The maximum clock frequency and propagation delays throughout all logic paths are just two of the metrics that make up a design's timing report. Parameters like setup and hold times, clock skew, and signal jitter may also be included in the report if they pertain to the time frame under study. Potential timing violations can be found and fixed in the report, and the design can be optimized for peak performance.

Using this information, we compared the time, space, and resources used by our current and proposed projects.

PARAMETER	EXISTING METHOD	PROPOSED METHOD
DELAY	1.065ns	0.65ns
UTILIZATION OF MULTIPLEXER`S	more	less

Fig 5. Comparison results

The operation and efficiency of digital circuits can be studied through the simulation of waveforms. The waveforms can be used to spot problems, verify functionality, and fine-tune design settings since they are visualizations of the voltages and currents in the circuit over time.

Fig 6. Output Wave forms

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