International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

ELSEVIER SSRN

IJIEMR Transactions, online available on 4th Sept 2019. Link :http://www.ijiemr.org/downloads.php?vol=Volume-08&issue=ISSUE-09

Title **IMPLEMENTATION OF NOVEL FLOATING POINT MULTIPLIER ACCUMULATOR CONTENT**

Volume 08, Issue 09, Pages: 10–14.

Paper Authors

DR. R. PRAKASH RAO, K. PRAVEEN

Matrusri Engg College, Hyderabad-59.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

IMPLEMENTATION OF NOVEL FLOATING POINT MULTIPLIER ACCUMULATOR CONTENT

DR. R. PRAKASH RAO[1] , K. PRAVEEN[2]

[1]Associate Professor, Department of ECE, Matrusri Engg College, Hyderabad-59.

[2]Assistant Professors, Department of ECE, Matrusri Engg College, Hyderabad-59.

[1]prakashiits@gmail.com, [2]kundapraveen@gmail.com

Abstract— The main bottleneck of fixed point Multiplier Accumulator Content (MAC) is- necessity of Analog to Digital Converter and Digital to Analog Converter. The MAC can be utilized to design the discrete wavelet transform (DWT) and the DWT can be used in the design of signal processing applications. Fixed point MAC cannot process the floating point values. Hence, the sampled version data which is a function of floating point (FP) numbers need to convert into fixed point and then stored in buffer. To convert the analogue data into digital A to D converters are to be used at input side. At the output side to reconstruction signal D to A converters are to be used. The disadvantage of A to D converters and D to A converters are nothing but system complexity. As sampling rate increases the design complexity of the system increases. Hence, here we are going to design a Floating Point Multiplier Accumulator Content (FP MAC) through VHDL for audio applications in order to eliminate usage of ADC and DAC. Here, FIR filters are chosen because they are stable. The Daubechy-4[1] window is used to design the FIR filters. Daubechy-4 window is the windowing technique defined for audio applications where 4 indicates the four floating point co-efficients.

Index Terms— fixed point MAC, ADC and DAC, floating point MAC, VHDL, FIR filters, Daubechy-4 window.

I. Introduction

In this digital era fundamentally, processors are two types. They are microprocessors and DSP processors. Microprocessors are used in order to process data processing algorithms. DSP processors are used to process the one dimensional signals like speech, voice, ECG, EEG, Seismographic signal etc,. The heart of the microprocessor is ALU where as the heart of the DSP processor is MAC. ALU is designed by the arithmetic operators and logical operators where as Multiplier Accumulator Content is designed using multiplier, adder & shifter. Multiplier Accumulator Content is constructed by the convolution operation. Convolution consists of addition, multiplication and shift operations. In DSP all LTI systems are designed by the convolution operation. DSP processors are two types that is fixed point DSP processors and floating point DSP processors. Wherever high precision is required there floating point DSP processors are used. But for all general purpose applications fixed point DSP processors are used [2]. The limitations of fixed point DSP processor IS speed. Even though the fixed point MAC can operate with greater speed, but it will be limited through ADC and DAC. Hence in order to enhance momentum of fixed point DSP processors fast algorithms are required at the bottom level subsystem designs. Therefore, customer defined IEEE-754 FP packages are developed then added to simulation tool of Modelsim 10.3c for build up FP MAC. With the updated Modelsim 10.3c tool, FP adder, FP multiplier & shifter has been designed, with theses three floating point MAC is designed through

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

convolution operation.

II. Traditional work

Figure 1 shows the fixed point MAC. In this, h(n) indicates the Debochy-4 filter co-efficient in floating point. Because, the input data is in fixed point which is the output of A to D converter, the filter co-efficients are also needed to be scaled to fixed-point notation.

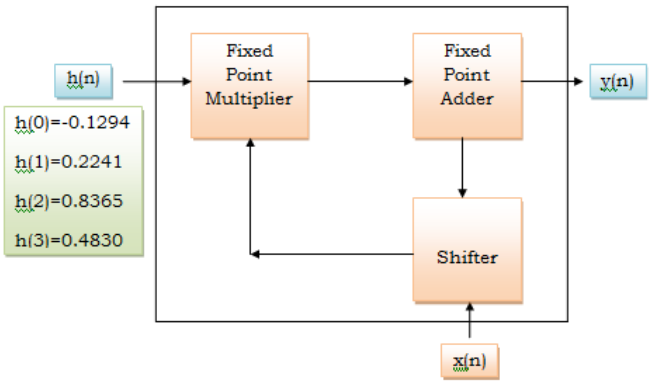

Fig 1: fixed point MAC

Hence the scaled version of the filter co-efficients are convolved with the input data x (n). The fixed point adder will add previous outcome with the current outcome [3]. In such a way, this operation goes on from n is equal to zero to till n is equal to N -1 and finally output which is convolved version is available at the output terminal of MAC.

Table 1: scaled version values

Filter co-efficients	Scaled up by 2^3
h(3)= 0.4829629	h(3)≈4
h(2)= 0.8365163	h(2)≈7
h(1)= 0.2241439	h(1)≈2
h(0)=-0.1294095	h(0)≈ -1

The table 1 shows the scaled version of the filter co-efficients. These Coefficients are scaled to 2^3 scale factor. The mathematical expression of convolution operation is given by-

$$y(n)=\sum_{k=0}^{N-1} h(k).x(n-k) \quad \text{--1}$$

This expression has been developed as MAC block diagram. The convolution operation with x(n) versus h(n) can be understood by the following graphical method shown in figure2.

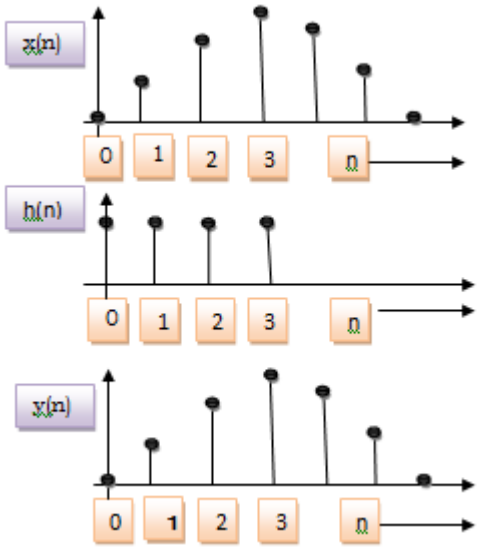

Fig 2: x(n) convolved with h(n)

If n=0,1,2,3; above equation1 becomes

y(1) = h(0).x(1) +h(1).x(0) +h(2).x(-1) +h(3).x(-2)

y(2) = h(0).x(2) +h(1).x(1) +h(2) .x(0) +h(3).x(-2)

y(3) = h(0).x(3) +h(1).x(2) +h(2).x(1) +h(3).x(0) and

y(0) = h(0). x(0) +h(1).x(-1) +h(2).x(-2) +h(3).x(-3)

III. Novel MAC

Novel Multiplier Accumulator Content is constructed by FP multiplier, FP adder and shifter. For avoiding disadvantages of fixed point Multiplier Accumulator Content floating point Multiplier Accumulator Content was developed. With this floating point MAC, ADC, DAC need not be used. They can be eliminated completely. Hence, now direct floating point input values are applied to the DSP system. The filter co-efficients

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

also need not to scale.

A.FP Adder:

The FP adder is the part of the FP MAC. If N1 is first FP number, N2 is the second floating point number, the first number sign, exponent and mantissa can be represented by S1, E1, M1 and the second number sign, exponent and mantissa can be represented by S2, E2, M2. Its step by step floating point addition operations can be illustrated as given as below figure 3.

At starting step, the system will read the two operands of N2 and N1 for de-normalization. If the numbers are the de-normalized, make implicit bit of fraction to zero otherwise set it to 1.

1. The two exponents E2 and E1 are compared through the 4-bit subtractor. If E2 is greater than E1 then N2 and N1 are swapped. It means that the earlier M1 is now treated as M2 and vice versa.
2. Now the smaller mantissa M1 is to shift right till both exponents make equal.
3. Add 2 mantissas of M1 & M2.
4. Then result is to pass to leading one detector for normalization operation.
5. Depending on output of detector, if it is required the result is to shift right by one bit.
6. The output is rounded to the nearest value after normalization.
7. Based on this result the exponent is adjusted.
8. Now the simulation is completed based on the maximum exponent.
9. The final result is noted after the underflow and overflow check.

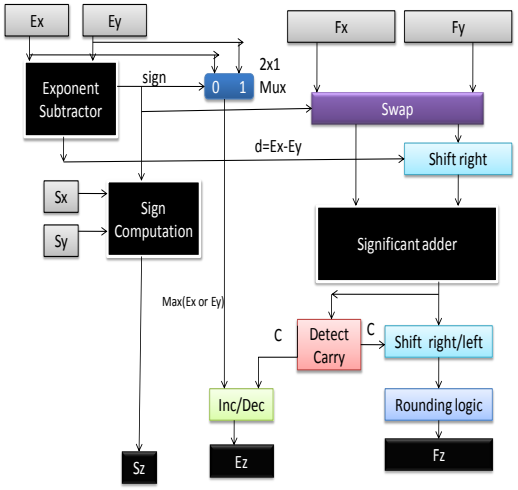

Fig 3: Traditional 16 bit floating point adder

B.FP Multiplier:

Implementation of 16-bit FP multiplier is quite easy. It contains eleven bits of mantissa, four bits of exponent & one bit of sign. In order to get multiplication between 2 sixteen bit FP numbers, the FP multiplier structure needs 2 sixteen bit registers for placing its fields.

Algorithm for Standard FP Multiplier:

If N1 is first FP number, N2 is the second floating point number, the first number sign, exponent and mantissa can be represented by S1, E1, M1 and the second number sign, exponent and mantissa can be represented by S2, E2, M2. Its step by step floating point multiplication can be illustrated as given as below:

1. For getting sign bit N1 & N2 should be functioned with exclusive-OR operation.

2. E1and E2 should be added and bias of 7 is subtracted for half precision. Exponent value is confirmed

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

depending on carry transmit from result of multiplication.

3. Two operands will be multiplied through basic multiplier algorithm.
4. After multiplication result bits will be increased.

Truncation mode will be applied. Hence right side bits are truncated for fitting result.

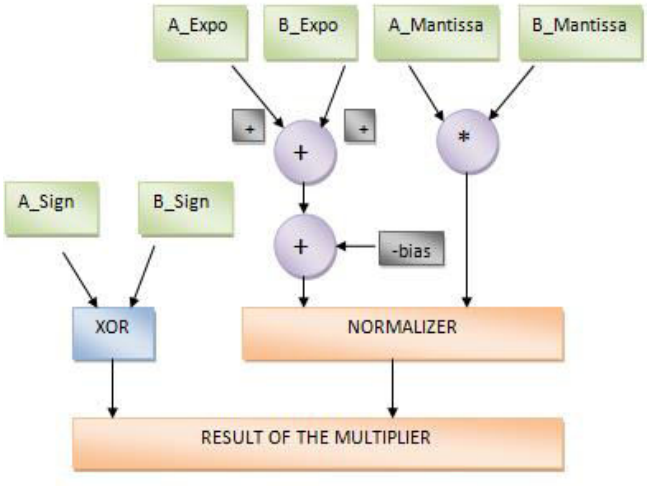

Fig 4: 16 bit floating point multiplier

With respect to the above description, the structural design of the 16- bit FP multiplier was developed and given in Fig 4,

C. Std. FP Multiplier Accumulator Content:

Using FP adder and FP multiplier & shifter the floating point MAC was developed as shown in below figure 5.

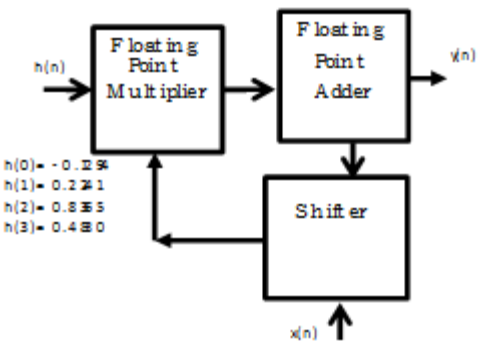

Fig 5: Std. FP MAC

V. Results

This section shows synthesis and simulation outcomes of FP MAC and FP adder.

Results for simulation:

simulation was done through a software tool of Modelsim 10.3c. Since, Modelsim doesn't have FP packages, consumer defined FP package is compiled with the standard library. Now input is applied by test-bench and after simulation output is attained.

For Std. FP Adder:

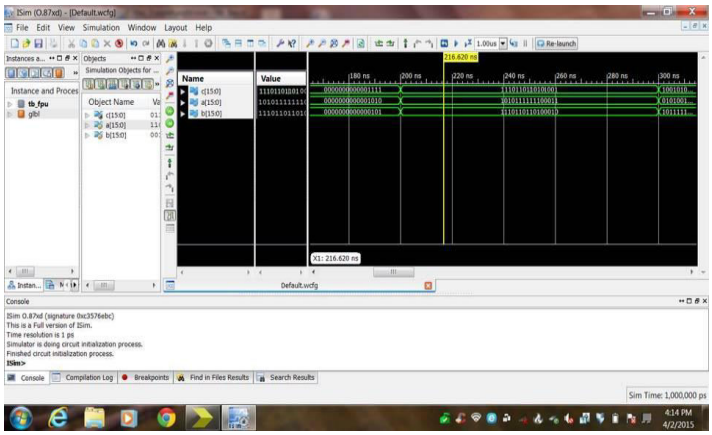

Fig 6: results of Std FP Adder

Synthesis was performed by Xilinx Synthesis Technology tool by SPARTAN 3e device with a package of Xc2s50e-ft256-6.

Table 2: Synthesis results for FP Adder

Hardware Resources/Parameters	**Std. FP Adder**
No. of Input - Outputs	31 of 182(17%)
No. of Basic Elements	59 of 1728(3.4%)
Min. time period	0.983 ns
Max. Freq (speed)	1017.2 MHz
Utilization of Power	9.726mw

Fig 6 & Table2 give synthesis and simulation

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

results of FP adder. This was observed as- the attained speed was 1017.2 MHz. Power consumption and delay of 9.726mw & 0.983 ns. The hardware resources are 17% of IOs and 3.4% of BELs.

Std. FP MAC:

Fig 7 & Table3 give synthesis report and simulation results of Standard FP MAC.

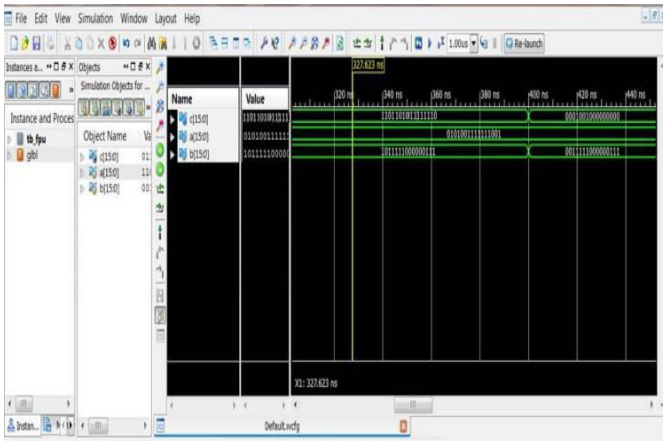

Fig 7: results of Std FP MAC

Table3: Synthesis report of floating point MAC

H/W Resources	Std FP MAC
No. of Input - Outputs	54 of 182(29%)
No. of Basic Elements	103 of 1728(6%)
Min. time period	1.286 ns
Max. Freq (speed)	793.65 MHz
Utilization of Power	12.493mw

By Table 3 analysis, this was observed as- attained speed was 793.65 MHz Power utilization & delay are 12.493mw and 1.286 ns. The resources taken are 29% of Input-outputs and 6% of Basic Elements.

VI. Conclusion

As so many bottlenecks seen by fixed point MAC that is mainly precision and speed, the Std. FP MAC was built up here through compiling consumer defined FP package to IEEE 754 library. Through the development and compilation of FP packages, a virtual connection was accomplished between input and system.

References

1 J. Karam, "On the Roots of Daubechies Polynomials,"International Journal ofApplied Mathematics, Vol. 20,No.8, 2007, pp. 1069-1076

2. Strang, G. and Nguyen, T., Wavelets and Filter Banks. Wellesley- Cambridge Press, Wellesley, Massachusetts, 1996.

3. A. Fettweiss. Wave digital filters: theory and practice. Proceedings of the IEEE, 74(2):270–327, February 1986.