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Paper Authors

MD SANA SAMREEN, SK ZEENATH, B SWETHA

Anu Bose Institute of Technology K.S.P Road, New paloncha, Bhadradri Kothagudem, Telangana, India

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BIDIRECTIONAL DC/DC CONVERTER IN HYBRID ELECTRIC VEHICLE SYSTEMWITH DUAL-BATTERY ENERGY STORAGE

MD SANA SAMREEN[1], SK ZEENATH[2], B SWETHA[3]

[1,2,3]UG Students, Dept. of Electrical and Electronics Engineering

Anu Bose Institute of Technology, K.S.P Road, New paloncha, Bhadradri Kothagudem, Telangana, India.

ss9989526135@gmail.com[1], zeenathzeenu558@gmail.com[2], bhukyaswetha3@gmail.com[3]

Abstract: -This investigation builds up a recently structured, protected, bidirectional dc/dc converter (BDC) that interfaces fundamental vitality stockpiling (ES1), a helper vitality stockpiling (ES2), and dc-transport of various voltage levels, for application in half breed electric vehicle frameworks. The proposed converter can work in a stage up mode (i.e., low-voltage double source-driving mode) and a stage down (i.e., high-voltage dc-interface vitality recovering mode), both with bidirectional power stream control. Moreover, the model can freely control power stream between any two low-voltage sources (i.e., low-voltage double source buck/help mode). Thus, the circuit setup, activity, unfaltering state examination, and shut circle control of the proposed BDC are talked about as per its three methods of intensity move. Besides, the recreation and exploratory outcomes for a 1 kW model framework are given to approve the proposed converter.

Index Terms: -Bidirectional dc/dc converter (BDC), dual battery storage, hybrid electric vehicle.

I.INTRODUCTION

Worldwide environmental change and vitality supply is declining have animated changes in vehicular innovation. Cutting edge innovations are at present being investigated for application in future vehicles. Among such applications, energy unit cross breed electric vehicles (FCV/HEV) are proficient and promising up-and-comers. Before, Ehsani et al. examined the vehicles' elements to search for an ideal torque-speed profile of the electric impetus framework [1]. Emadi et al. talked about the working properties of the topologies for various vehicles including HEV, FCV, and progressively electric vehicles [2]. Emadi et al. additionally incorporated power hardware escalated arrangements in cutting edge vehicular power framework to fulfill immense vehicular burden [3]. Schaltz et al. adequately separate the heap control among the power module stack, the battery, and the ultracapacitors dependent on two proposed vitality the board systems [4]. Thou thong et al. considered the impact of energy component (FC) execution and the upsides of hybridization for control systems [5]. Chan et al. looked into electric, half breed, and power module vehicles and concentrated on structures and displaying for vitality the board [6].

Khaligh and Li displayed vitality stockpiling topologies for HEVs and module HEVs (PHEVs). They likewise examined and thought about battery, UC, and FC advances. Moreover, they additionally tended to different cross breed ESSs that coordinate at least two stockpiling

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gadgets [7]. Rajashekara looked into the flow status and the necessities of essential electric drive segments the battery, the electric engines, and the power gadgets framework [8]. Lai et al. executed a bidirectional dc/dc converter topology with two-stage and interleaved qualities. For EV and dc-microgrid frameworks, the converter has an improved voltage change proportion [9]. Moreover, Lai likewise contemplated a bidirectional dc to dc converter (BDC) topology which has a high voltage transformation proportion for EV batteries associated with a dc-microgrid framework [10]. In FCV frameworks, the fundamental battery stockpiling gadget is generally used to begin the FC and to supply capacity to the impetus engine [2, 3]. The battery stockpiling gadgets improve the naturally moderate reaction time for the FC stack through providing pinnacle control during quickening the vehicle [7]. Also, it contains a powerful thickness part, for example, supercapacitors (SCs) takes out pinnacle control drifters during quickening also, regenerative braking [11]. As a rule, SCs can store regenerative vitality during deceleration and discharge it during speeding up, in this way providing extra power. The powerful thickness of SCs draw out the life expectancy of both FC stack and battery stockpiling gadgets and upgrades the general productivity of FCV frameworks [2-8, 12]. An utilitarian chart for a run of the mill (FCV/HEV) control framework is represented in Fig. 1 [4, 13]. The low-voltage FC stack is utilized as the fundamental power source, and SCs straightforwardly associated in parallel with FCs. The dc/dc control converter is utilized to change over the FC stack voltage into an adequate dc-transport voltage in the driving inverter for providing capacity to the impetus engine.

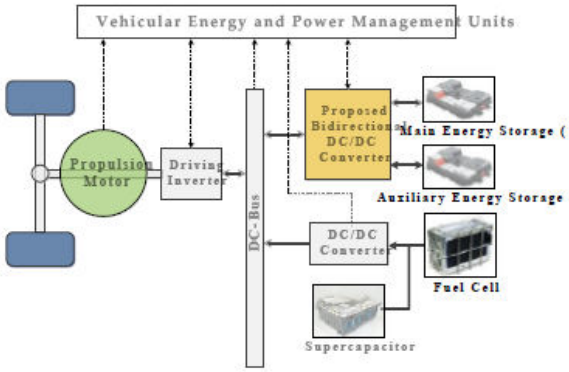

Fig. 1. Typical functional diagram for a FCV/HEV power system.

Besides, ES1 with rather higher voltage is utilized as the fundamental battery stockpiling gadget for providing pinnacle power, and ES2 with rather lower voltage could be a helper battery stockpiling gadget to accomplish the vehicle go extender idea [13]. The capacity of the bidirectional dc/dc converter (BDC) is to interface double battery vitality stockpiling with the dc-transport of the driving inverter. For the most part, the FC stack and battery stockpiling gadgets have diverse voltage levels. A few multiport BDCs have been created to give explicit voltages to burdens and control power stream between various sources, in this way decreasing in general cost, mass, and power utilization [14-27]. These BDCs can be ordered into confined and no disengaged sorts. In separated converters, high-recurrence control transformers are connected to empower galvanic segregation. A couple of disengaged multiport BDC topologies have been researched, for example, the fly back, half-or full-connect circuits, double dynamic scaffolds, and resounding circuits [14-17, 20, 22, 24]. The writing recommends that no disengaged BDCs are more viable than ordinary segregated BDCs

in EVs [18, 19, 21, 23, 25-27]. Liu et al. [18] inferred no secluded multi-input converter topologies by method for a blend of buck, lift, Ćuk, and Sepic. In [23], Wu et al. built up the three-port no segregated multi-input-multi-yield (MIMO) converter topologies for interfacing a sustainable source, a capacity battery, and a heap at the same time. The three twofold info converters created in [19] include a solitary post triple-toss switch and just a single inductor. A measured no disconnected MIMO converter was introduced in [26]. This converter is connected to hybridize clean vitality wellsprings of EVs and the fundamental lift circuit was altered and incorporated. Be that as it may, the voltage increase of the MIMO lift circuit is restricted by and by, due to the misfortunes related with certain parts, for example, the fundamental influence switch, inductor, channel capacitor, and rectifier diode. To beat this disadvantage, three-port power converter that has high-increase trademark and contains FC, battery sources and stacked yield for interfacing HEV, just as a dc-microgrid was displayed [27]. In spite of the fact that the multiport BDC examined in [25] can interface multiple wellsprings of intensity and work at various voltage levels, despite everything it has restricted static voltage gains, bringing about a limited voltage go and a low voltage contrast between the high-and low-side ports. This examination proposes another BDC topology for FCV/HEV control frameworks that comprises of an interleaved voltage-doubler structure [9, 28] and a synchronous buck-support circuit. It highlights two fundamental working modes: a low-voltage double source-controlling mode and a high-voltage dc-transport vitality recovering mode. What's more, the proposed converter can autonomously control power stream between any two low-voltage sources when in the low-voltage double source buck/help mode. A comparable topology was presented in [29] that just portrays a concise idea. On the other hand, this investigation shows a nitty gritty examination of the activity and shut circle control of this new topology just as recreation and exploratory outcomes for every one of its methods of activity. Additionally, this examination extended the topology displayed in [29] in light of the fact that the proposed converter can work over a more extensive scope of voltage levels. The primary attributes of the proposed converter are condensed as pursues: 1) interfaces in excess of two dc hotspots for various voltage levels, 2) controls power stream between the dc transport and the two low-voltage sources and furthermore autonomously controls power stream between the two low-voltage sources, 3) improves static voltage increase and consequently lessens switch voltage stress, and 4) has a sensible obligation cycle and delivers a wide voltage distinction between its high-and low-side ports. The rest of this paper is organized as pursues. The converter topology and activity rule are introduced in Section II. The consistent state attributes of the converter, which depend on the activity rule, are investigated in Section III, though Section IV introduces the converter control plot. A 1 kW converter model was developed in this examination to approve the proposed converter and exhibit its benefits. The comparing recreated and trial results are presented in Section V. Finally, Section VI details the conclusions of this study.

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II.TOPOLOGY AND OPERATION MODES

The proposed BDC topology with dual-battery energy storage is illustrated in Fig. 2, where V_H, V_{ES1}, and V_{ES2}represent the high-voltage dc-bus voltage, the main energy storage (ES1), and the auxiliary energy storage (ES2) of the system, respectively. Two bidirectional power switches (S_{ES1} and S_{ES2}) in the converter structure, are used to switch on or switch off the current loops of ES1 and ES2, respectively. A charge-pump capacitor (C_B) is integrated as a voltage divider with four active switches (Q_1, Q_2, Q_3, Q_4) and two phase inductors (L_1, L_2) to improve the static voltage gain between the two low-voltage dual sources (V_{ES1}, V_{ES2}) and the high-voltage dc bus (V_H) in the proposed converter. Furthermore, the additional C_B reduces the switch voltage stress of active switches and eliminates the need to operate at an extreme duty ratio. Furthermore, the three bidirectional power switches (S, S_{ES1}, S_{ES2}) displayed in Fig. 2 exhibit four-quadrant operation and are adopted to control the power flow between two low-voltage dual sources (V_{ES1}, V_{ES2})and to block either positive or negative voltage.

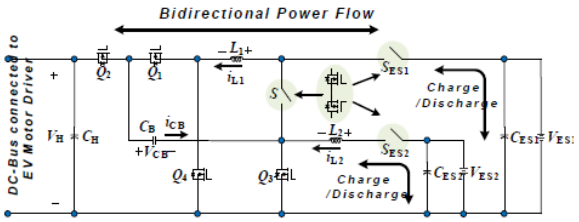

Fig. 2. Proposed BDC topology with dual-battery energy storage.

TABLE I
CONDUCTION STATUS OF DEVICES FOR DIFFERENT OPERATING MODES

Operating Modes	ON	OFF	Control Switch	Synchronous Rectifier (SR)
Low-voltage dual-source-powering mode (Accelerating, x_1=1, x_2=1)	S_{ES1}, S_{ES2}	S	Q_3, Q_4	Q_1, Q_2
High-voltage dc-bus energy-regenerating mode (Braking, x_1=1, x_2=1)	S_{ES1}, S_{ES2}	S	Q_1, Q_2	Q_3, Q_4
Low-voltage dual-source buck mode (ES1 to ES2, x_1=0, x_2=0)	S_{ES1}, S_{ES2}	Q_1, Q_2, Q_4	S	Q_3
Low-voltage dual-source boost mode (ES2 to ES1, x_1=0, x_2=0)	S_{ES1}, S_{ES2}	Q_1, Q_2, Q_4	Q_3	S
System shutdown	--	S_{ES1}, S_{ES2} Q_1, Q_2, Q_3, Q_4	--	--

This bidirectional power switch is actualized by means of two metal-oxide-semiconductor field-impact transistors (MOSFETs), pointing in inverse bearings, in arrangement association. To clarify the idea for the proposed converter, all the conduction statuses of the power gadgets engaged with every activity mode are shown in Table I. As needs be; the four working modes are outlined as pursues to improve understanding.

A. Low-Voltage Dual-Source-Powering Mode

Fig. 3(a) depicts the circuit schematic and steady-state waveforms for the converter under the low-voltage dual-source-powering mode. Therein, the switch S is turned off, and the switches (S_{ES1}, S_{ES2}) are turned on, and the two low-voltage dual sources (V_{ES1}, V_{ES2}) are supplying the energy to the dc-bus and loads. In this mode, the low-side switches Q_3 andQ_4 are actively switching at a phase-shift angle of 180°, and the high-side switches Q_1 andQ_2 function as the synchronous rectifier (SR). Based on the typical waveforms shown in Fig. 3(b), when the duty ratio is larger than 50%, four circuit states are possible (Fig. 4). In the light of the on/off status of the active switches and the operating principle of the BDC in low-voltage dual-source-powering mode, the

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operation can be explained briefly as follows.

a) State 1 [$t_0 < t < t_1$]: During this state, the interval time is $(1\text{-}D_u)T_{sw}$, switches Q_1, Q_3 are turned on, and switches Q_2, Q_4 are turned off. The voltage across L_1 is the difference between the low-side voltage V_{ES1} and the charge-pump voltage (V_{CB}), and hence i_{L1}decreases linearly from the initial value. In addition, inductor L_2 is charged by the energy source V_{ES2},

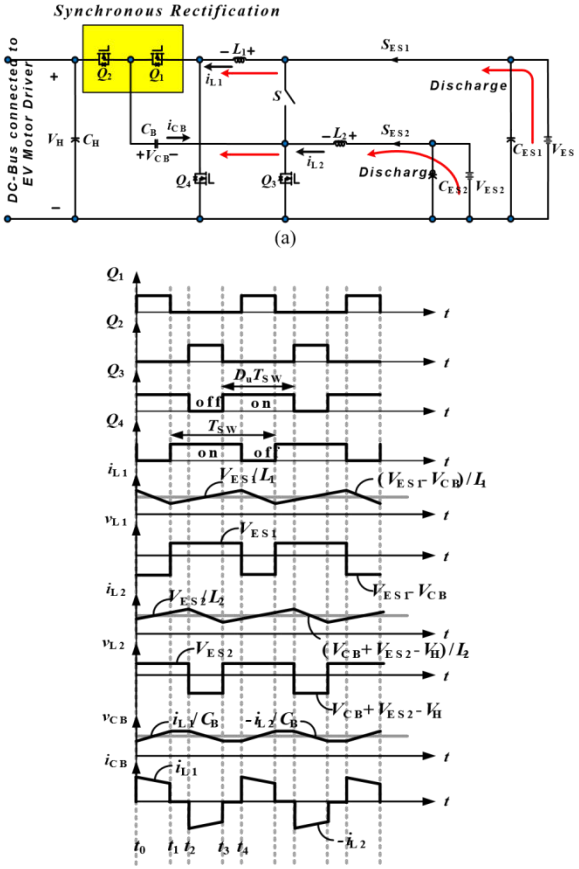
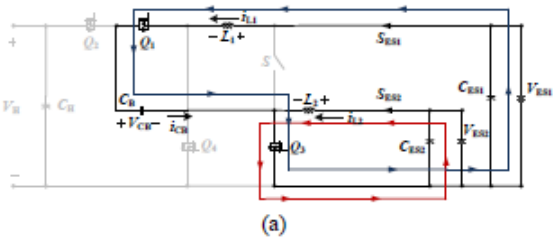


Fig. 3. Low-voltage dual-source-powering mode of the proposed BDC: (a) circuit schematic and (b) steady-state waveforms.



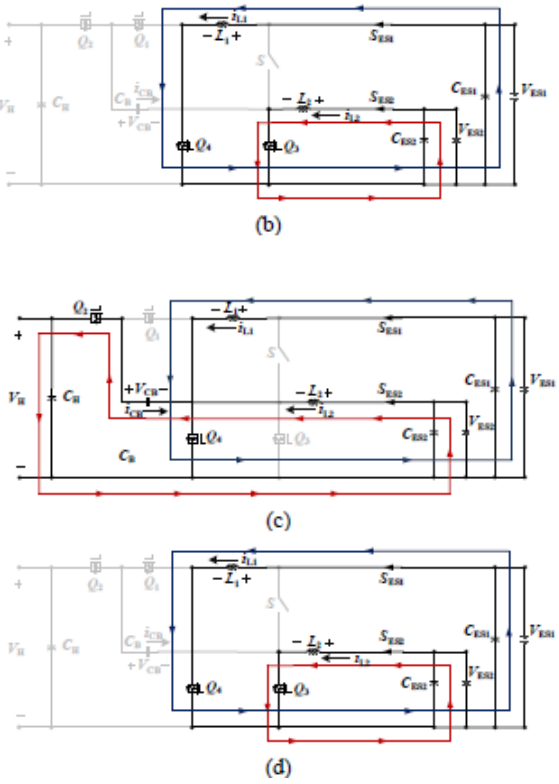


Fig. 4. Circuit states of the proposed BDC for the low-voltage dual-source-powering mode. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

Thereby generating a linear increase in the inductor current. The voltages across inductors L1 and L2 can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES2} - V_{CB}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2}$$

b) State 2 [$t_1 < t < t_2$]: During this state, the interval time is $(D_u\text{-}0.5)T_{sw}$; switches Q_3 and Q_4 are turned on; and switches $Q_1$and Q_2 are turned off. The low-side voltages V_{ES1} and V_{ES2} are located between inductors L_1 and L_2,respectively, thereby linearly increasing the inductor currents, and initiating energy to storage. The voltages across inductors L_1 and L_2 under state 2 can be denoted as

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$$L_1 \frac{di_{L1}}{dt} = V_{ES1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2}$$

c) **State 3 [t_2 < t < t_3]:** During this state, the interval time is $(1\text{-}D_u)T_{sw}$; switches Q_1 and $Q_3$are turned on, whereas switches Q_2 and $Q_4$are turned off. The voltages across inductors L_1 and L_2 can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{CB} + V_{ES2} - V_H$$

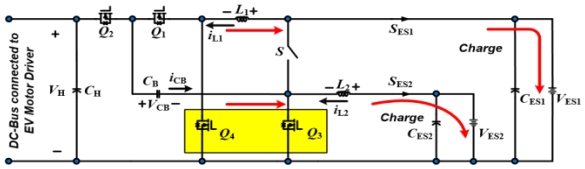
State 4 [t_3< t <t_4]: During this state, the interval time is $(D_u\text{-}0.5)T_{sw}$; switches Q_3 and Q_4 are turned on, and switches $Q_1$and Q_2 are turned off. The voltages across inductors L_1 and L_2

$$L_1 \frac{di_{L1}}{dt} = V_{ES1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2}$$

B. High-Voltage DC-Bus Energy-Regenerating Mode

In this mode, the active vitality put away in the engine drive is sustained back to the source during regenerative braking activity. The regenerative power can be a lot higher than what the battery can retain. Subsequently, the abundance vitality is utilized to charge the vitality stockpiling gadget. The circuit schematic and the enduring state waveforms of the BDC under the high-voltage dc transport vitality recovering mode are represented in Fig. 5.



Synchronous Rectification (a)

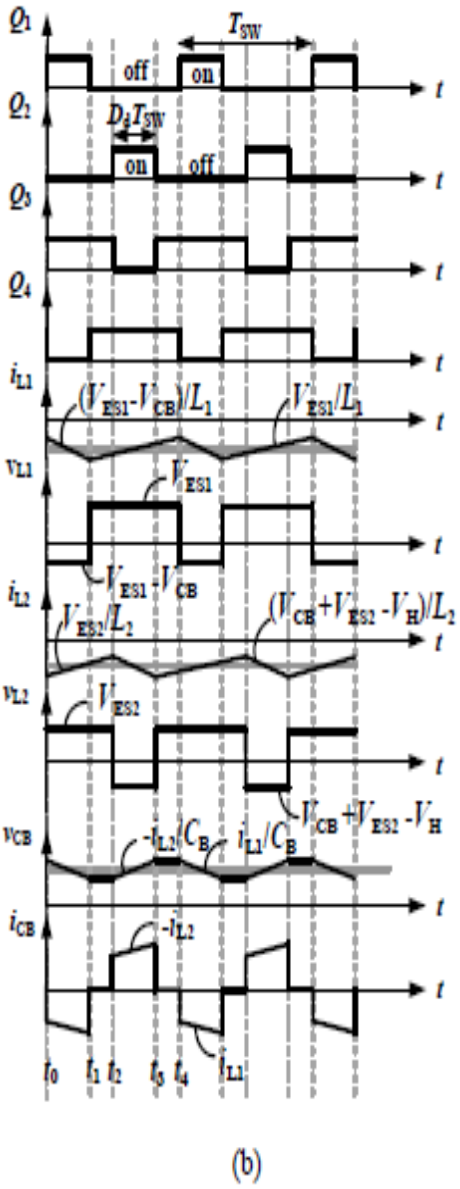
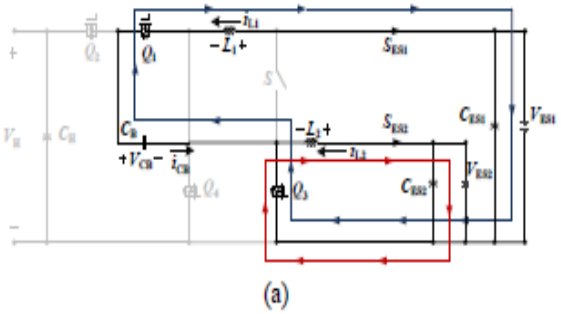


Fig. 5. High-voltage dc-bus energy-regenerating mode of the proposed BDC: (a) circuit schematic and (b) steady-state waveforms.



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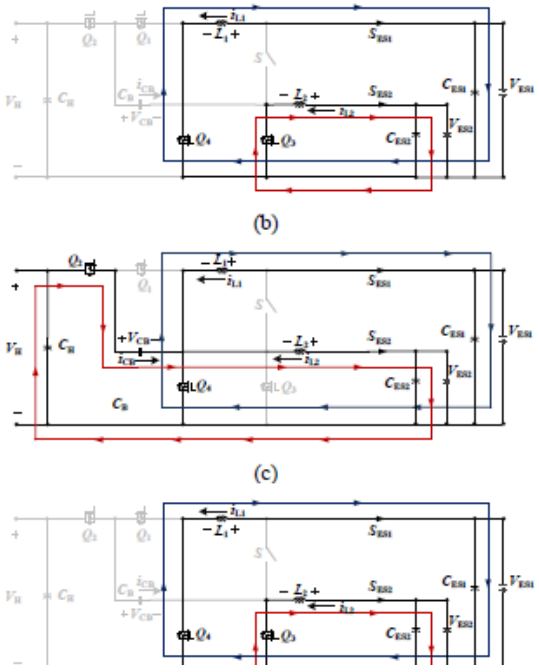

Fig. 6. Circuit states of the proposed BDC for the high-voltage dc-bus energy-regenerating mode. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

Therein, the current in the inductors is controlled by the active switches Q_1 and Q_2,which have a phase-shift angle of 180° and thereby direct theflow away from the dc-bus and toward the dual energy storage devices; the switches Q_3 and Q_4 function as the SR to improve the conversion efficiency.

On the basis of the steady-state waveforms shown in Fig. 5(b), when the duty ratio is below 50%, four different circuit states are possible, as shown in Fig. 6. In the light of the on-off status of the active switches and the operating principle of the BDC in high-voltage dc-bus energy-regenerating mode, the operation can be depicted briefly as follows.

a) **State 1 [$t_0 < t < t_1$]:** During this state, the interval time is D_dT_{sw}; switches Q_1 and $Q_3$are turned on, and switches Q_2 and Q_4 are turned off. The voltage across L_1 is the difference between the low-side voltage V_{ES1} and the charge-pump voltage V_{CB}; hence, the inductor current i_{L1}decreases linearly from the initial value. In addition, inductor L_2 is charged by the energy source V_{ES2}, which also contributes to the linear increase in the inductor current. The voltages across inductors L_1 and L_2 can be denoted as

$$L_2 \frac{di_{L2}}{dt} = V_{ES2}$$

b) **State 2 [$t_1 < t < t_2$]:** During this state, the interval time is $(0.5\text{-}D_d)T_{sw}$; switches Q_3 and $Q_4$are turned on, and switches Q_1 and Q_2 are turned off. The voltages across inductors $L_1$and $L_2$are the positive the low-side voltages V_{ES1} and V_{ES2}, respectively; hence, inductor currents $i_{L1}$and i_{L2}increase linearly. These voltages can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2}$$

c) **State 3 [$t_2 < t < t_3$]:** During this state, the interval time is D_dT_{sw}; switches Q_1 and $Q_3$are turned off, and switches Q_2 and Q_4 are turned on. The voltage across L_1 is the positive low-side voltage V_{ES1} and hence i_{L1}increases linearly from the initial value. Moreover, the voltage across L_2 is the difference of the high-side voltage V_H, the charge-pump voltage V_{CB}, and the low-side voltage V_{ES2}, and its level is negative. The voltages across inductors L_1 and L_2 can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} + V_{CB} - V_H$$

State 4 [$t_3 < t < t_4$]: During this state, the interval time is $(0.5\text{-}D_d)T_{sw}$; switches Q_3 and

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$Q_4$are turned on, and switches Q_1 and Q_2 are turned off. The voltages across inductors L_1 and L_2 can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2}$$

C. Low-Voltage Dual-Source Buck/Boost Mode

The circuit schematic for this mode, which involves the transfer of energy stored in the primary vitality stockpiling to the helper vitality stockpiling and the other way around is displayed in Fig. 7. In that, the topology is changed over into a solitary leg bidirectional buck-support converter. As appeared in Fig. 8, when the obligation cycle of the dynamic bidirectional switch S is controlled, the buck converter channels control from principle vitality stockpiling to the helper vitality stockpiling. On the other hand, when the obligation cycle of switch Q3 is controlled, control streams from the helper vitality stockpiling to principle vitality stockpiling, showing that the converter is working in lift mode, as delineated in Fig. 9.

III.STEADY-STATE ANALYSIS

In this section, we analyze the voltage gain, switch voltage stress, and uniform average current sharing characteristics of the proposed BDC when operating in a steady state.

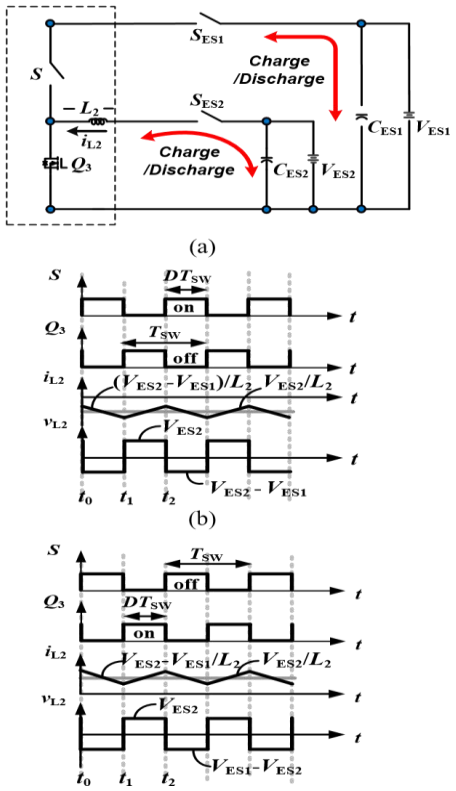

Fig. 7. Low-voltage dual-source buck/boost mode of the proposed BDC: (a) circuit schematic; (b) steady-state waveforms underbuck mode; (c) steady-state waveforms under boost mode.

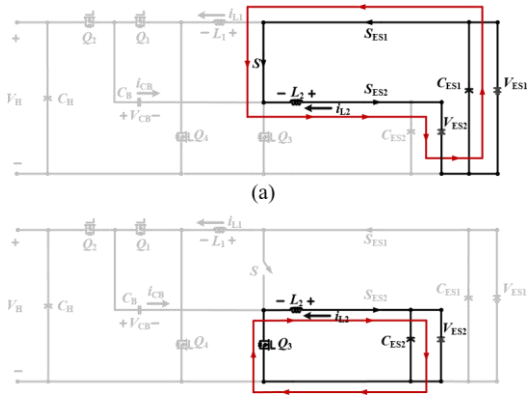

Fig. 8. Circuit states of the proposed BDC for the low-voltage dual-source buck mode. (a) State 1. (b) State 2.

A. Voltage Gain

The voltage gains of the proposed BDC can be derived by applying the principle of inductor volt-second balance to the different modes. To enhance simplicity and

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practicality, the equivalent series resistances (ESRs) of the inductors L_1 and L_2 have been substituted into the state equations as nonideal cases, and the parameters $R_{L1}=R_{L2}=R_L=50m\Omega$ are also given.

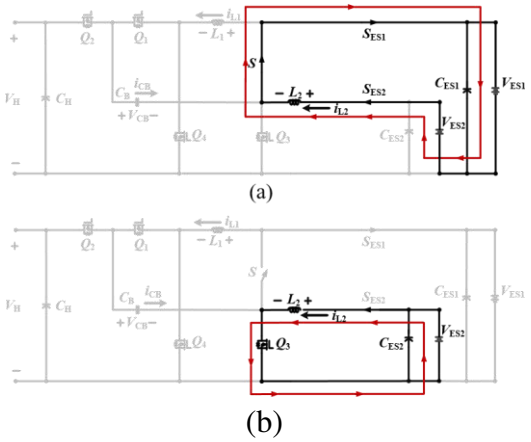

Fig. 9. Circuit states of the proposed BDC for the low-voltage dual-source boost mode. (a) State 1. (b) State 2.

1)Low-Voltage Dual-Source-Powering Mode

The relationship among the voltage gains of the three dc sources under steady-state operation are given by (17) and (18).

$$\frac{V_H}{V_{s2}}=\left[(k+1)-\frac{2V_{RL}}{V_{s2}}\right]\frac{1}{1-D_u}$$

$$\frac{V_H}{V_{s1}}=\left[\frac{k}{(k+1)}-\frac{2V_{RL}}{V_{s1}}\right]\frac{1}{1-D_u}$$

where V_{RL} is the voltage difference across the ESR of inductance, k is the ratio of $V_{s1}=V_{ES1}$ to $V_{s2}=V_{ES2}$, and $D_u$is the duty cycle of Q_3 and Q_4 and is >50%.

Using (17) and (18), the ideal static voltage gains of V_H/V_{s1} and V_H/V_{s2} can be expressed as (19) and (20).

$$\frac{V_H}{V_{s2}}=\frac{k+1}{1-D_u}$$

$$\frac{V_H}{V_{s1}}=\frac{k}{(1-D_u)(k+1)}$$

Accordingly, the relation between dc-bus voltage V_H and the dual-source voltages (V_{ES1}, V_{ES2}) is given by (21).

$$\frac{V_H}{V_{s1}+V_{s2}}=\frac{1}{1-D_u}\;;V_{s1}=kV_{s2}$$

High-Voltage DC-Bus Energy-Regenerating Mode

Under steady-state operation, the relationship among the voltage gains of the three dc sources are given by

$$\frac{V_{s1}}{V_H}=(D_d-\frac{2V_{RL}}{V_H})\frac{k}{k+1}$$

$$\frac{V_{s2}}{V_H}=(D_d-\frac{2V_{RL}}{V_H})\frac{1}{k+1}$$

where$D_d$is the duty cycle of Q_1 and Q_2 and is <50%.

From (22) and (23), the ideal static voltage gains of $V_{s1}/V_H$and $V_{s2}/V_H$are given as (24) and (25).

$$\frac{V_{s1}}{V_H}=\frac{D_d k}{k+1}$$

$$\frac{V_{s2}}{V_H}=\frac{D_d}{k+1}$$

Accordingly, the relation between the dual-source voltages (V_{ES1}, V_{ES2}) and the dc-bus voltage V_H is given by (26).

$$\frac{V_{s1}+V_{s2}}{V_H}=D_d\;;V_{s1}=kV_{s2}$$

Although these voltage gains are reduced by the ESR of the inductors under the nonideal situation, the parasitic effect is relatively small and thus the reduced voltage gain can be easily compensated for by increasing the duty control.

3) Low-Voltage Dual-Source Buck/Boost Mode

The relation between the two low-side voltages is given by (27).

$$\begin{cases}V_{ES2}-V_{RL2}=D_sV_{ES1}\;;(buck\;\;mode)\\ V_{ES1}=\dfrac{1}{1-D}(V_{ES2}-V_{RL2})\;;(boost\;\;mode)\end{cases}$$

In (27), D_s is the duty cycle of S for the energy transferred from the main energy

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storage to the auxiliary energy storage, whereas D is the duty cycle of Q_3 for the energy transferred from the auxiliary energy storage to the main energy storage. The relationship between the two low-side voltages without the effect of the ESR of inductors can be expressed as (28).

$$\begin{cases} V_{ES2} = D_s V_{ES1} ; (buck\ \ mode) \\ V_{ES1} = \dfrac{V_{ES2}}{1-D} ; (boost\ \ mode) \end{cases}$$

B. Charge-Pump Voltage

The voltage across the C_B under different modes can be derived as follows.

1) Low-Voltage Dual-Source-Powering Mode

$$V_{ES1} D_u + (V_{ES1} - V_{CB})(1-D_u) = 0$$

$$V_{CB} = \frac{V_{ES1}}{(1-D_u)}$$

2) High-Voltage DC-Bus Energy-Regenerating Mode

$$V_{ES1}(1-D_d) + (V_{ES1} - V_{ES2}) D_d = 0$$

$$V_{CB} = \frac{V_{ES1}}{D_d}$$

C.VOLTAGE STRESSES ON SWITCHES

To simplify the voltage stress analyses of the converter, the voltage ripples on the capacitors were ignored. As shown in Figs. 4, 6, 8, and 9, the maximum voltage stresses of the main power MOSFETs Q_1~Q_4 can be obtained directly as (33)-(36).

$$V_{Q_1,\max} = V_H$$

$$V_{Q_2,\max} = V_H - V_{CB}$$

$$V_{Q_3,\max} = V_H - V_{CB}$$

$$V_{Q_4,\max} = 2V_{ES1} - V_{CB}$$

D.Characteristic of Uniform Average Current Sharing

Through charge balance principles and the state-space averaging technique, the averaged state equations can be obtained directly as

$$\frac{2(i_{L1} - i_{L2})(1-D_u)}{C_B f_{SW}} = 0$$

$$\frac{2(i_{L1} - i_{L2}) D_d}{C_B f_{SW}} = 0$$

$$\frac{(i_{L1} + i_{L2}) R_H - V_H}{R_H C_H} = 0$$

where $I_H = V_{CH}/R_H$.

From (37)-(39), the following equation can be obtained:

$$i_{L1} = i_{L2} = \frac{i_H}{2}$$

From (40), the uniform average current sharing can be determined, independent of the values of the capacitors.

IV.CONVERTER CONTROL

Fig. 10(a) depicts the converter control structure, which consists of a vehicular strategic management level and the proposed BDC controller. The corresponding realized DSP flowchart for selecting operating modes of the proposed BDC is also shown in Fig. 10(b) for reference.The strategic management level involves an electrical power demand estimation and contains a vehicular power and voltage management unit. The global results of the management must maximize the use of the source that best suits the powertrain power demand, fulfilling the driver and route requirements [21, 25-33]. In FCV/HEV power systems (Fig. 1), the dc-bus voltage of the driving inverter is regulated and powered by the FC stack through a dc-dc converter. Hence, instead of controlling the converter output voltage of each operation mode, the inductor current i_{L1} or i_{L2} is detected and compared with the reference current to control the power flow as shown in Fig. 10(a). In the converter control structure, the vehicular energy and

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power and voltage management unit selects the BDC mode according to the operating conditions of the vehicle, such as power demand of different driving state (P_{dem})and the dual-source voltages (V_{ES1}, V_{ES2}). It then selects the appropriate current references $i_{L1,ref}$ or $i_{L2,ref}$ that can control the active switches (S, Q_1~Q_4) with proportional integral (PI) or more advanced methods. Notably, in spite of it is not easy to choose the optimal parameter of PI controller, the advantages of zero steady-state error and capability of noise filtering, making PI control the most widely used industry algorithm. Furthermore, referring to Table I, two switch selector (x_1, x_2) of BDC controller can be defined for various operating modes. The pulsed-width-modulation (PWM) switching scheme converts the duty cycle determined by different switch selector statuses into gate control signals for the power switches.

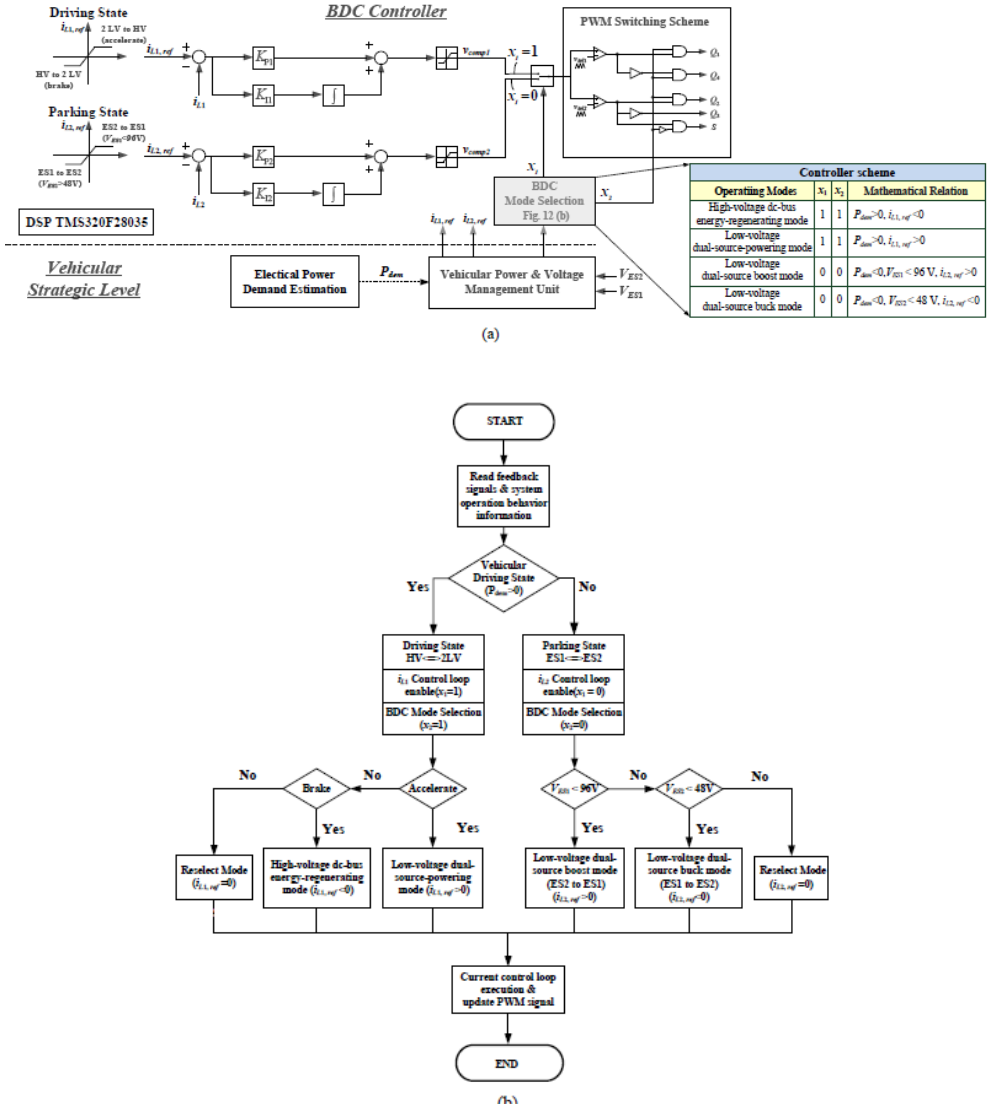

Fig. 10. (a) Block diagram of the closed-loop control scheme; (b) realized DSP flowchart for various operating modes of the proposed BDC.

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As Fig. 10(a) displays, the current reference $i_{L1,ref}$ is used to control the bidirectional power flow between the low-voltage dual-source and the high-voltage dc-bus (i.e., 2 LV to HV or HV to 2 LV). In either case, the average inductor current$i_{L2}$is equal to the controlled average inductor current i_{L1} because of the inherent uniform average current sharing in the proposed BDC topology. By contrast, the current reference $i_{L2,ref}$ is used to control the power flow between the main energy storage and the auxiliary energy storage (i.e., ES1 to ES2 or ES2 to ES1).The procedure of mode switching is shown in Fig. 10(b) and it is depicted below. First of all, when vehicle is in driving state (P_{dem}>0), the controller is i_{L1} control loop (x_1=1), and the controlled switches as shown in Table I (vehicle is accelerating($i_{L1,ref}$>0, HV to 2 LV) or braking ($i_{L1,ref}$<0, 2 LV to HV)). If neither of the two situations, it will execute reselect mode to process the next judgement of mode switching. Additionally, when vehicle is in parking state (P_{dem}<0), the controller is i_{L2} control loop (x_1=0), and controlled switches as shown in Table I. In this state, the judgement of mode switching depends on the voltage of V_{ES1} (96 V) and V_{ES2} (48 V). If V_{ES1}<96 V, the mode is low-voltage dual-source boost mode ($i_{L2,ref}$>0, V_{ES2} to V_{ES1}). When V_{ES2}<48 V, the mode is low-voltage dual-source buck mode ($i_{L2,ref}$<0, V_{ES1} to V_{ES2}). If both situations do not be satisfied, it executes reselect mode to process the next

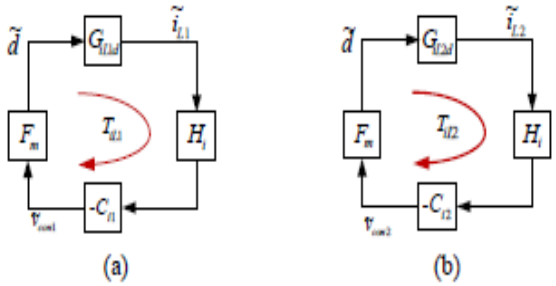

Fig. 11. Block diagram of the closed-loop control scheme for (a) the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes; (b) the low-voltage dual-source buck/boost mode.

judgement of mode switching. Only two closed-loop controllers were developed to control the four power flow conditions based on the average model of the proposed converter derived by using the state-space averaging technique. Fig. 11(a) shows the closed-loop control block diagram that is compatible with both low-voltage dual-source-powering boost mode (i.e., 2 LV to HV) and high-voltage dc-bus energy-regenerating mode (i.e., HV to 2 LV); the closed-loop control block diagram displayed in Fig. 11(b) is compatible with the low-voltage dual-source buck/boost mode (i.e., ES1 to ES2 or ES2 to ES1).In Fig. 11, F_M represents the constant gain of the PWM generator; G_{iL1d}denotes the transfer function, which converts the duty cycle to inductor current i_{L1}; $G_{iL2d}$is the transfer function from duty cycle to inductor current i_{L2}; C_{i1} and C_{i2} represent the transfer function of inductor current controllers, and H_i is the sensing gain of the current sensor.

To design the closed-loop controller and simplify the mathematics of the proposed BDC, the PSIM© circuit model is built under the following three assumptions: 1) power switches and diodes are ideal; 2) equivalent series resistances of all inductors

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and capacitors of the converter are considered to obtain a relatively precise dynamic model; and 3) the converter is operated under a continuous conduction mode. In the PSIM© circuit model, the adopted circuit parameters are L_1=L_2=250 μH, C_B=10 μF, C_H =1880 μF, C_{ES1}=C_{ES2}=400 μF, the ESR of inductances R_{L1}=R_{L2}=R_L=50 mΩ and ESR of capacitances R_{CB}=20 mΩ, R_{ES1}=R_{ES2}=50 mΩ, and line resistances R_{ES1}=12 mΩ and R_{ES2}=6 mΩ. Based on these assumptions, the design of the two closed-loop controllers are illustrated in the following sections.

A. Controller for Low-Voltage Dual-Source-Powering and High-Voltage DC-Bus Energy-Regenerating Modes

Under these two modes, the open-loop gain of the current loop of the proposed BDC can be derived as

TiL1 □F G HCm iL1d i i1 (41) where F_M=1/100, H_i=1.

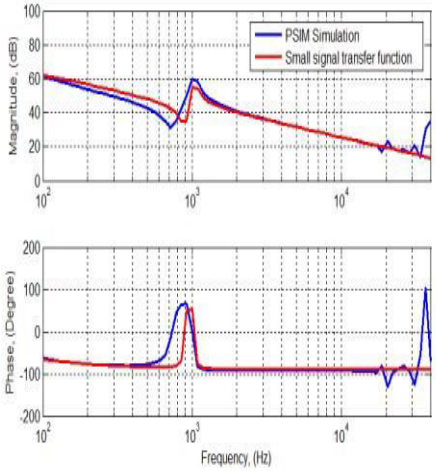

Fig. 12. Loop gain frequency responses of uncompensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes.

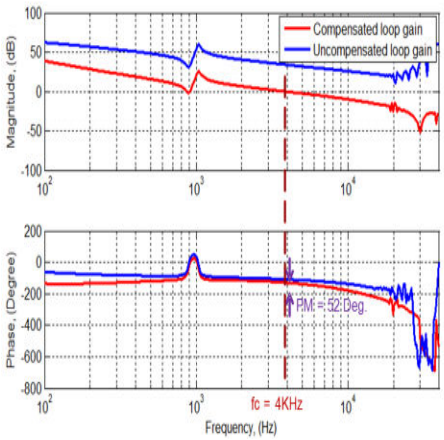

Fig. 13. Loop gain frequency responses of compensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes.

To simply the derivation, we assume that the dc-bus voltage V_H and the dual energy source voltage (V_{ES1}, V_{ES2}) are constant; beside, the key circuit parameters (C_B, L_1, L_2, R_{CB}, R_{L1}, R_{L2}) are used to derive the small-signal transfer function $G_{iL1d}$from the duty cycle to the inductor current i_{L1}, as (42). Substituting the above-mentioned circuit parameter values into (42), the numerical result can be expressed by third-order transfer functions as shown in (43).

To check the correctness, Fig. 12 shows the fitting curves made by Matlab© and PSIM© simulation software, and the results are closely between each other. Furthermore, in Fig. 12, the observable resonant behavior around 1-kHz is caused by three poles and two zeros that induced from the circuit parameters (C_B, L_1, L_2). The corresponding current controllers of the proposed converter under both low-voltage dual-source-powering and high-voltage dc-bus energy-regenerating modes are selected as

$$T_{iL1} = F_m G_{iL1d} H_i C_{i1}$$

where F_M=1/100, H_i=1.

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Fig. 13 shows the loop-gain frequency response of the compensated current loop in low-voltage dual-source-powering and high-voltage dc-bus energy-regenerating modes, under full-load conditions; this design results in a phase margin of 52° and a crossover frequency of approximately 4 kHz.

$$G_{iL1d}=\frac{\hat{i}_{L1}}{\hat{d}}=\frac{(L_1C_BV_{CB})s^2+(L_1i_LR_{CB}+R_LC_BV_{CB}+C_BV_{CB}R_{CB}D_u)s+(1\text{-}D_u)V_H+(i_LR_{CB})(R_L+R_{CB}D_u)}{C_BL_1(L_1R_L+R_{CB}+R_{CB}D_u)s^3+C_BL_1[R_L^{\,2}+R_{CB}R_L+R_{CB}D_u(R_{CB}D_u+R_L+2R_{CB})]s^2+2L_1(1\text{-}D_u)^2s+2(1\text{-}D_u)^2(R_L+R_{CB})}$$

$$G_{iL1d}=\frac{(1.53\times10^{-6})s^2+(3.76\times10^{-4})s+48.2}{(1.28\times10^{-12})s^3+(6.36\times10^{-10})s^2+(5.38\times10^{-5})s+0.016}$$

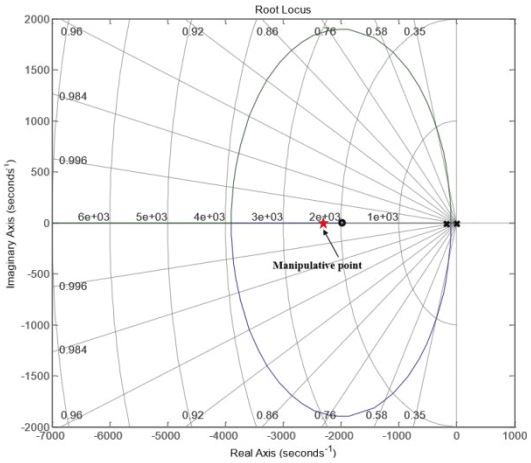

Fig. 14. Root locus of compensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes.

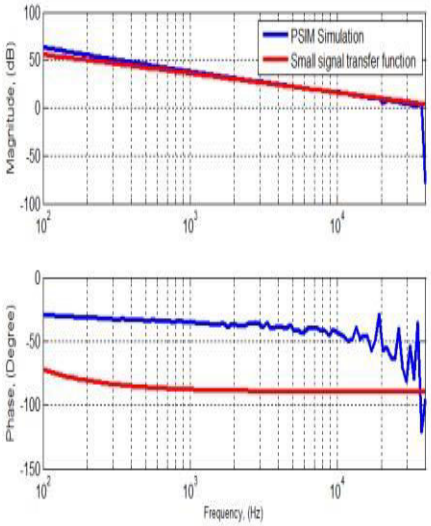

Fig. 15. Loop gain frequency responses of uncompensated current loop in the low-voltage dual-source buck/boost mode.

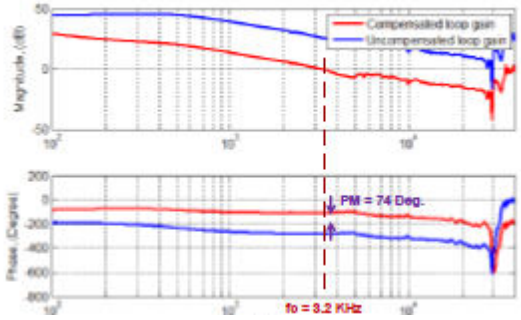

Fig. 16. Loop gain frequency responses of compensated current loop in the low-voltage dual-source buck/boost mode.

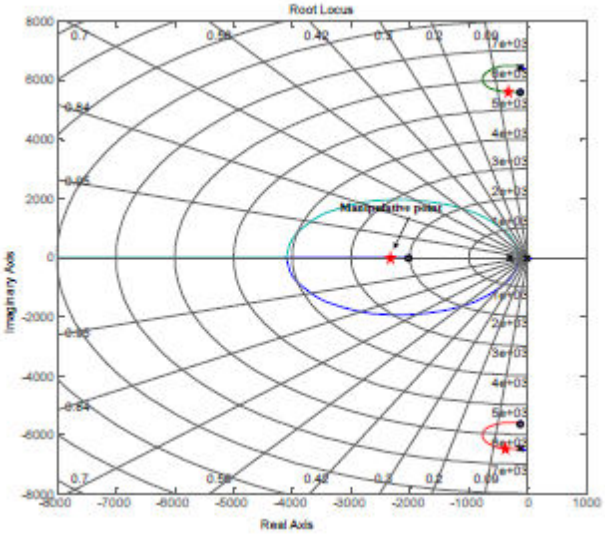

Fig. 17. Root locus of compensated current loop in the low-voltage dual-source buck/boost mode.

Fig. 14 shows the root locus of compensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes. The result of compensation has four poles and three zeros that all on the left side of imaginary axis baseline, by contrast, if there is any pole or

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zero point on the right side of imaginary axis baseline, the designed controller will be unstable. As a result, the controller is stable and the manipulative point is pinpointed on Fig. 14.

B. Controller for Low-Voltage Dual-Source Buck/Boost Mode

In this mode, the open-loop gain of the current loop of the proposed BDC can be derived as

$$T_{iL2} = F_m G_{iL2d} H_i C_{i2}$$

The small-signal transfer function $G_{iL2d}$from the duty cycle to the inductor current i_{L2} can be represented as follows.

$$G_{iL2d} = \frac{\hat{i}_{L2}}{\hat{d}} = \frac{V_{ES1}}{sL_2 + R_{L2}} = \frac{96}{2.5\times10^{-4}s + 5\times10^{-2}}$$

To check the correctness, Fig. 15 shows the fitting curves made by Matlab© and PSIM© simulation software, and the results are closely each other. The corresponding current controllers of the proposed converter in low-voltage dual-source buck/boost mode are selected using (47) below.

$$C_{i2} = 0.05 \cdot (1 + \frac{2000}{s})$$

Fig. 16 illustrates the loop-gain frequency response of the compensated current loop in low-voltage dual-source buck/boost mode, under full-load conditions; this design results in a phase margin of 74° and a crossover frequency of approximately 3.2 kHz.

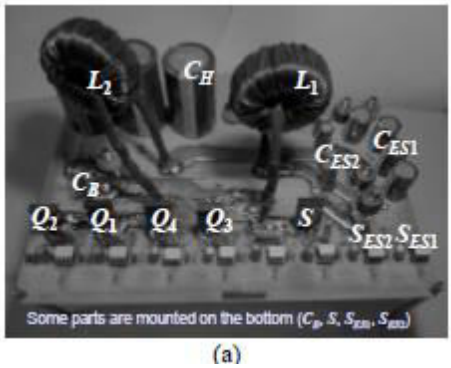
Fig. 17 shows the root locus of compensated current loop in the low-voltage dual-source buck/boost mode. The result of compensation has two poles and one zeros that all on the left side of imaginary axis baseline, by contrast, if there is any pole or zero point on the right side of imaginary axis baseline, the designed controller will be unstable. As a result, the controller is stable and the manipulative point is pinpointed on Fig. 17.

V.SIMULATION AND EXPERIMENTAL RESULTS

Simulations and experiments were conducted to verify the performance of the proposed model. A 1 kW laboratory prototype was constructed according to the specifications and parameters presented in Table II. A photograph of the realized BDC prototype and the test bench are shown in Fig. 18. DC voltage sources and electric loads were substituted for the main energy storage and the auxiliary energy storage. The system developed in this study included two loads for the high-voltage dc-bus energy-regenerating mode and two sources for the low-voltage dual-source-powering mode. In this experimental

TABLE II: SPECIFICATIONS AND PARAMETERS OF THE PROTOTYPE SYSTEM

Specifications	
ES1 voltage	V_{ES1}: 96 V
ES2 voltage	V_{ES2}: 48 V
DC-bus voltage	V_H: 430 V
Output power	P_o: 1 kW
Switching frequency	f_{SW}: 40 kHz
Parameters	
Inductors	L_1, L_2: CH330060, 250 uH
High-side capacitor	C_H: aluminum capacitor, 1880 μF
Low-side capacitor	C_{ES1}: aluminum capacitor, 400 μF C_{ES2}: aluminum capacitor, 400 μF
Charge-pump capacitor	C_B: film capacitor, 10 μF
Switches	S, S_{ES1}, S_{ES2}: IXFK360N15T2 Q_1, Q_4, Q_2, Q_3: W45NM60



(a)

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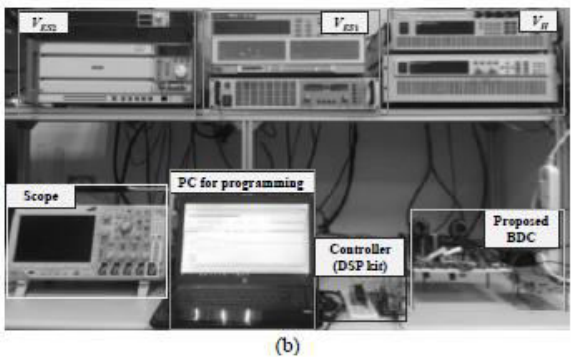


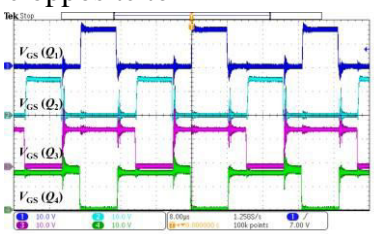
(b)

Fig. 18. Photograph of the realized BDC prototype and the test bench system. (a) BDC prototype; (b) test bench system. setup, a general purpose Texas Instrument Piccolo DSP kit on a TMS320F28035 fixed-point 32-bit/60MHz CPU was used to generate the PWM control signals.

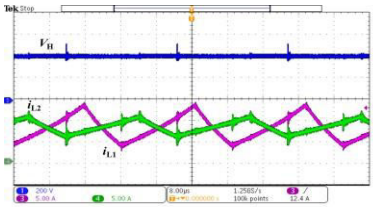
PSIM© simulation software was also applied to verify the feasibility of the proposed BDC. Fig. 19 illustrates that both sources powered the traction motor, thereby boosting the two input voltages. Therefore, both sources contributed to the dc-bus voltage V_H of 430V.

The observations on the power flow from the dc-bus to the main energy storage and the auxiliary energy storage are detailed in Fig. 20. Inductor currents i_{L1} and i_{L2}flowed in a direction opposite that of the input power. The low-side output voltages V_{ES1} and V_{ES2} were approximately 96V and 48V, respectively.

Fig. 21 illustrates the experimental waveforms for the low-voltage dual-source buck mode and the boost mode. The directions of the inductor currents in Fig. 21(a) are opposite to

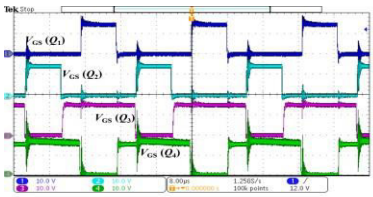


(a)

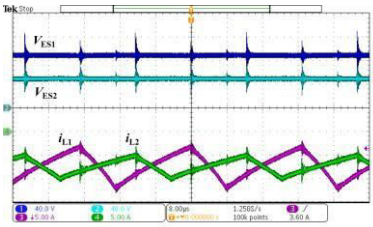


(b)

Fig. 19. Measured waveforms for low-voltage dual-source-powering mode: (a) gate signals; (b) output voltage and inductor currents.

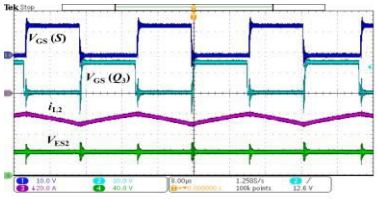


(a)

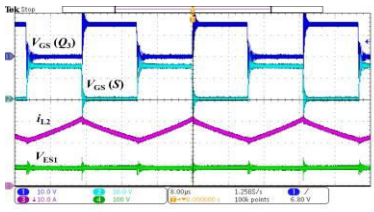


(b)

Fig. 20. Measured waveforms for high-voltage dc-bus energy-regenerating mode: (a) gate signals; (b) output voltage and inductor currents.



(a)



(b)

Fig. 21. Measured waveforms of gate signals, output voltage and inductor currents for the low-voltage dual-source buck/boost mode: (a) buck mode; (b) boost mode.

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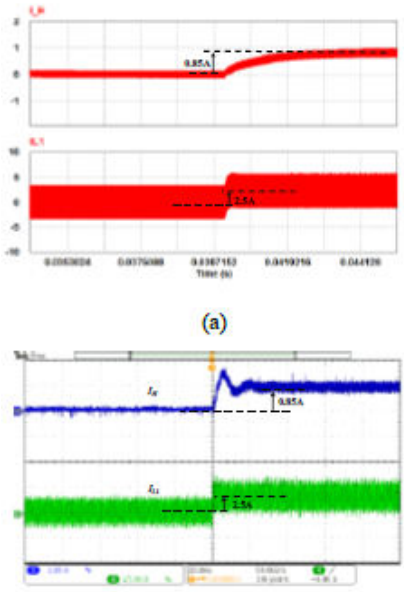

Fig. 22. Waveforms of controlled current step change in the low-voltage dual-source-powering mode: (a) b y simulation; and (b) by measurement. (i_H is changed from 0 to 0.85 A; i_{L1} is changed from 0 to 2.5 A; Time/Div=20 ms/Div)

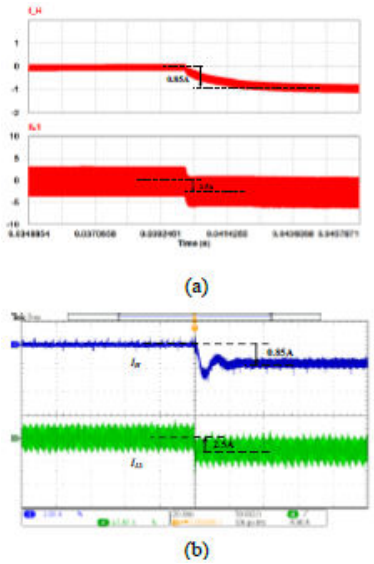

Fig. 23. Waveforms of controlled current step change in the high-voltage dc-bus energy-regenerating mode: (a) by simulation; and (b) by measurement. (i_H is changed from 0 to -0.85 A; i_{L1} is changed from 0 to -2.5 A; Time/Div=20 ms/Div)

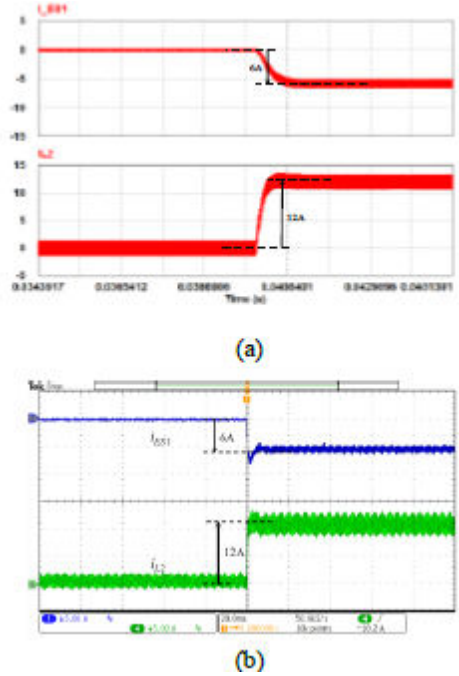

Fig. 24. Waveforms of controlled current step change in the low-voltage dual-source boost mode: (a) by simulation; and (b) by measurement. (i_{ES1} is changed from 0 to -6 A; i_{L2} is changed from 0 to 12 A; Time/Div=20 ms/Div)

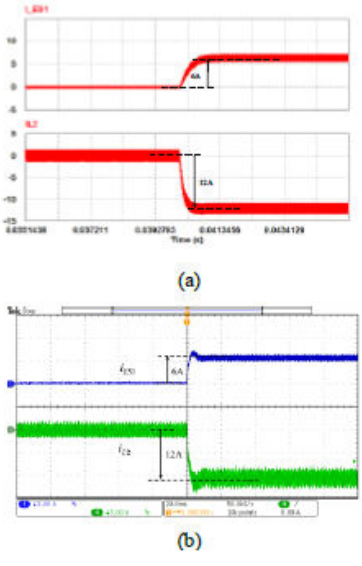

Fig. 25. Waveforms of controlled current step change in the low-voltage dual-source buck mode: (a) by simulation; and (b) by measurement. (i_{ES1} is changed from 0 to 6 A; i_{L2} is changed from 0 to 12 A; Time/Div=20 ms/Div)

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that of those in Fig. 20(b), verifying the ability of the model to conduct bidirectional power flow between the main energy storage and the auxiliary energy storage. In summary, all the experimental results were very similar to the simulation results, and both sets of results were consistent with the predictions of the steady-state analyses.

Figs. 22 and 23 present the waveforms of a controlled current step change for the prototype system in the low-voltage dual-source-powering mode and in the high-voltage dc-bus energy-regenerating mode, respectively. As demonstrated in Fig. 22, the high-side current i_H and the inductor current i_{L1} were manipulated to deliver 360-W power

from the low-side dual sources to the high-side dc-bus. The negative current waveforms displayed in Fig. 23 indicate that the power flow was successfully reversed. Figs. 24 and 25 illustrate the waveforms of a controlled current step change for the prototype system in the low-voltage dual-source boost mode and in the low-voltage dual-source buck mode, respectively. As demonstrated in Fig. 24, the high-side current i_{ES1} and the inductor current i_{L2} were manipulated to deliver 576 W power between low-voltage dual-source. The negative current waveforms displayed in Fig. 25 indicate that the power flow was successfully reversed.

The current of main energy storagei_{ES1} and the inductor current i_{L2} were manipulated to deliver 580 W of power from the

Table III
PERFORMANCE COMPARISON AMONG A VARIETY OF CONVERTERS.

Items	Topology				
	[25]	[34]	[35]	[36]	Proposed
Switching control structure	single-phase	single-phase	single-phase	four-phase	two-phase
Bidirectional power flow	Yes	No	No	Yes	Yes
Output ripple	Medium	High	Low	Low	Low
Number of PWM controlled switches	6	5	4	8	6
Passive components	5	7	15	4	6
Realized prototype power rating	5 kW	1 kW	90 W	5 kW	1 kW
Maximum conversion efficiency	91.5%	94%	93%	95%	97.25%
High-side voltage	300 V	400 V	540 V	200 V	430 V
Low-side voltages	V_{ES1}: 125 V V_{ES2}: 144 V	V_{ES1}:30~50 V V_{ES2}: 50~100 V	V_{ES1}: 240~300 V V_{ES2}: 240~300 V	V_{ES1}: 42~63 V V_{ES2}: 48 V	V_{ES1}: 96 V V_{ES2}: 48 V

the auxiliary energy storage to the main energy storage (Fig. 24). The negative current waveforms shown in Fig. 25 further confirm that power flow was successfully reversed. In summary, the experimental results presented in Figs. 22-25 closely patterned the simulation results. The efficiency of the proposed BDC under different load conditions was examined and the results are presented in Fig. 26. Its efficiency under 50-W to 1 kW experimental loads was above 88% for all modes of operation. Its conversion efficiency was measured using a precise digital power meter (Yokogawa-WT310).

As shown in Fig. 26, the highest conversion efficiencies of the high-voltage dc-bus energy-regenerative buck mode, low-voltage dual-source-powering mode, low-voltage dual-source boost mode (ES2 to ES1), and low-voltage dual-source buck mode (ES1 to ES2) were 97.25%, 95.32%, 95.76%, and 92.67%, respectively.

Performance comparisons of the proposed BDC and models presented in related studies are summarized in Table III. The models in [34] and [35] possessed a higher

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number of passive components than the proposed converter does. Moreover, the models therein do not possess bidirectional power flow capabilities. Although the converters in [25] and [36] featured bidirectional power flow, their corresponding maximum conversion efficiencies were lower than that of the converter proposed in this study. Additionally, the voltage conversion ratio of the proposed BDC is higher than that of the models presented in [25] and [34-36].

For convenience, numerous active-power MOSFETs were adopted in the proposed BDC. However, only six power MOSFETs were switched using PWM-controlled signals. The power MOSFETs (S_{ES1} and S_{ES2}) can be replaced with suitable breakers. Moreover, several commercial ES1or ES2 packs include an on–off control function for shutting down the energy storage device; hence, the MOSFETs for S_{ES1} and S_{ES2} can be removed in future studies. In summary, compared with the works announced in [25] and [34-36], the proposed BDC topology achieved higher conversion efficiency, and

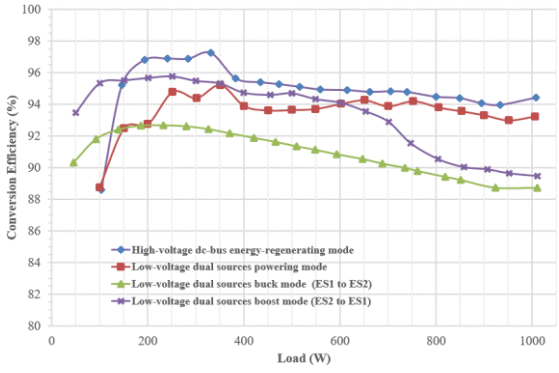

Fig. 26. Efficiency of the proposed BDC in different modes of operation under different load conditions.

driving loss, and the rest of all components such as capacitors and inductors only take conductive loss as a consideration.The losing estimation of switches include bidirectional power flow, as well as lower output current and voltage ripples under 1 kW power loads. Furthermore, the price–performance ratio of the proposed BDC is higher than that of the aforementioned announced works.

VI.POWER LOSS ANALYSIS

For further consideration for increasing the power rating of the proposed converter, the resulting loss breakdown charts are depicted in Figs. 27 and 29 as reference. Through estimated loss analysis of all components on four modes, it can be more understand that the influence of each component loss to converted efficiencies at different modes. Moreover, both situation of rising temperature and limitation of voltage or current stress are the major factor to damage components. Additionally, power loss estimation could be as reference before deciding specification of components, helping us to enhance the efficiencies of BDC. For simplicity the power loss estimation of switches include switching, conductive and

switching, conductive and driving loss, and the rest of all components such as capacitors and inductors only take conductive loss as a consideration.

A. Loss Analysis for Low-Voltage Dual-Source-Powering and High-Voltage DC-Bus Energy-Regenerating Modes

As shown in Fig. 27(a) and Fig. 27(b), the majority of loss is focus on inductors. The reason is both $I_{L1(rms)}$ and $I_{L2(rms)}$ are larger lead to substantial conductive loss. The only way to reduce conductive loss of inductors is to choose relatively lower equivalent of ESR. In addition, the loss and highest temperature of Q_4 is more than other switches because the conducted time is the longest and the $I_{Q4(rms)}$ is the biggest. By

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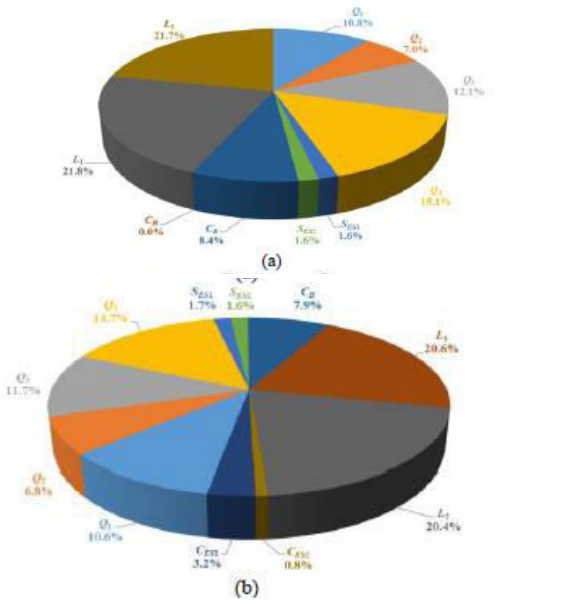


Fig. 27. Loss breakdown charts for (a) low-voltage dual-source-powering mode; and (b) high-voltage DC-Bus energy-regenerating modes.

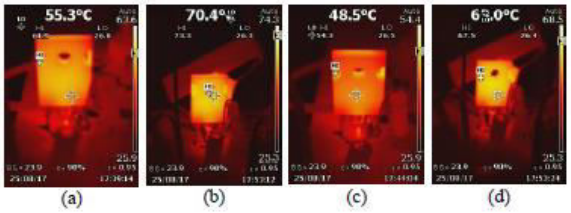


Fig. 28. Thermal image for low-voltage dual-source-powering mode: (a) Q_2 (b) Q_4; for high-voltage DC-Bus energy-regenerating mode: (c) Q_2 (d) Q_4.

Fig. 29. Loss breakdown charts for (a) low-voltage dual-source boost mode; and (b) low-voltage dual-source boost mode.

contrast, the loss and highest temperature of Q_2 is the smallest because conducted time is the shortest and the $I_{Q2(rms)}$ is the smallest. As shown in Fig. 28, when proposed converter is operated at low-voltage dual-source-powering mode, the loss and temperature of both Q_4 and Q_2 would be significantly higher than high-voltage DC-Bus energy-regenerating mode. The results in the measured efficiency of low-voltage dual-source-powering mode are lower than

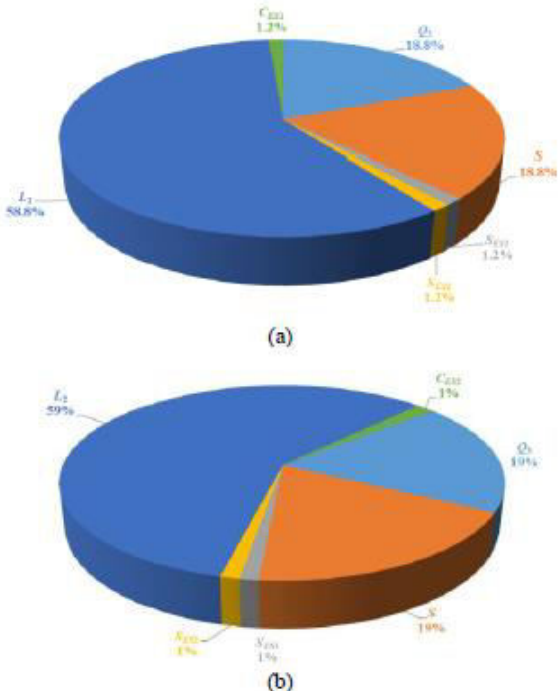
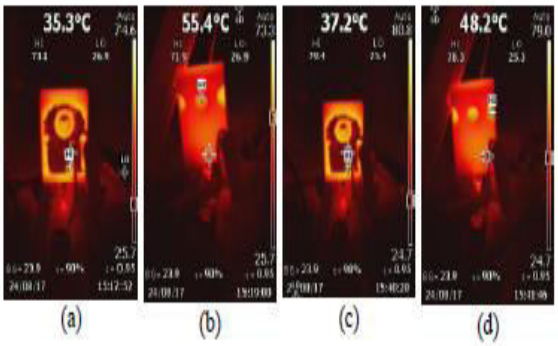


Fig 30. Thermal image for low-voltage dual-sourceboost mode: (a) Q_3 (b) S; for low-voltage dual-sourcebuck mode: (a) Q_3 (b) S.



that of high-voltage DC-Bus energy-regenerating mode.As shown in Fig. 29(a) and Fig. 29(b), the majority of loss is consumed on inductors. The reason is $I_{L2(rms)}$ is biggest lead to substantial conductive loss. The only way to reduce conductive loss of inductors is to choose relatively lower equivalent of ESR. In addition, the loss of Q_3 and S are equivalent and their highest temperature are closed because $I_{Q3(rms)}$ and $I_{S(rms)}$ are quietly closed and their

duty are basically the same. As shown in Fig. 30, when proposed converter is operated at low-voltage dual-source buck mode, the loss and temperature of both Q_3 and S would be significantly higher than low-voltage dual-source boost mode.The results in the measured efficiency of low-voltage dual-source buck mode are lower than that of low-voltage dual-source boost mode. It should be noticed that all images Fig. 28 and Fig. 30 was measured using an industrial thermal camera (Fluke-TiS75). It has automatic focus function to catch the highest temperature point of the device for the reliable results.

VII.CONCLUSIONS

Another BDC topology was displayed to interface double battery vitality sources and high-voltage dc transport of various voltage levels. The circuit setup, activity standards, examinations, and static voltage increases of the proposed BDC were talked about based on various methods of intensity move. Recreation and exploratory waveforms for a 1 kW model framework featured the presentation and plausibility of this proposed BDC topology. The most noteworthy transformation efficiencies were 97.25%, 95.32%, 95.76%, and 92.67% for the high-voltage dc-transport vitality regenerative buck mode, low-voltage double source-fueling mode, low-voltage double source support mode (ES2 to ES1), and low-voltage double source buck mode (ES1 to ES2), individually. The outcomes show that the proposed BDC can be effectively connected in FC/HEV frameworks to deliver half and half power design (has been protected [37]).

REFERENCES

1) M. Ehsani, K. M. Rahman, and H. A. Toliyat, "Propulsion system design of electric and hybrid vehicles," IEEE Transactions on industrial electronics, vol. 44, no. 1, pp. 19-27, 1997.
2) Emadi, K. Rajashekara, S. S. Williamson, and S. M. Lukic, "Topological overview of hybrid electric and fuel cell vehicular power system architectures and configurations," IEEE Transactions on Vehicular Technology, vol. 54, no. 3, pp. 763-770, 2005.
3) Emadi, S. S. Williamson, and A. Khaligh, "Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems," IEEE Transactions on Power Electronics, vol. 21, no. 3, pp. 567-577, 2006.
4) E. Schaltz, A. Khaligh, and P. O. Rasmussen, "Influence of battery/ultracapacitor energy-storage sizing on battery lifetime in a fuel cell hybrid electric vehicle," IEEE Transactions on Vehicular Technology, vol. 58, no. 8, pp. 3882-3891, 2009.
5) P. Thounthong, V. Chunkag, P. Sethakul, B. Davat, and M. Hinaje, "Comparative study of fuel-cell vehicle hybridization with battery or supercapacitor storage device," IEEE transactions on vehicular technology, vol. 58, no. 8, pp. 3892-3904, 2009.
6) Chan, A. Bouscayrol, and K. Chen, "Electric, hybrid, and fuel-cell vehicles: Architectures and modeling," IEEE transactions on vehicular technology, vol. 59, no. 2, pp. 589-598, 2010.
7) Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art," IEEE transactions on Vehicular Technology, vol. 59, no. 6, pp. 2806-2814, 2010.

8) K. Rajashekara, "Present status and future trends in electric vehicle propulsion technologies," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 1, no. 1, pp. 3-10, 2013.
9) C.-M. Lai, Y.-C. Lin, and D. Lee, "Study and implementation of a two-phase interleaved bidirectional DC/DC converter for vehicle and dc-microgrid systems," Energies, vol. 8, no. 9, pp. 9969-9991, 2015.
10) C.-M. Lai, "Development of a novel bidirectional DC/DC converter topology with high voltage conversion ratio for electric vehicles and DC-microgrids," Energies, vol. 9, no. 6, p. 410, 2016.