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REDUCED CARRIER PWM SYSTEM WITH UNITED LOGICAL FOR REDUCED SWITCH COUNT MULTILEVEL INVERTERS

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Abstract: The imperative decline inswitch check ofsymmetrical/uneven reduced switch count amazed inverters(RSCMLI) topologieshas changed the action of inverter with the ultimate objective that the standard conveyor based heartbeat width change (PWM) plans, for instance, level-moved PWM and stage moved PWM canno more recognize them. To controlthese RSC-MLItopologies, diminished transporter PWMplans with balanced trading method of reasoning expanded increasingly observable quality. These plans incorporate sensible reliable enunciations to comprehend the trading states oftheinverter. Regardless, these reasonable explanations vary with topological strategy and numberof levels. Likewise, these plans producehigh complete consonant bending (THD) in linevoltages. Along these lines, toimprove the line-voltageTHD and entirety up the trading reason, a balanced diminished conveyor PWMplot with bound together reliable explanations is shown here. The proposed PWMplan is really generous forany topology and canbe adequately flexible toanynumberoflevels in the inverters. To endorse the utilization oftheproposedPWM to control anyRSC-MLI, preliminary examinations of various amiss RSC-MLI topologies with the proposed PWMplan are finished. Further,to affirm the pervasiveness oftheproposed arrangement with respect to THD, multifaceted design, flexibility, and estimation load, its introduction is differentiated and conveyor based PWM plans point by point in the composition.

1. INTRODUCTION

The interest for diminishing the sizeof staggered inverters (MLI)has prompted another area ofMLIs, named as decreased switch tally (RSC)MLIs[1]. Contingent upon dcsource voltage proportions, theseRSC-MLIs are named symmetrical and topsy-turvy. With deviated dcsource voltages, further decrease inswitch tally canbe accomplished. A few RSC-MLI topologies, for example, staggered dc interface(MLDCL)[2], pressed U-cell (PUC) [3], fellbi-polar exchanged cells (CBSC) [4], invert voltage (RV) [5], exchanged dc sources [6], essential unit MLI [7],envelope-type(E-type)[8],T-type half breed T-type arrangement associated exchangedsources(SCSS), exchanged arrangement parallelsources (SSPS) settledMLI, exchanged capacitor unit decreased fell & different topologies are

accounted for inthe writing. InFig.1 demonstrates thecircuit setup of different single-stage 13-level lopsided RSCtopologies, for example, exchanged dcsources, PUC, fell T-type, cross breed T-type, CBSC, SSPS, RV, MLDCL, and E-type. Among the beat width tweak (PWM) plans reportedfor MLIs, transporter based plans, for example, level-moved PWM (LSPWM) and stage moved PWM (PSPWM) are the least difficult because of their ease in implementaThese PWM plans can understand inverter exchanging states in which gadgets directing for accomplishing lowerlevels stay in conductionat higherlevels also. This went about as an impediment of the traditional transporter based plans to acknowledge RSC-MLIs, since these topologies has restricted redundancies and have the exchanging activity where the lower level conduction gadgets may not stay in conduction at higher level.In the writing, different regulation plans are accounted for controlling symmetrical and deviated RSC-MLI designs. Among them, half breed PWM is one of the prevalent plans for executing awry fell topologies, for example, Cascade H-bridgeThis plan can likewise be actualized to non-fell topologies, for example, SSPS by including an extra H-connect in each stage In this plan, estimation or estimation of yield voltage of the higher voltage connect/units is important, to infer the reference signal for the lower voltage connect/units. Henceforth, any slack or blunders in the estimation or estimation will affect the yield voltage. PWM plans, for example, particular consonant end [8] and space vector are accounted for E-type, PUC, settled cell, and different three-stage RSC topologies. These exchanging plans can be summed up to higher levels, yet requires subtle estimations to get exchanging instants.Switching plans utilizing low-recurrence bearer (50 or 100 Hz) with and without legitimate administrators are accounted for different RSC MLIs, for example, MLDCL, CBSC, fundamental unit MLI, T-type, and half breed T-type These low-recurrence PWM plans brings about lower request sounds and poor THD. To get better THD and diminish the multifaceted nature in usage, different novel PWM plans are accounted for. Multi-reference tweak plan is one of such plan revealed for T-type, fell T-type, and couple of other fell topologies. This plan can be appropriate to any MLI with any number of levels, yet this plan results high THD in line-voltages .Switching capacity PWM is the other famous plan detailed for PUC, exchanged dc sources, and crossover T-type topologies. To get the exchanging beats, this plan builds up a crossover capacity utilizing least and greatest points of confinement of every bearer. In this manner, to understand these bearer limitations, controller requires various comparators, which builds the unpredictability at higher levels.Reduced transporter PWMis the other prominent PWM, which includes a unipolar tweaking and level-moved transporter signals. In this plan, beats are produced by straightforwardly contrasting reference and its bearers and further worked with client

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characterized intelligent articulations to get wanted changing heartbeats to control the inverter. Notwithstanding, these legitimate articulations shift with topological game plan and number of stage voltage levels. Further, this ordinary diminished bearer course of action results high THD in linevoltage. Consequently, an other regulating signal and diminished bearer course of action is reported.The exchanging rationale of this plan includes least and greatest limitations of every transporter to get wanted activity.

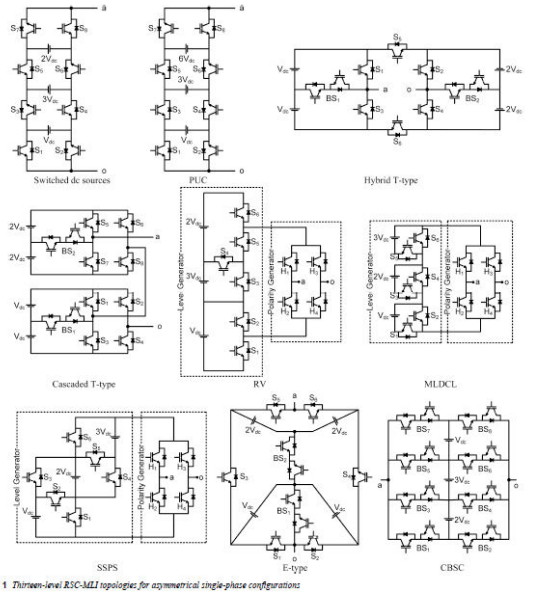

Fig. 1 *Thirteen-level RSC-MLI topologies for asymmetrical single-phase configurations*

Notwithstanding, it is to be noted thatreduced transporter PWM plans with summed up intelligent articulations are the least difficult and a lot simpler to actualize contrasted with exchanging plan including bearer least and most extreme constraints.By exploring the different adjustments of RSC-MLI topologies, the accompanying ends can be drawn

• Among the adjustment plans detailed for RSC-MLIs, decreased bearer PWM plot with sensible articulations are the easiest. Be that as it may, these legitimate articulations are not summed up and differ with inverter topology and number of levels.

• Conventional diminished transporter PWM plan results debased line THD execution, as its bearer course of action is like LSPWM–inverse stage attitude (OPD) .Consequently, in this paper, an altered diminished bearer PWM plot with summed up intelligent articulations is proposed, to such an extent that the proposed exchanging rationale can control any RSC-MLI regardless to the voltage proportions and topological course of action. To determine these bound together sensible articulations, constraints of ordinary decreased bearer tweak conspire in controlling RSC-MLI topologies are investigated. To confirm the effectiveness of the proposed PWM conspire, its presentation in controlling different 13-level unbalanced RSCMLI topologies is explored. Further, to guarantee the predominant presentation of the proposed plan, a far reaching test correlation with best in class plans revealed in the writing is exhibited. This paper is spread out as pursues: Section 2 explores the impediments of customary diminished transporter tweak plans and displays the need of bound together legitimate articulations to acknowledge RSC-MLI topologies. Area 3 shows the approach of the proposed plan and deduction of bound together coherent articulations. Trial execution of the proposed plan to different RSC topologies is talked about in Section 4.

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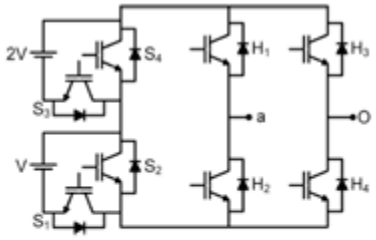

Fig. 2 Seven-level single-phase configuration of RSC-MLI-based MLDCL

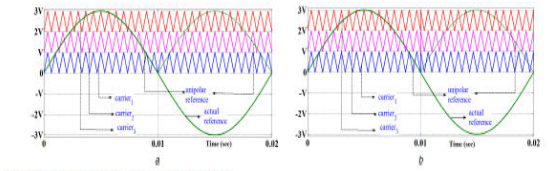

Fig. 3 *Reduced carrier PWM for seven-levels in phase-voltage*
(a) Conventional reduced carrier arrangement, (b) alternative carrier arrangement

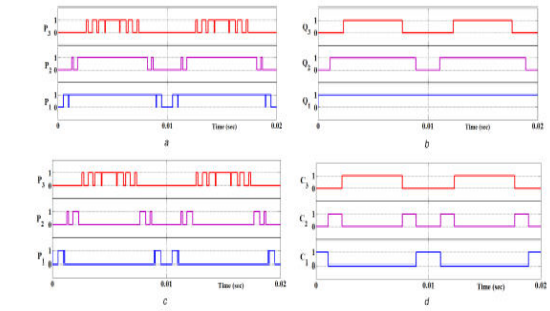

Fig. 4 *Switching pulses (P) and conduction intervals (Q and C) of seven-level reduced carrier PWM scheme:*
(a) Overlapped switching pulses, (b) Overlapped conduction intervals (Q), (c) Non-overlapped switching pulses, (d) Non-overlapped conduction interval (C)

2. Methodology and implementation of the proposed modulation scheme

To determine a brought together rationale articulation for getting non-covered interim (C) from the covered interim (Q), the nature of both these conduction interims ought to be broke down. Fig. 5 (got from Figs. 4b and d) demonstrates the conduction interims Q and C together. This figure deduces that the ideal conduction interim Ccan be acquired by playing out an intelligent activity on Q with its adjoining groups. From Fig. 5a, by watching Q3 and C3 uncovers their indistinguishable nature of exchanging and consequently

C3 = Q3 (2)

In any case, Q2 and C2 are unique in relation to one another and from Fig. 5b, the accompanying connections are gotten.

If $Q_3 = 0$ and $Q_2 = 0$, then $C_2 = 0$;
if $Q_3 = 1$ and $Q_2 = 1$, then $C_2 = 0$;
if $Q_3 = 0$ and $Q_2 = 1$, then $C_2 = 1$.

It ought to be noticed that Q3 = 1 and Q2 = 0 case does not show up as lower conduction interim Q2 consistently stays high when upper conduction interim Q3 is high. To get an intelligent connection for C2 as far as Q3 and Q2, a two-variable Karnaugh-map (K-map) is actualized in Fig. 5b. From Fig. 5b, consistent connection for C2 is gotten as C2 = Q3Q2. To understand this rationale in equipment, two rationale entryways NOT AND are required. To lessen these rationale doors, a couldn't care less factor is incorporated into K-map and the intelligent connection (3) is acquired, which requires an Ex-OR entryway as it were

$$C_2 = \bar{Q}_3 Q_2 + Q_3 \bar{Q}_2 = Q_2 \oplus Q_3 \quad (3)$$

To obtain conduction interval C_1, Fig. 5c is considered and following relationships are obtained.

If $Q_2 = 0$ and $Q_1 = 0$, then $C_1 = 0$;
if $Q_2 = 1$ and $Q_1 = 1$, then $C_1 = 0$;
if $Q_2 = 0$ and $Q_1 = 1$, then $C_1 = 1$.

With the help of K-map shown in Fig. 5c, logical relation (4) is obtained for conduction interval C_1

$$C_1 = Q_1 \oplus Q_2 \quad (4)$$

Generalising (2)–(4), (5) can be obtained, where i is the carrier number

$$\begin{aligned} &\text{for} \quad i = (n-1)/2 \\ &\quad C_i = Q_i \\ &\text{for} \quad 1 \le i < (n-1)/2 \\ &\quad C_i = Q_i \oplus Q_{i+1} \end{aligned} \quad (5)$$

Applying the beat Pi (|ref|>carrieri) over the interim Ci brings about wanted non-covered exchanging beats. This exchanging activity of the proposed balance plan to control seven-level inverter is appeared in Fig. 6.In Fig. 6, C3 should be dynamic to getting

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voltage band of 3 V to 2 V. So also, C2 and C1 should be dynamic for getting voltage band of 2 V to V and V to 0, individually. C3 high with P3 high, for example beat C3P3 is in charge of getting 3 V voltage state. C3 high with P3 low or C2 high with P2 high, for example beat C3P⁻3 + C2P2 acquires 2 V voltage state. Correspondingly, C2 high with P2 low or C1 high with P1 high, for example C2P⁻2 + C1P1 brings about V voltage state. C1 high with P1 low, for example beat C1P⁻1results in zero voltage. The extremity of these voltage states is chosen by the extremity of the adjusting signal, where positive voltage levels are acquired for the positive portion of the reference and negative voltage levels are gotten for negative portion of the balancing signal. Table 1 demonstrates the execution of the proposed changing rationale to understand a seven-level inverter topology appeared in Fig. 1. For instance, to acquire +3 V voltage level, switches H4, S1, S3, and H1 ought to be in conduction. In this manner, these switches are connected with heartbeat C3P3 for the positive portion of the reference. Also, to acquire −3 V voltage level, beat C3P3 connected to switches H2, S1, S3, and H3 for the negative portion of the reference. A comparative clarification holds useful for outstanding voltage level as displayed in Table - 1.In this proposed plan, the acquired number of wanted pulseswill be equivalent to the quantity of stage voltage levels, where eachpulse is in charge of getting a specific voltage level. Further, every one of these ideal heartbeat will be given to the gadgets (of the thought about inverter) to be in conduction to accomplish the separate voltage state. Further, summing up these got exchanging beats for higher voltage levels (6) is acquired

$$\begin{aligned}
&\text{for} \quad \frac{n-1}{2}V \\
&\quad \Rightarrow \text{switching pulse} = C_{\frac{n-1}{2}}P_{\frac{n-1}{2}} \\
&\text{for} \quad V \le iV \le \left(\frac{n-1}{2}-1\right)V \\
&\quad \Rightarrow \text{switching pulse} = C_{i+1}\bar{P}_{i+1} + C_iP_i \\
&\text{for} \quad 0\,V \\
&\quad \Rightarrow \text{switching pulse} = C_1\bar{P}_1
\end{aligned} \tag{6}$$

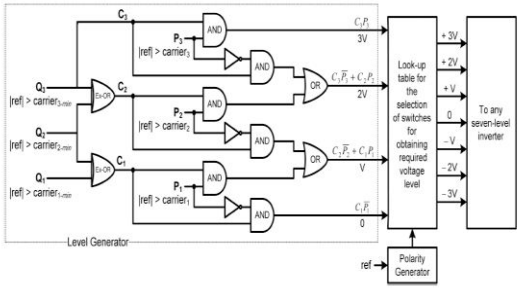

Fig. 6 *Implementation of the proposed PWM scheme for seven-level phase-voltage*

Table 1 Selection of switching devices to control seven-level inverter with the proposed scheme

Polarity generation	Voltage level	Switching pulse	Devices to be in on to obtain the respective voltage level in Fig. 2
ref ≥ 0	+3 V	C_3P_3	H_4–S_1–S_3–H_1
	+2 V	$C_3\bar{P}_3 + C_2P_2$	H_4–S_2–S_3–H_1
	+V	$C_2\bar{P}_2 + C_1P_1$	H_4–S_1–S_4–H_1
for zero-level	0	$C_1\bar{P}_1$	H_4–S_2–S_4–H_1 or H_2–S_2–S_4–H_3
	—	—	
ref < 0	−V	$C_2\bar{P}_2 + C_1P_1$	H_2–S_1–S_4–H_3
	−2 V	$C_3\bar{P}_3 + C_2P_2$	H_2–S_2–S_3–H_3
	−3 V	C_3P_3	H_2–S_1–S_3–H_3

Table 2 Experimental parameters

Circuit/parameter	Component/value
30 V isolated dc power supplies (12 no.)	30 V, 3 A dual channel regulated power supply
13-level asymmetrical RSC-MLI	developed using 2 modules of generalised converter with 24 IGBTs each
IGBT model and rating	IKW40T120, 40 A and 1200 V
carrier frequency (f_{cr})	2 kHz
amplitude modulation index (m_a)	0.98
load	three-phase star-connected 1 kW 0.85 power factor lagging.
controller (to obtain firing signals for IGBTs)	dSPACE micro-lab box RTI1202 R&D controller sampling time (20 μs)

4. Implementationofthe proposed scheme to 13-levelasymmetrical RSC-MLItopologies

The presentation of the proposedPWM plan is approved creating trial set-ups of various 3-stage IGBTbased 13-level unbalanced RSC-MLItopologies. The created topologiesare MLDCL, SSPS, exchanged

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dcsources, half and half T-type&E-type (as appeared in Fig. 1). Further,to approve the predominance of theproposed PWM conspire, the above chose topologiesare likewise controlled utilizing customary diminished transporter PWM plot. Distinctive invertertopologies are created by utilizing twoinverter modules with 24 individual IGBTsin each. The balance plans are executed indSPACE Micro-lab boxRTI1202 R&Dcontroller. The transporter signalrecurrence (fcr) and abundancy regulation file (mama) are chosen as2kHzand0.98, separately. The dc info sourcevoltage (Vdc) is chosen as 30Vandwith this, the greatest adequacy of stage voltage is180V. The total rundown ofparameters utilized in test study isgiven in Table 2 andthe photo of the exploratory set-up is appeared in Fig. 7. Table 3 demonstrates the usage oftheproposed changing rationale understandthesechose RSC-MLI topologies. Fig. 8 demonstrates the exploratory exhibition of stage voltages and their relating consonant spectra. Figs. 8a–eshow the stage voltage execution of13-level MLDCL,SSPS, exchanged dc sources, mixture T-type,&E-typehilterkilter topologies withthe proposed PWM conspire. Fig.8f delineates the stage voltageexecution of13-level MLDCL with traditional decreased transporter PWM plot. Correspondingly, Fig. 9 delineates the test line-voltage execution of these RSC topologies with the proposed PWM plan and traditional diminished bearer PWM conspire. Line-voltages and their comparing symphonious spectra of the proposed plan for considered13-level filter kilter topologies are appeared in Figs. 9a–e. Fig. 9f portrays the line-voltage performance of13-level MLDCL with traditional decreased transporter PWM plot.

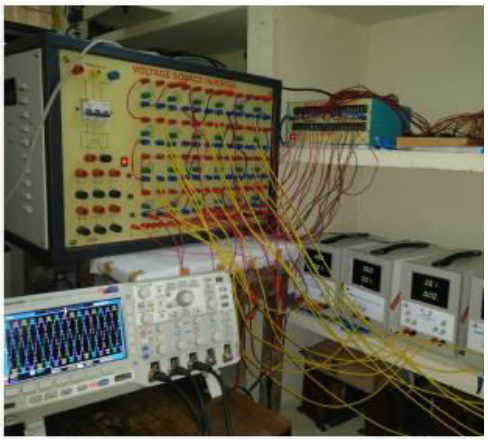

Fig. 7 Photograph of the experimental set-up for realising 13-levelasymmetrical switched dc source inverter

Table 3 Selection of switching devices to control 13-level inverter with the proposed scheme

Polarity generation	Level	Switching pulse	Devices to be in conduction to obtain the respective voltage level				
			MLDCL	SSPS	Switched dc sources	Hybrid T-type	E-type
ref ≥ 0	+6 V	C_1P_1	H_4–S_1–S_3–S_5–H_1	H_4–S_2–S_5–H_1	S_2–S_3–S_5–S_7	S_2–S_5–S_1	S_1–S_4–S_5
	+5 V	$C_2\bar{P}_6+C_2P_3$	H_4–S_2–S_3–S_5–H_1	H_4–S_1–S_5–H_1	S_1–S_3–S_5–S_7	S_2–S_5–BS_1	BS_1–S_4–S_5
	+4 V	$C_2\bar{P}_3+C_2P_1$	H_4–S_1–S_4–S_5–H_1	H_4–S_2–S_4–H_1	S_2–S_3–S_5–S_8	BS_2–S_5–S_1	S_2–S_4–S_5
	+3 V	$C_2\bar{P}_4+C_2P_3$	H_4–S_1–S_3–S_5–H_1	H_4–S_1–S_4–H_1	S_1–S_3–S_5–S_8	BS_2–S_5–BS_1	S_1–BS_2–S_5
	2 V	$C_2\bar{P}_2+C_2P_2$	H_4–S_2–S_3–S_5–H_1	H_4–S_1–S_5–H_1	S_2–S_4–S_5–S_7	S_4–S_5–S_1	S_1–S_4–S_5
	V	$C_2\bar{P}_1+C_2P_1$	H_4–S_1–S_4–S_5–H_1	H_4–S_3–S_5–H_1	S_2–S_3–S_5–S_7	S_4–S_5–BS_1	BS_1–S_4–S_5
for zero-level	0	$C_1\bar{P}_1$	H_4–S_2–S_4–S_5–H_1 or H_2–S_2–S_4–S_5–H_3	H_1–H_3 or H_2–H_4	S_1–S_3–S_5–S_7	S_4–S_5–S_3	S_1–S_3–S_5
ref < 0	−V	$C_2\bar{P}_1+C_2P_1$	H_2–S_1–S_4–S_5–H_3	H_2–S_3–S_5–H_3	S_1–S_4–S_5–S_8	S_2–S_5–BS_1	BS_1–S_3–S_5
	−2 V	$C_2\bar{P}_3+C_2P_2$	H_2–S_2–S_3–S_5–H_3	H_2–S_1–S_5–H_3	S_1–S_3–S_5–S_8	S_2–S_5–S_3	BS_1–BS_2–S_5
	−3 V	$C_2\bar{P}_4+C_2P_3$	H_2–S_1–S_3–S_5–H_3	H_2–S_1–S_4–H_3	S_2–S_4–S_5–S_7	BS_2–S_5–BS_1	S_2–BS_2–S_5
	−4 V	$C_2\bar{P}_5+C_2P_4$	H_2–S_1–S_4–S_5–H_3	H_2–S_2–S_4–H_3	S_1–S_4–S_5–S_7	BS_2–S_5–S_3	S_1–S_3–S_5
	−5 V	$C_2\bar{P}_6+C_2P_5$	H_2–S_2–S_3–S_5–H_3	H_2–S_1–S_5–H_3	S_2–S_4–S_5–S_8	S_4–S_5–BS_1	BS_1–S_3–S_5
	−6 V	C_2P_6	H_2–S_1–S_3–S_5–H_3	H_2–S_2–S_5–H_3	S_1–S_4–S_5–S_8	S_4–S_5–S_3	S_2–S_3–S_5

So as assess the entire inverter framework, itis important demonstrate the presentation ofthe inverter flows. Fig10 delineates the exploratory line-current execution of RSC topologies with proposedand customary decreased bearer PWM plans for three-stage star-associated load.Line-current and their comparing consonant spectraofthe proposed plan forconsidered 13-level topsy-turvy topologiesare appeared inFigs.10a–e. Fig. 10f portrays theline-current execution of

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13level MLDCLwith customary diminished bearer PWM scheme.Inaviewto appraise the adequacy ofthe proposed PWM conspire, a far reaching correlation is completed transporter based PWM plans revealed in the writing. Forthis, the PWM conspire alongside theinverterrevealed inthe writing executed tentatively contrasted and the proposedPWM plot regarding consonant execution, multifaceted nature in usage, and calculation load. The synopsis of benefits and negative marks are introduced inTable 4. Looking atFigs.8–10 alongside Table4,the accompanying ends are inferred.

a) From Figs. 8a–e, itis seen thatall the stage voltagewaveforms and their symphonious spectraare indistinguishable with predominant consonant showed up at recurrence adjustment list (mf=40).

b) Comparing Fig. 8f with Figs. 8a–e, it very well may be seen that THD estimations of customary decreased transporter plot (6.1%) are less when contrasted and the proposed plan (7.8%). By the by, the customary decreased transporter PWM conspire

c) haslessTHD esteem however its side-band music are unique and focused at mf. Thesizeofthe music is likewise extraordinary in the two techniques, which prompts huge contrast inline-voltageTHD.

d) Theline-voltagewaveformsandtheir relating consonant spectra withtheproposedPWM plan appeared inFigs. 9a–eare indistinguishable as far as waveform shapeand symphonious execution. The acquired THDare indistinguishable withside-band music focused atmf=40.

e) ComparingFigs. 9a–e withFig. 9f, it very well may be seen thatthe proposed plan producesimproved symphonious execution (2.8%)when contrasted and regular diminished bearer PWM plot (6.0%). The explanation behind this is theproposed PWM plan willhelpforbetter wiping out music displayed in stage voltages.

f) Fromline-current execution appeared in Fig. 10, it is seen that line-current waveformsand their comparing symphonious spectra withthe proposed PWM plan are indistinguishable as far as waveform shapeand consonant execution. It can likewise be seen that the proposed plan producesimproved consonant execution (2.3%)when contrasted and ordinary decreased bearer PWM plan line-flows (5.4%) appeared in Fig. 10f.

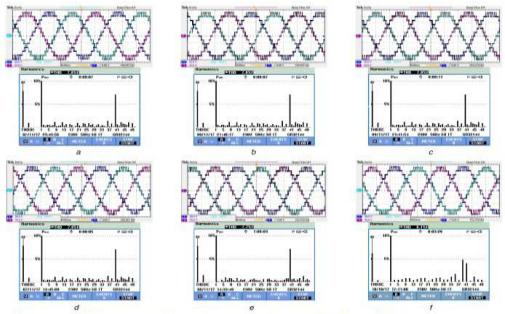

Fig. 8 *Phase-voltage waveforms and their corresponding harmonic spectra (scale: X-axis: 4 ms/div and Y-axis: 50 V/div)*
(a) MLDCL, *(b)* SSPS, *(c)* Switched dc sources, *(e)* E-type, *(f)* MLDCL with conventional reduced carrier PWM

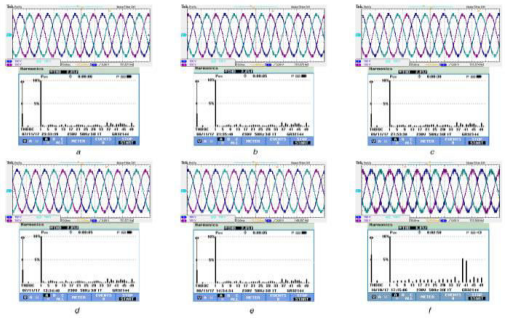

Fig. 9 *Line-voltage waveforms and their corresponding harmonic spectra (scale: X-axis: 10 ms/div and Y-axis: 100 V/div)*
(a) MLDCL, *(b)* SSPS, *(c)* Switched dc sources, *(d)* Hybrid T-type, *(e)* E-type, *(f)* MLDCL with conventional reduced carrier PWM

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i. Theproposed plan canbe straightforwardly pertinent toany MLI topologyand effectively versatile to higher numberoflevels independent oftopological course of action and dcvoltage proportions.

ii. Theproposed PWM plan produces improvedlineTHD . execution contrasted and regular diminished bearer andmulticarrier PWM plans and comparative THD execution when contrasted and exchanging capacity PWM plot.

iii. The turnaroundtime for execution ofthe proposed PWM I. plan is altogether diminished andremains practically invertertopology. Theless calculation weight ofthe proposed plan will enable thecontrollerto precisely execute higher exchangingfrequencies.

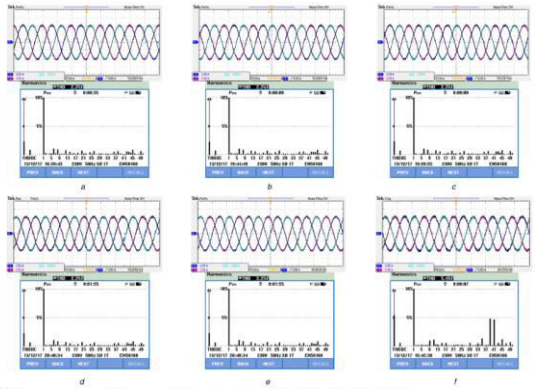

Fig. 10 *Line-current waveforms and their corresponding harmonic spectra (scale: X-axis: 10 ms/div and Y-axis: 2 A/div) (a)* MLDCL, *(b)* SSPS, *(c)* Switched dc sources, *(d)* Hybrid T-type, *(e)* E-type, *(f)* MLDCL with conventional reduced carrier PWM

Conclusion

To defeat the impediments of traditional decreased bearer PWM conspire, this paper displayed a changed diminished transporter PWM plot with brought together legitimate articulations. The adequacy of the proposed exchanging rationale is approved with test ponders on different 13-level hilter kilter RSC-MLItopologies. Further, unrivaled execution oftheproposed plan confirmed by contrasting its presentation and traditional transporter PWM plans. Topology-autonomous activity, streamlined changing rationale speculation to higherlevels, less calculation weight, and improvedline-voltageTHD execution ofthe proposed decreased bearer PWMplan fills in asa feasible answer for defeat the negative marks of ordinary multicarrier, diminished transporter, and multireference PWM plans.

Table 4 Performance comparison of carrier-based PWM schemes reported in the literature with the proposed PWM scheme

Carrier-based PWM scheme and topology reported in the literature					With the proposed PWM scheme			Merits and demerits of PWM scheme reported in the literature
PWM scheme	Topology	Phase-voltage THD, %	Line-voltage THD, %	Turnaround time, µs	Phase-voltage THD, %	Line-voltage THD, %	Turnaround time, µs	
multi-reference [11, 13, 23, 25]	T-type seven-level [11]	15.7	14.8	6.5	15.7	4.9	6.2	✓ require less computational time ✓ scalable to higher levels ✓ directly applicable to all topologies ✗ high line-voltage THD ✗ difficulty in implement for closed-loop applications due to the presence of multiple references
reduced carrier with logic gates [9, 10, 27]	modified T-type seven-level [10]	15.8	15.0	19	15.6	4.8	5.9	✗ high line-voltage THD ✗ switching logic is complex and requires more computational time ✗ neither scalable nor directly applicable to all topologies
switching function PWM [6, 16]	symmetrical seven-level switched dc-sources [6]	15.6	4.8	7.5	15.5	4.7	6.0	✓ good line-voltage THD performance ✓ scalable and applicable to all topologies ✗ involves large number of comparators which occupies more memory and requires more computation time to realise the switching pulses
reduced carrier [5]	RV seven-level [5]	15.7	14.9	5.3	15.6	4.8	6.1	✓ scalable with simplified switched logic and takes very less computational time ✗ not applicable to all topologies ✗ high line-voltage THD
hybrid PWM [17, 20, 22, 32]	asymmetrical SSPS with H-bridge eleven-level [17]	9.9	3.1	6.6	9.6	3.0	7.2	✓ good line-voltage THD performance ✓ scalable and possess simplified switched logic and takes very less computational time ✗ applicable only to asymmetrical cascaded topologies ✗ may involve mixed switching frequencies, hence may produce unwanted voltage spikes in phase and line-voltages

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