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Paper Authors

VALAVALA SUMA, PULAKHANDAM VANI

KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY FOR WOMEN,KORANGI,ANDHRAPRADESH,INDIA,533461

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MULTI MODULAR ADDER WITH GDI-BASED MUX DESIGN IN CMOS CIRCUITS

[1]VALAVALA SUMA', [2]PULAKHANDAM VANI

[1]M.TECH VLES, DEPT OF E.C.E, KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY FOR WOMEN, KORANGI, ANDHRAPRADESH,INDIA,533461

[2]ASSISTANT PROFESSOR, KAKINADA INSTITUTE OF ENGINEERING AND TECHNOLOGY FOR WOMEN, KORANGI, ANDHRAPRADESH, INDIA,533461

ABSTRACT:

Since there is many advancement in VLSI technology and there are many efficient styles of designing VLSI circuits. Some of the styles are CMOS, PTL, GDI (Gate Diffusion Input) techniques. GDI technique helps in designing low-power digital combinatorial circuit by which we can eradicate demerits of CMOS, PTL techniques. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. This paper discusses about the performance characteristics of a Full Adder based Carry Select Adder using various logics and also GDI-MUX technique. The adders are used in many data path applications and also the area, power consumption and delay in the design can be reduced. The proposed technique is the GDI-Mux which enables the reduction of above mentioned parameters and also reduce the number of transistors. The Full Adder based Carry Select Adder designed in Complementary Pass Transistor Logic, Complementary Metal Oxide Semiconductor Logic and Gate Diffusion Input –Mux and they are compared and the most efficient technique is identified. The different methods are compared with respect to the layout area; transistor count, delay, and power dissipation are discussed here in this paper showing advantages and drawbacks of GDI compared to CMOS style.

I. INTRODUCTION:

In VLSI digital circuits, power and area reduction is the important parameter which decides the efficiency of the circuit [4&9]. Power consumption is the primary factor in high performance computing application [5-6], Image processing applications [7], Portable applications [8&10] and wireless applications. Silicon area also has the direct impact on device size and cost. CMOS logic was introduced in early 80's and from that several design techniques was developed to save power & area and also to increase the speed of operation. Another one design technique known as Gate Diffusion Input (GDI) style [1-3] that replaces CMOS logic and it was originally developed for fabrication in SoI and twin-well CMOS process. In GDI style, complex logic functions such as MUX, encoder, decoder...etc., can be implemented using

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only two transistors. It‘s clear that, area and dynamic power consumption in GDI style based combinational and sequential logics were significantly reduced as compared to CMOS logics. In GDI style, the voltage swing at the output side is reduced due to threshold drops as compared to pass transistor logic (PTL) technique. This causes the degradation in performance and increased short circuit power. But this performance degradation is negligible, since GDI style uses only two transistors as compared to other techniques. The performance of the system increases day by day and this results in increasing number of transistors in the circuit. To manage this, it is necessary to develop standard cells with low power to improve the overall system performance. In ASIC design methodology standard cell libraries are required by all CAD tools for IC design. Standard cells are predesigned and verified blocks. This helps the designer to reduce the product development time and easily manages the overall chip complexity. CMOS logic based standard cell are popular and almost used in all designs. Here we proposed GDI style based standard cells and its one of the power reduction techniques compared to CMOS logic. A single GDI cell consists of one NMOS & PMOS transistor and it has three input terminals and one output terminal. Fig 1 shows the single GDI cell.

The advantages of GDI technique are:

(i)Less power dissipation

(ii)Reduced delay

(iii)Reduced area.

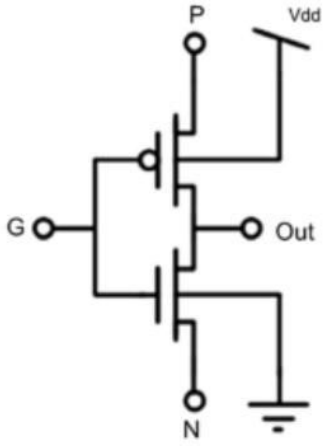

Figure 1: Representing Basic GDI Cell

II. POWER REDUCTION TECHNIQUES:

2.1 REDUCTION TECHNIQUES

1. Design time techniques

The design time techniques are static, they can‟t be modified or changed once they are fixed, while the circuit is operating.

$$I_{off} = I_0 e^{\frac{V_{GS} - V_{th,0} + mV_{DS}}{\eta V_T}}$$

To reduce leakage it exploit the delay slack.

a) Dual threshold CMOS.

This technique compromise between the high performance and low leakage power. Transistors those are located on critical paths are assigned as low threshold voltage and the transistors that are not critical to timing can tolerate high threshold voltages and slow switching speeds. The selection of the control voltages are conducted at design times, no additional circuits are required. The below table shows the leakage current for high and low threshold voltage transistors in a 70nm process technology. We observe that leakage energy of transistors of low threshold voltage is larger

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than a factor of 75 than the high threshold voltage transistors. Hence if we replace the low –Vt transistor with a high –Vt transistor it will reduce the energy or power.

Tr type	V_{dd}	V_t	I_{off}
High-V_t	0.75	0.4	26
Low-V_t	0.75	0.2	1941

Table 1: Representing Voltage levels for transistor

b) Multiple supply voltage Supply voltage scaling also reduces the leakage power, because subthreshold leakage due to the GIDL and DIBL as well as the gate leakage component when the supply voltage is scaled down. To achieve low power with respect to high performance two methods can be employed i.e. dynamic and voltage scaling.

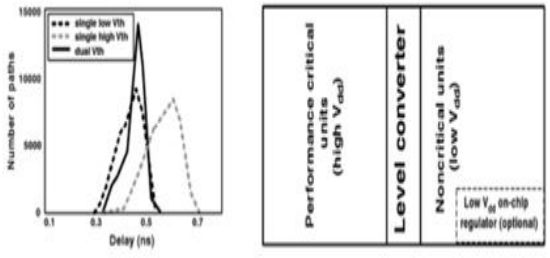

Figure 1.2: Representing the Threshold graphs a) path vs delay Threshold graph b) performance flow model

2. Runtime leakage reduction
   a) Transistor stacking (self reverse biased)

Subthreshold leakage current reduces when it flows through a stack of series connected transistors. The below figures shows the transistor stacking process.When both M1 and M2 are turned off, the voltage at the intermediate nodeVm is positive due to small drain current. Due to positive source potential, gate to source voltage of M1 becomes negative, hence subthreshold current reduces.

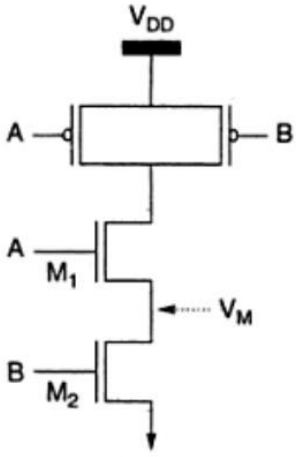

Figure 1.3: Representing Transistor stacking

b) Sleep transistor technique

The sleep transistor approach is most commonly used technique for the leakage power reduction. In this technique an extra "sleep" PMOS transistor is placed between pull up network and VDD and an additional NMOS transistor is place between the ground and pull down network. These transistors turn off the circuit by cutting off the power in the sleep mode. So this technique can reduce the leakage power in good margin by cutting off the power source. However this technique causes floating output in the sleep mode.

3. Sleepy stack approach

We have discussed the stack approach already, so when the stack approach effectively merged with sleep transistor technique, this sleep stack approach is developed. By using stack effect this technique divides transistors into two half-length transistors.

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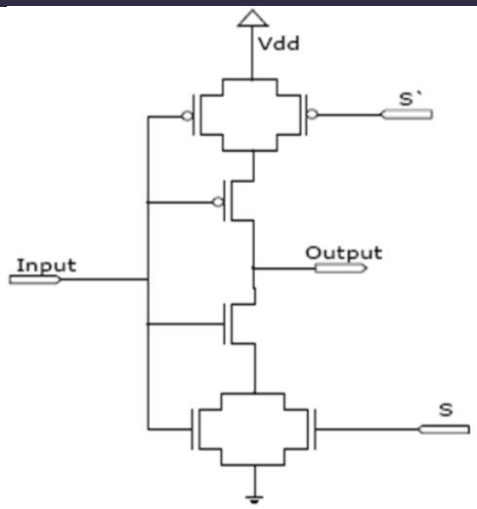

Figure 1.4: Representing Transistor stacking

Then the sleep transistors are connected parallel to one of the divided transistor. During the sleep mode sleep transistors are off, stacked transistors reduces the leakage current. The main cons of this technique is the power delay since we are replacing the transistors

4. Sleepy keeper approach

In sleepy keeper technique, sleep transistors is parallel in both pull up and pull down network. It uses the leakage feedback technique.

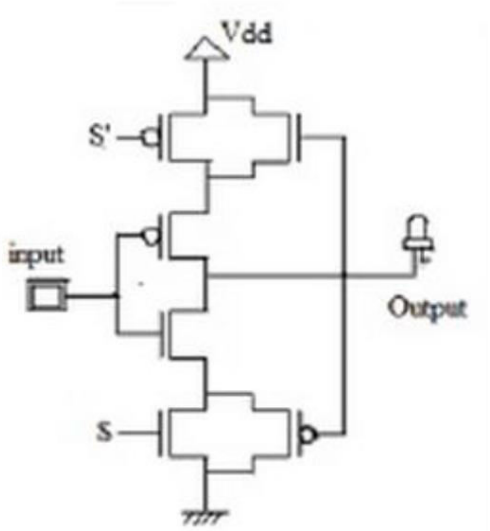

Figure 1.5: Representing sleep keep logic diagram

In this technique a PMOS and NMOS is placed in parallel transistors. In sleep mode sleep transistors are turned off and one of the parallel connected transistors keep on track power rail.

5. Dual sleep technique

In dual sleep methods two transistors are connected in parallel similar to the keeper approach. In both active and inactive mode sleep transistors is always in both pull down and pull up network. So output is connected to GND and VDD always. In this method less number of transistors is needed to apply a certain logic circuit. This method has good tradeoff between the delay, power and area.

6. Dual stack technique

In dual stack method two PMOS and two NMOS transistors are used. The two PMOS transistors are used in the pull down network and two NMOS network are used in pull up network. The advantage of this method is, NMOS degrades at high logic level and PMOS degrades at low logic level. But the disadvantages of this technique compared to previous technique is delay, the delay increases

7. Variable threshold CMOS (VTCMOS)

This is a body biasing design technique. To achieve different threshold voltages, a self-substrate bias circuit is used to control body bias. In the active mode a zero body bias is applied, while in standby mode a reverse body bias is applied to control the threshold voltage and cut off leakage current.

III. DESIGN MODELS BASED ON GDI TECHNIQUE:

Figure 1, shows the single GDI cell and looks like CMOS inverter, since it consists of two transistors. However it contains three

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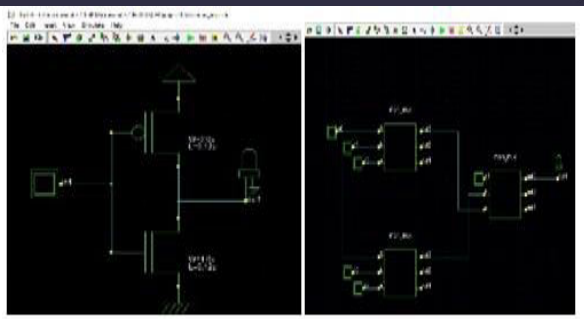
inputs, G (common gate input of both the nMOS and pMOS), P (input to the source/drain of pMOS) and N (input to the source /drain of nMOS). Using this single GDI cell, different logic functions (AND, OR NOT) can be implemented as shown in table 1. These logic functions implementation were complex in standard CMOS logic (6-12 transistors), hence these ogic functions are implemented using only 2 transistors. The Multiplexer (MUX) function can also implemented using GDI style and it's efficient as compared to CMOS implementation. GDI gates can be affected by threshold voltage drops at the output side which reduces current drive strength and reduces the performance of the standard cells. This drop also increases the direct path static power dissipation. The above said two effects can be overcome by using swing restoration buffers with a multiple Vth approach (MVT). This MVT suggest uses of low threshold transistors where voltage drop is expected.

CONCEPT:

A **multiplexer** or mux is a combinational circuits that selects several analog or digital input signals and forwards the selected input into a single output line. A multiplexer of 2^n inputs has n selected lines, are used to select which input line to send to the output.

DESIGN MODEL IN MICROWIND



a) CMOS INVERTER b) CMOS 4X1 mux

Figure 6 shows how a 4:1 MUX can be constructed out of two 2:1 MUXs.

Design using pass-transistor logic

A multiplexer can be designed using various logics. Fig.5.1 shows how a 2:1 MUX is implemented using a pass-transistor logic.

The pass-transistor logic attempts to reduce the number of transistors to implement a logic by allowing the primary inputs to drive gate terminals as well as source-drain terminals. The implementation of a 2:1 MUX requires 4 transistors (including the inverter required to invert S), while a complementary CMOS implementation would require 6 transistors. The reduced number of devices has the additional advantage of lower capacitance.

Design using transmission gate logic

A transmission gate is an electronic element and good non mechanical relay built with CMOS technology. It is made by parallel combination of nMOS and pMOS transistors with the input at the gate of one transistor (*C*) being complementary to the input at the gate () of the other. The symbol of a transmission gate is shown below in fig.5. The transmission gate acts as a bidirectional switch controlled by the gate signal *C*. When *C=1*, both MOSFETs are on, allowing the signal to pass through the gate. In short, *A=B, if C=1*. On the other hand, *C=0*,

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places both transistors in cut-off, creating an open circuit between nodes *A* and *B*. Fig.5. b shows the implementation of a 2:1 MUX using transmission gate logic.

Here, the transmission gates selects input *A* or *B* on the basis of the value of the control signal *S*. When *S=0, Z=A* and when *S=1, Z=B*.

IV. PROPOSED MODEL FOR 2X1 and 4X1 MUX USING GDI:

4.1 GDI Technique Based For Mux And Inverter:

The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low-power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top-down approach by means of small cell library [5]. The basic cell of GDIis shown in Fig. 2.1.The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supplyand it can be randomly biased.2.It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal) [11].GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design. We can realize different Boolean functions with GDI basic cell. Table I shows how different Boolean functions can be realized by using different input arrangements of the GDI cell.

GDI technique solves the problem of poor ON to OFF transition characteristic of PMOS and providing the full swing at internal node of circuit. Fig.5.1a show the b is to 1 MUX select line S is common input for gate terminal of PMOS_1 and NMOS_1. Input A and input B is connected to the source terminal of PMOS_1 and NMOS_1 respectively. When S is low then PMOS_1 is ON and pass the input B from source terminal to drain terminal. When S is high then NMOS_1 is ON and PMOS_1 is off. Output is common for drain terminal for PMOS_1 and NMOS_1

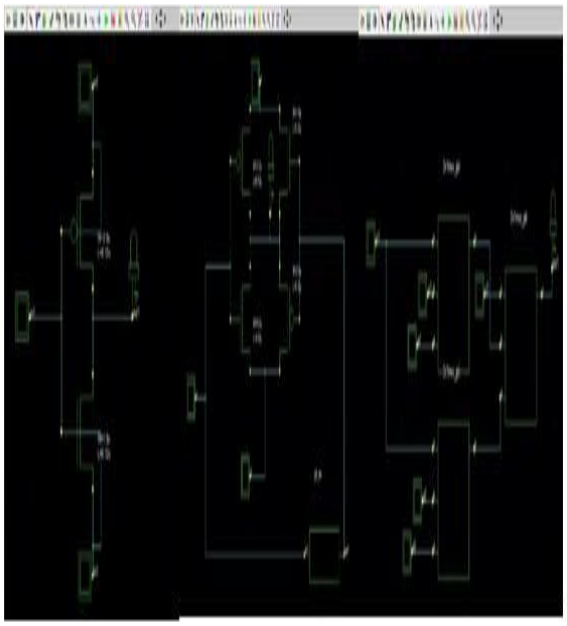

FIGURE 4.1 a) Inverter design b) 2X1 MUXc) 4X1 Mux

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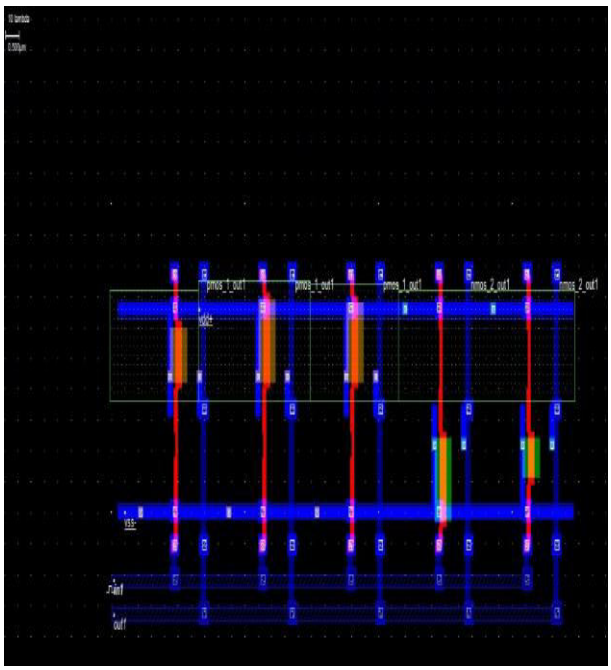
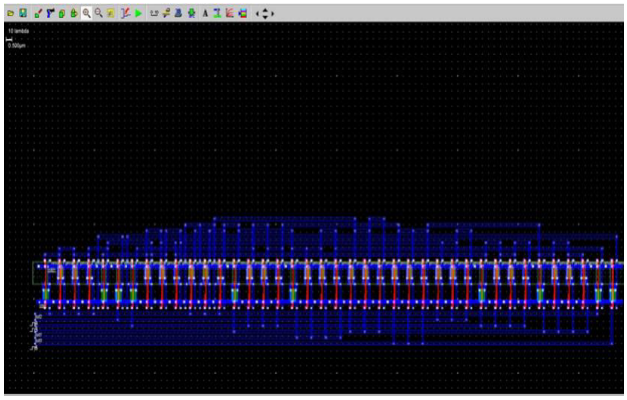
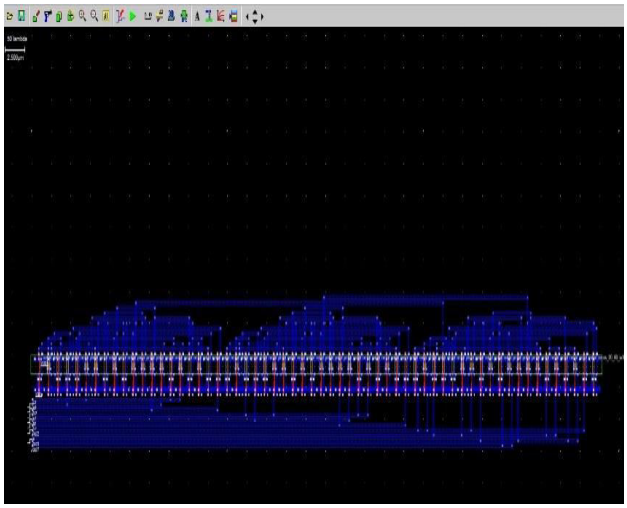
V.RESULTS AND DISCUSSION:

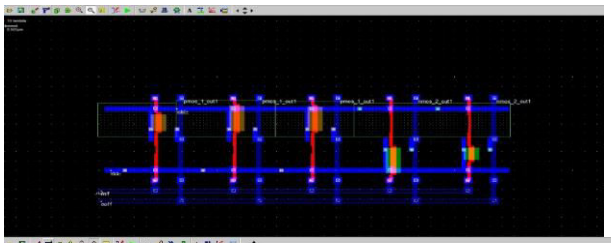
Layout Diagram for CMOS Inverter And Mux:

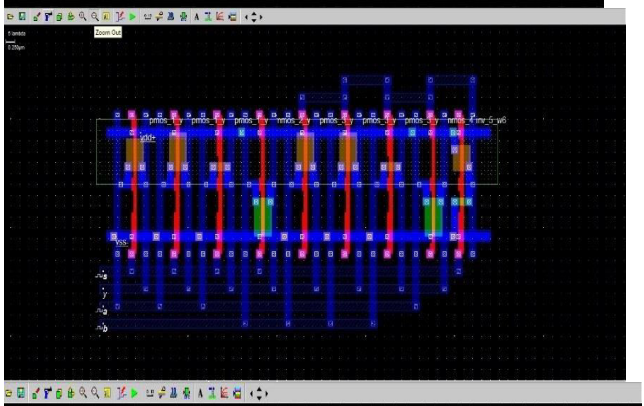


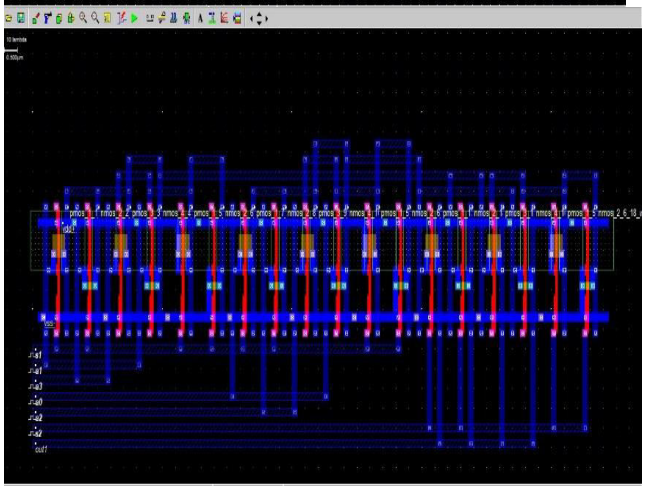




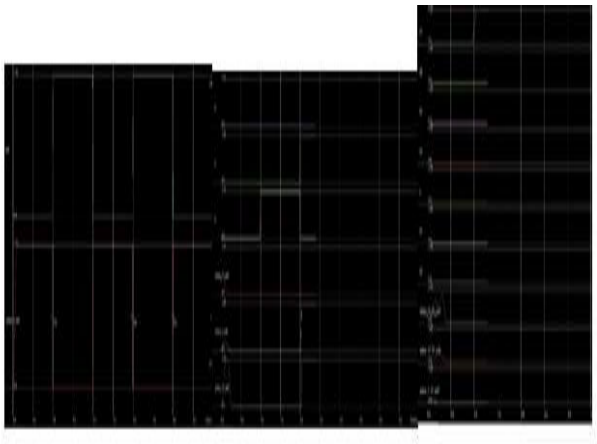
LAYOUTS FOR GDI TECHNIQUE FOR INVERTER AND MUX







Transient Analysis For CMOS:



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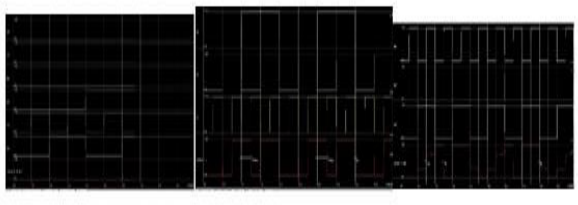
TRANSCIENT ANALYSIS FOR GDI BASED INVERTER AND MUX:



DISCUSSION:

1. Each model for the CMOS and GDI based design is modelled and implemented in DSCH as spice diagram shown in chapter 5.
2. Such spice models are being converted to Verilog modules and are implemented as Layouts in Microwind software.
3. The results are obtained based on the BSIM4 simulation of the design (Layouts). Each condition from the Chapter 5 table is verified and accordingly implemented.
4. Finally the power, area and delay are represented as a tabulated for each design models utilized.

COMPARISION TABLE

FACTORS	CMOS						GDI		
	INVERTER		MUX 2X1		MUX 4X1		INVERTER		MUX
	90	45	90	45	90	45	90	45	90
POWER (WITH 90 nm and 45 nm technology) (uW)	3.67	0.414	42.95	21.95	117	114	0.09	2 nw	5.36
AREA (um)	0.221	0.114	4.2	2.1	18.7025	9.36	1.025	0.51	0.675
DELAY (ns)	1.9	1.7	0.8	0.4			0	0	1.6
NO of TRANSISTORS	2		20		60		2		6

VI. CONCLUSION:

The main aim behind the whole works is to design and propose new low power digital circuits for the Multiplexer employing the GDI technique for power reductions and area reduction also. The GDI technique for MUX is chosen for the work as a systematic and simple approach for Boolean expressions with multiple terms. The proposed circuit consumes only about a quarter amount of power in comparison to the conventional CMOS in this converter. 72.43% decreases power consumption of GDI MUX with respect to CMOS logic. Whereas, 25.42% decreases power consumption of GDI mux with respect to Pass transistor.

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