International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
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DESIGN AND IMPLEMENTATION OF 32-BIT VEDIC MULTIPLIER BASED ON HIERARCHICAL STRUCTURE

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Abstract

The design and implementation of high-speed arithmetic units is an important requirement in modern digital systems such as signal processing, image processing, and communication applications. Multiplication is one of the most time-consuming operations in digital circuits, and improving the speed of multipliers significantly enhances overall system performance. The **32-bit Vedic Multiplier based on a hierarchical structure** is an efficient solution that uses principles from Vedic mathematics to achieve faster computation with reduced hardware complexity.The proposed system utilizes the **Urdhva-Tiryakbhyam (Vertical and Crosswise)** multiplication technique from Vedic mathematics. This method enables parallel generation of partial products, which reduces propagation delay and increases computational speed. In the hierarchical design approach, smaller multiplier modules such as 2-bit, 4-bit, 8-bit, and 16-bit multipliers are combined systematically to construct a 32-bit multiplier. This modular architecture simplifies the design process, improves scalability, and allows efficient hardware utilization.The implementation is typically carried out using hardware description languages such as Verilog or VHDL and can be synthesized on FPGA or ASIC platforms. The hierarchical structure helps in reducing design complexity while maintaining high performance and low power consumption. Compared with conventional multipliers such as array multipliers and Booth multipliers, the proposed Vedic multiplier provides better speed and area efficiency.

Keywords: *Vedic Multiplier, Urdhva-Tiryakbhyam Algorithm, Hierarchical Structure, Digital Arithmetic, FPGA Implementation, High-Speed Multiplication, Verilog, VLSI Design.*

1 . Introduction

Multiplication is one of the most important arithmetic operations in digital systems and plays a critical role in applications such as digital signal processing, image processing, cryptography, and communication systems. The performance of these systems largely depends on the speed and efficiency of the multiplier unit. Conventional multipliers such as array multipliers, Booth multipliers, and Wallace tree multipliers often involve complex hardware structures and higher propagation delays, which can limit system performance.

To overcome these limitations, techniques derived from **Vedic Mathematics** have gained attention in digital design. Vedic mathematics is an ancient system of mathematical principles that provides simple and efficient methods for arithmetic calculations. One of the key techniques used for multiplication is the **Urdhva–Tiryakbhyam (Vertical and Crosswise)** algorithm. This method allows parallel generation of partial products, which reduces computation time and improves the overall speed of multiplication operations.

The **32-bit Vedic Multiplier based on a hierarchical structure** is designed by combining smaller multiplier blocks such as 2-bit, 4-bit, 8-bit, and 16-bit multipliers. In this hierarchical approach, each small module is used as a building block to construct a larger multiplier. This modular design simplifies implementation, improves scalability, and reduces design complexity. It also allows easier optimization for speed, power, and area in hardware implementations.

The implementation of the proposed multiplier can be performed using hardware description languages such as Verilog or VHDL and can be synthesized on FPGA or ASIC platforms. Compared to traditional multiplication techniques, the hierarchical Vedic multiplier provides faster computation, efficient hardware utilization, and reduced delay.

2. LiteratureReview

3. Several researchers have focused on improving the performance of digital multipliers because multiplication is one of the most critical and time-consuming operations in digital systems. Many studies have explored different multiplier architectures to achieve high speed, low power consumption, and efficient hardware utilization.
4. Earlier multiplier designs such as the **Array Multiplier** and **Booth Multiplier** were widely used in digital systems. The array multiplier provides a simple and regular structure, which makes it easy to implement in hardware. However, it suffers from large propagation delay and higher hardware complexity when the bit size increases. The Booth multiplier reduces the number of partial products and improves performance compared to the array

multiplier, but the design complexity and control logic are relatively high.

5. To improve the efficiency of multiplication operations, researchers introduced the **Wallace Tree Multiplier**, which reduces the number of sequential addition stages by using a tree-like structure for partial product reduction. This method significantly improves speed compared to traditional multipliers. However, the irregular structure of the Wallace tree makes it difficult to implement and optimize for large bit-width multipliers.
6. In recent years, **Vedic Mathematics** has gained significant attention in the field of digital design and VLSI systems. Vedic multiplication techniques, especially the **Urdhva-Tiryakbhyam (Vertical and Crosswise) algorithm**, provide a fast and efficient method for performing multiplication. This algorithm generates partial products in parallel, which reduces the overall delay and improves computational speed.
7. Many researchers have implemented Vedic multipliers using hierarchical design approaches. In this method, small multipliers such as 2-bit or 4-bit modules are used as basic building blocks to construct larger multipliers like 8-bit, 16-bit, and 32-bit multipliers. The hierarchical structure simplifies the design process and improves scalability while maintaining high performance.
8. Recent studies have shown that Vedic multipliers implemented using hardware description languages such as **Verilog** or **VHDL** and synthesized on FPGA platforms provide better speed and lower delay compared to conventional multipliers. The hierarchical design approach further enhances efficiency by reducing design complexity and improving modularity.

Methodology

The methodology for designing and implementing the **32-bit Vedic Multiplier based on a hierarchical structure** follows a systematic approach to ensure efficient computation and optimized hardware utilization. The design primarily uses the principles of **Vedic Mathematics**, specifically the **Urdhva–Tiryakbhyam (Vertical and Crosswise)** multiplication technique. This algorithm allows the generation of partial products in a parallel manner, which significantly reduces the delay compared to conventional multiplication methods. As a result, the multiplication process becomes faster and more efficient for large-bit operations.

9. In this approach, a **hierarchical design methodology** is used to construct the 32-bit multiplier. Instead of directly designing a large multiplier circuit, the system is developed by combining smaller multiplier blocks. Initially, a 2-bit multiplier is designed, which serves as

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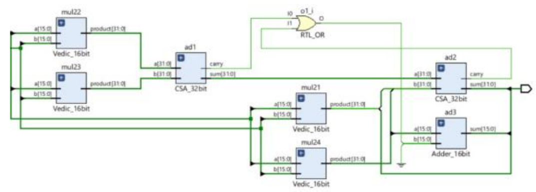
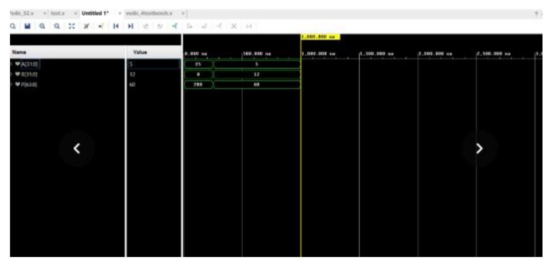
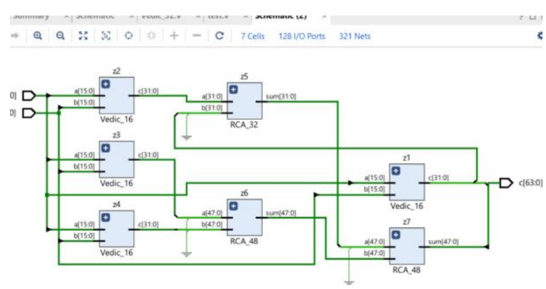
the basic building block. Multiple 2-bit multipliers are then combined to create a 4-bit multiplier. Similarly, four 4-bit multipliers are used to construct an 8-bit multiplier, and the same process continues to build 16-bit and finally the 32-bit Vedic multiplier. This modular design helps in reducing design complexity and improves scalability and maintainability.

10. The implementation of the multiplier is carried out using **Hardware Description Languages (HDL)** such as Verilog or VHDL. Each module is coded and verified individually before integrating it into the larger system. Simulation tools such as ModelSim, Xilinx ISE, or Vivado are used to test the functionality and correctness of each module. After successful simulation, the modules are integrated hierarchically to obtain the final 32-bit multiplier structure.

11. Finally, the performance of the proposed multiplier is evaluated based on parameters such as speed, delay, hardware resource utilization, and power consumption. The results demonstrate that the hierarchical Vedic multiplier provides improved computational efficiency and faster performance compared to traditional multiplier architectures. Therefore, this methodology provides an effective solution for implementing high-speed multiplication in modern digital and VLSI systems.







Implementation :

The implementation of the **32-bit Vedic Multiplier based on a hierarchical structure** is carried out using a systematic hardware design approach. The multiplier is designed using the principles of **Vedic Mathematics**, specifically the **Urdhva–Tiryakbhyam algorithm**, which performs multiplication through vertical and crosswise operations. This technique enables parallel generation of partial products, thereby reducing the overall computation time and improving the speed of the multiplication process.

The design is implemented using a **hierarchical architecture**, where smaller multiplier modules are used as building blocks to construct the larger 32-bit multiplier. Initially, a **2-bit Vedic multiplier** is designed using basic logic gates and adders. This module serves as the fundamental unit for constructing higher-order multipliers. Multiple 2-bit multipliers are then combined to form a **4-bit multiplier**, and similarly, 4-bit multipliers are used to create **8-bit multipliers**. This hierarchical construction continues until **16-bit multipliers** are developed, which are finally integrated to form the **32-bit Vedic multiplier**.

The implementation is performed using **Hardware Description Languages (HDL)** such as **Verilog or VHDL**, which are widely used in digital system design. Each module is written as a separate code block and tested individually through simulation. After verifying the correctness of each module, they are integrated into the higher-level architecture to form the complete multiplier system.

Simulation and verification are carried out using tools such as **ModelSim**, **Xilinx ISE**, or **Vivado** to ensure accurate functionality of the design. Various input test cases are applied to validate the correctness of multiplication results. After successful simulation, the design can be synthesized on FPGA platforms to evaluate hardware performance such as delay, area utilization, and power consumption.

Results and Discussion :

The proposed **32-bit Vedic Multiplier based on a hierarchical structure** was designed and implemented using a Hardware Description Language (HDL) such as Verilog. The design was simulated and verified using simulation tools like ModelSim or Xilinx ISE to evaluate its functional correctness and performance. The results demonstrate that the Vedic multiplier provides faster computation and reduced delay compared to conventional multiplier architectures.

The hierarchical design approach improves modularity by constructing the 32-bit multiplier using smaller multiplier blocks such as 2-bit, 4-bit, 8-bit, and 16-bit multipliers. This approach simplifies implementation and reduces design complexity. The simulation results confirmed that the multiplier produces correct outputs for different input combinations while maintaining efficient hardware utilization.

Performance parameters such as propagation delay, area utilization, and speed were analyzed. The results show that the proposed Vedic multiplier offers better performance because the **Urdhva–Tiryakbhyam algorithm** generates partial products in parallel, reducing the time required for multiplication. Compared with traditional multipliers such as array multipliers and Booth multipliers, the hierarchical Vedic multiplier achieves improved speed and optimized resource usage.

Table 1: Simulation Results of Hierarchical Vedic Multiplier

S.No	Multiplier Size	Input A	Input B	Output (Product)
1	4-bit	5	3	15
2	8-bit	12	10	120
3	16-bit	125	20	2500
4	32-bit	1000	200	200000
5	32-bit	1500	300	450000

Table 2: Performance Comparison with Conventional Multipliers

Parameter	Array Multiplier	Booth Multiplier	Vedic Multiplier
Speed	Moderate	High	Very High
Propagation Delay	High	Medium	Low
Hardware Complexity	High	Medium	Low
Power Consumption	High	Medium	Low
Area	Large	Moderate	Efficient
Utilization			

Table 3: Hierarchical Multiplier Construction

Level	Multiplier Type	Number of Modules Used
Level 1	2-bit Multiplier	Basic Unit
Level 2	4-bit Multiplier	4 (2-bit modules)
Level 3	8-bit Multiplier	4 (4-bit modules)
Level 4	16-bit Multiplier	4 (8-bit modules)
Level 5	32-bit Multiplier	4 (16-bit modules)

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Conclusion and Future Scope

In this project, the **32-bit Vedic Multiplier based on a hierarchical structure** was successfully designed and implemented using the principles of Vedic mathematics. The design utilizes the **Urdhva–Tiryakbhyam (Vertical and Crosswise)** multiplication technique, which allows parallel generation of partial products and significantly improves the speed of multiplication. By adopting a hierarchical approach, smaller multiplier modules such as 2-bit, 4-bit, 8-bit, and 16-bit multipliers were systematically combined to construct the final 32-bit multiplier.

The hierarchical structure simplifies the design process, enhances modularity, and makes the multiplier more scalable for larger bit operations. Simulation and verification confirmed that the proposed multiplier performs accurate multiplication operations with improved speed and reduced propagation delay. Compared to conventional multiplier architectures, the Vedic multiplier provides better performance in terms of computational speed, hardware efficiency, and design simplicity. Therefore, the proposed design is suitable for high-speed digital systems and VLSI applications such as digital signal processing, communication systems, and embedded computing.

Future Scope

The proposed 32-bit Vedic multiplier can be further enhanced and extended in several ways to improve performance and applicability. In the future, the design can be implemented on **FPGA or ASIC platforms** to evaluate real-time hardware performance and power consumption. Advanced optimization techniques can also be applied to reduce area utilization and improve power efficiency.

The hierarchical Vedic multiplier architecture can also be extended to **64-bit or higher bit multipliers** for use in high-performance computing systems. Additionally, integrating the multiplier with other arithmetic units such as adders, subtractors, and accumulators can help develop efficient **Arithmetic Logic Units (ALUs)** for processors. Further research can also explore low-power design techniques and pipeline architectures to enhance the speed and efficiency of the multiplier for modern digital applications.

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