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DESIGN AND IMPLEMENTATION OF 32 BIT UNSIGNED MULTIPLIER USING CLAA AND CSLA

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ABSTRACT:

This project deals with the comparison of the VLSI design of the carry look-ahead adder (CLAA) based 32-bit unsigned integer multiplier and the VLSI design of the carry select adder (CSLA) based 32-bit unsigned integer multiplier. Both the VLSI design of multiplier multiplies two 32-bit unsigned integer values and gives a product term of 64-bit values. The CLAA based multiplier uses the delay time of 99ns for performing multiplication operation where as in CSLA based multiplier also uses nearly the same delay time for multiplication operation. But the area needed for CLAA multiplier is reduced to 31 % by the CSLA based multiplier to complete the multiplication operation. These multipliers are implemented using Altera Quartus II and timing diagrams are viewed through avan waves.
Keywords: Low Power, Ripple carry adder, Carry look ahead adder (CLAA), Carry select adder (CSLA), Unsigned Multiplier, Xilinx

I INTRODUCTION

High-speed data path logic systems are one of the most substantial areas of research in VLSI system design. The speed of addition is limited by the time required to propagate a carry through the adder in digital adders. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sumthe CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry. Design of high speed data path logic systems are one of the most substantial research area in VLSI system design. High-speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The basic idea of the proposed work is using n-bit binary to

excess-1 code converters (BEC) to improve the speed of addition.The detailed structure and function of BEC. This logic can be implemented with any type of adder to further improve the speed. The proposed 16, 32 and 64-bit adders are compared in this paper with the conventional fast adders such as carry save adder (CSA) and carry look ahead adder (CLA). This paper has realized the improved performance of the CSA with BEC logic through custom design and layout. The final stage CPA constitutes a dominant component of the delay in the parallel multiplier. Signals from the multiplier partial products summation tree do not arrive at the final CPA at the same time. This is due to the fact that the number of partial-product bits is larger in the middle of the multiplier tree. Due to un-even arrival time of the input signals to the final CPA, the selection of the ASIC Implementation of Modified Faster Carry Save Adder 54 final adder is an important work in parallel multipliers. Therefore decrease in carry propagation delay will result in major enhancement of the speed of the adder and multiplier. This paper is structured as follows. In Section 2, an overview of the 4-bit binary to excess-1 logic is provided. Section 3 deals with the proposed modified carry save adder (MCSA) architecture. Among the myriad of aggressive techniques, carry select adder (CSL) has been an eminent technique in the space-time tug-of-war of CPA design.

It exhibits the advantage of logarithmic gate depth as in any structure of the distant-carry adder family. Conventionally, CSL is implemented with dual ripple-carry adder (RCA) with the carry-in of 0 and 1, Respectively. Depending on the configuration of block length, CSL is further classified as either linear or square root. The basic idea of CSL is anticipatory parallel computation. Although it can achieve high speed by not waiting for the carry-in from previous sub-block before computation can begin, they consume more power due to doubling the amount of circuitry needed to do the parallel addition of which half of the speculative computations will be redundant. Digital Adders are the core block of DSP processors. The final carry propagation adder (CPA) structure of many adders constitutes high carry propagation delay and this delay reduces the overall performance of the DSP processor. This paper proposes a simple and efficient approach to reduce the maximum delay of carry propagation in the final stage. Based on this approach a 16, 32 and 64-bit adder architecture has been developed and compared with conventional fast adder architectures. This work identifies the performance of proposed designs in terms of delay-area-power through custom design and layout in process technology.

II.LITERATURE SURVEY

LITERATURE SURVEY 1:

Power-Delay Product Minimization in High-Performance 64-Bit Carry-Select Adders- Amaury Nève, Member, IEEE, Helmut Schechter, Thomas Ludwig, Member, IEEE. March 2004 This paper analyzes methods to minimize the power-delay product of 64-bit carry-select adders intended for high-

performance and low-power applications. A first realization in partially depleted (PD) silicon-on-insulator (SOI),using complex branch-based logic (BBL) cells. The reduction of the stack height in the critical path, combined with the optimization of the global carry network with cell sharing and the selection of 8-bit pre-sums, leads to a reduction of the power-delay product.

LITERATURE SURVEY 2:

A Low Power Carry Select Adder With Reduced Area- Yotmgjoon Kim and Lee-Sup Kim Department of EECS, KAIST, Korea 2001. A carry-select adder can be implemented by using single ripple carry adder and an add-one circuit instead of using dual ripple-carry adders. This paper proposes a new add-one circuit using the first zero finding circuit and multiplexers to reduce the area and power with no speed penalty. For bit length n = 64, this new carry-select adder requires fewer transistors than the dual ripple-carry carry-select adder and fewer transistors than Chang's carry-select adder using single ripple carry adder.

LITERATURE SURVEY 3:

An Area Efficient 64-Bit Square Root Carry-Select Adder For Low Power Applications Yajuan He, Chip-Hong Chang and Jiangmin Gu Centre for High Performance Embedded Systems, Nan yang Technological University, July 2005 In this paper, Carry-select method has deemed to be a good compromise between cost and performance in carry propagation adder design. However, conventional carry-select adder (CSL) is still area-consuming due to the dual ripple carry adder structure. The excessive area overhead makes CSL relatively unattractive but this has been circumvented by the use of add-one circuit introduced recently. In this paper, an area efficient square root CSL scheme based on a new first zero detection logic is proposed. The proposed CSL witnesses a notable power-delay and area-delay performance improvement by virtue of proper exploitation of logic structure and circuit technique.

III. PROBLEM OUTLINE

OBJECTIVE:

- The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with Cin = 1 in the regular CSLA to achieve lower area and power consumption.
- The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

EXISTING SYSTEM:

- High-speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem.
- High-speed data path logic systems are one of the most substantial areas of research in VLSI system design. The speed of addition is limited by the time required to propagate a carry through the adder in digital adders

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PROPOSED SYSTEM:

A structure of 4-bit BEC and the truth table is shown. How the goal of fast addition is achieved using BEC together with a multiplexer (mux) is described, one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial product results in parallel and the muxes are used to select either BEC output or the direct inputs according to the control signal Cin.

The Boolean expressions of 4-bit BEC are listed below

(**Note**: functional symbols, ~ NOT, & AND, ^ XOR).

X0 = ~ B0 (1)

X1 = B0 ^ B1 (2)

X2 = B2 ^ (B0 & B1) (3)

X3 = B3 ^ (B0 & B1 & B2)

XOR GATE MODEL:

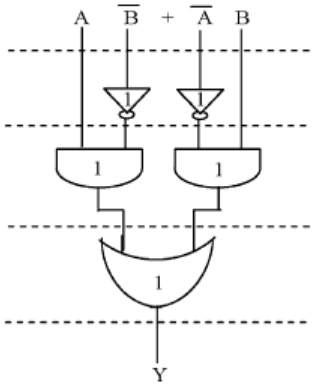

Figure 1: XOR gate model

ADAVANTAGES IN PROPOSED SYSTEM:

1. Better performance in power consumption.
2. Less number of gate counts.

IV. METHODOLOGY

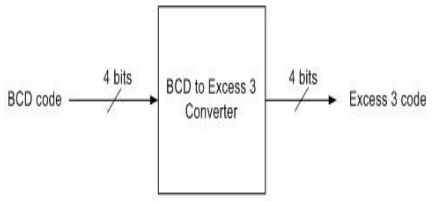

Figure 2: Block diagram of BCD To excess 3 code converter

The availability of a large variety of codes for the same discrete elements of information results in the use of different codes by different digital systems. It is sometimes necessary to use the output of one system as the input to another. A conversion circuit must be inserted between the two systems if each uses different codes for the same information. Thus, a code converter is a circuit that makes the two systems compatible even though each uses a different binary code. The bit combinations assigned to the BCD and excess-3 codes. Both BCD code and Excess 3 code use 4 bits to represent the numbers. But only 10 of 16 combinations are listed in the truth table. The rest 6 combinations not listed for the input variables are treated as don't cares.

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Therefore, the corresponding output variables can be assigned as either 1 or 0, whichever gives a simpler circuit.

Binary	Excess-1
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

TABLE 1: Truth Table of 4-Bit Binary To Excess-3

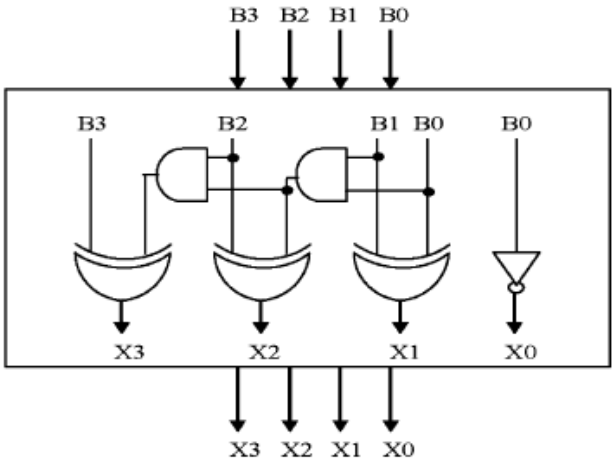

Figure 3: Structure for 4-Bit Binary to Excess-3 Code Converter

V.RESULTS

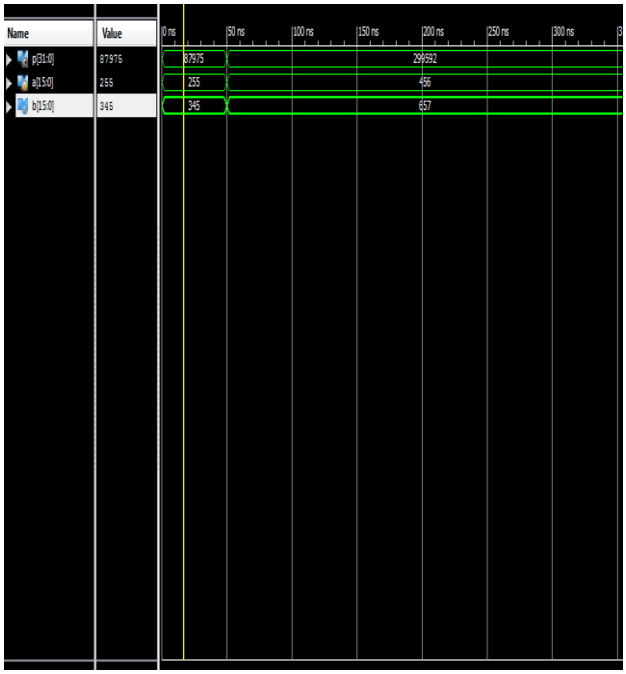

Fig 4: 32bit Multiplier By Using CLAA And CSLA

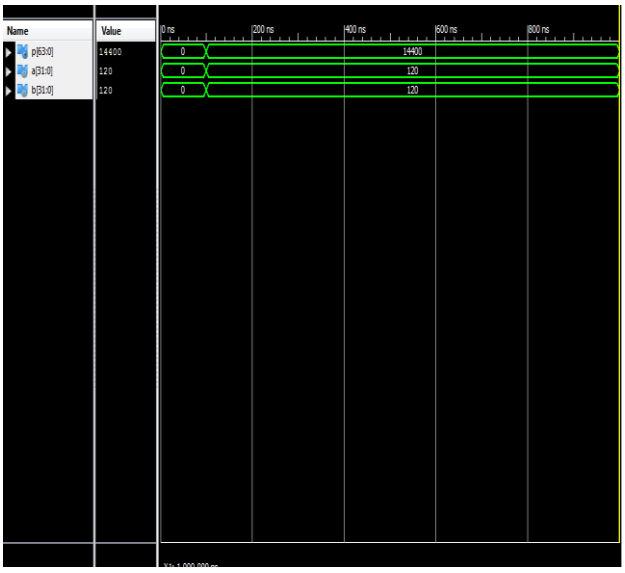

Fig 5:32 bit multiplier by using CSA

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VI.CONCLUSION

Fast adders have the advantage to scale better with increasing word widths, since the delay of the n-bit fast adders is O(log(n)) (carry-look ahead adder). It has been found that CLA occupies less area, Different bit Carry-look ahead adder design using Verilog HDL is successfully designed, simulated, tested and implemented onto the Spartan 3E FPGA. It is not possible to use CLA to realize constant delay for the wider-bit adders since there will be a substantial loading capacitance, and hence larger delay and larger power consumption. The CLA has the fastest growing area and power requirements with respect to the bit size. Similarly the other types of adders can also be designed and simulated using software and hardware used in this paper.Performance analysis of assorted adders is analyzed in terms of delay, frequency and memory from these carry choose adder is best parameter values than alternative adders. And also the regular carry choose is any changed for speed and space potency. A style and implementation of a HDL-based 32-bit Signed and unsigned multiplier factor with CLAA and CSLA was given. The ability analysis some same for each CLAA & amp CSLA. Therefore a 06 the world delay product reduction is feasible with the employment of the CSLA thirty two bit signed Array multiplier factor than CLAA based thirty two bit signed Array multiplier factor.The 32-Bit Carry Look Ahead Adder designed using cadence tool which has less delay and less power consumption and memory consumption is very low. Though compared with other different logic design approaches carry look ahead adder employed the great importance to reducing carry propagation delay of the adder..

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