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PERFORMANCE ANALYSIS OF 4-BIT MULTIPLIER USING 90NM TECHNOLOGY

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Abstract – This study looks at the performance of three different 4-bit multipliers built at the 90nm technology node utilizing a modified full adder. The research compares the efficiency of low-power, high-speed multiplier designs to that of CMOS counterparts. Given the multiplier module's significant power consumption and influence on circuit speed, the suggested multipliers attempt to optimize and improve overall circuit performance. Analyzing the findings of our study, we discover that the proposed multipliers provide significant advantages over CMOS-based designs, including up to approximately power reduction, decrease in delay, and approximately decrease in transistor count, increase in speed by using 90nm technology via Dtmos technology, and decrease in transistor count.

Index Terms – CMOS, Multiplier, Low Power Application, Delay, Power Dissipation, Area, Pass Transistor Logic (PTL), Adder.

I. INTRODUCTION

The evolution of integrated circuit technology has resulted in the creation of more complicated digital systems. Multipliers are essential in a variety of applications, including mathematical operations, digital signal processing, and error correcting codes. As a result, multiplier performance has a direct influence on the overall efficiency and functioning of these systems.

The constant desire for faster computing and reduced power usage has motivated academics to investigate novel techniques to creating efficient multipliers. This research focuses on the performance analysis of 4-bit multipliers utilizing the 90nm technology node in this context. The 90nm technology provides a good blend of circuit density and performance, making it a popular choice for many digital designs. The suggested multipliers attempt to minimize power consumption and improve circuit performance by implementing a modified full adder, addressing the problems associated with typical CMOS-based designs.

The purpose of this research is to compare the performance of the proposed low-power, high-speed multipliers to that of their CMOS equivalents. Power consumption, latency, and transistor count are the

major metrics of interest. We want to assess the usefulness of the suggested multipliers in boosting overall circuit efficiency by a thorough investigation. This study's findings will add to the body of knowledge on efficient multiplier designs and give insight into the trade-offs between power consumption, circuit speed, and transistor count. This understanding may be used to the design and optimization of digital systems in which multipliers play an important role. The next sections of this study will provide a full overview of the technique used, design considerations for the 4-bit multipliers, experimental setup, and data analysis. Finally, in the conclusion, the findings will be summarized and the implications for future study and practical implementations will be discussed. The necessity for integrating a larger density of capabilities on a single chip has grown as the integration scale has advanced. These features, however, come at a high cost in terms of energy consumption and computational power. Integrated circuit designers must now balance power dissipation, speed, and area issues [1].To overcome these issues, low-power system development has emerged as a crucial priority. The search of low-power designs is motivated by two basic factors. For starters, increasing integration capacity has resulted in increased current flow inside circuits, resulting in overheating of integrated circuits (ICs). This jeopardizes their dependability and lifespan. Second, low-power designs allow devices to run for extended periods of time even with limited battery capacity [2].Low-power design efforts have become critical for improving the overall performance and efficiency of integrated circuits. Designers may maintain the lifetime and dependability of ICs while also allowing for extended battery life in portable devices by minimizing power dissipation. As a result, researchers and engineers are constantly developing new approaches and procedures to reduce power consumption while maintaining processing capabilities.

This study digs into the world of low-power design and provides a thorough examination of the many strategies used to minimize power dissipation in integrated circuits. The parts that follow will go over the methodology, concerns, and experimental discoveries linked to low-power design, before going over the consequences and future possibilities in this sector. Multiplication is an important component in circuits since it is used in many signal processing techniques. The multiplier's performance has a direct influence on total system performance, and it is frequently the bottleneck due to its significantly slower functioning [3]. Multiplier design issues centre upon obtaining high speed while reducing space use. Full adders are widely used in multipliers, and increasing their efficiency can improve the multiplier's overall effectiveness. However, because area requirements and circuit speed are often inversely related, it is critical to find a compromise. As a result, there is a need to investigate various multiplier designs that give optimum speed and area limits. In this study, we introduce a complete adder based on Power Transmission Lines (PTLs) that is more efficient. This method is extended further by designing and analyzing two frequently used multipliers: the Wallace tree multiplier and the DADDA multiplier. The PTL-based complete adder is used to implement these multipliers. Simulations are run at the 90nm technology node using the

Cadence Virtuoso toolbox to evaluate their performance.

The simulations examine power consumption and delay characteristics, revealing information about the efficiency and efficacy of the suggested systems. We want to optimize the trade-off between speed and area in the planned multipliers by using the PTL-based full adder, hence improving their overall performance.

Array multiplier

An array multiplier is a type of digital circuit that performs binary number multiplication. It is a typical and basic multiplier implementation. An array multiplier is made up of numerous rows and columns of logic gates, often AND gates and adders. The multiplicand and multiplier input numbers are typically separated into bits and sent into the array multiplier. Each multiplier bit is linked to a row of AND gates, where it serves as a control signal. The multiplicand bits are linked to the AND gate columns. The AND gates' outputs are then linked to a series of adders, which add up the partial products formed by the AND gates. The array multiplier produces partial products for each bit combination of multiplicand and multiplier. Using the AND gates, the partial products are generated by conducting bit-wise multiplication between the multiplicand bits and their associated multiplier bits.

Wallace tree multiplier

The Wallace tree multiplier is a binary multiplier implementation. It is a digital circuit that can multiply binary values and produce partial products. Wallace tree implementation employs ordinary adders (Half adders and Full adders) and AND logic gates. Full and Half adders are used to sum partial products in stages until only two numbers remain. To decrease latency, parallel multipliers employ carry saving addition. Its multiplier design is frequently used in many memory units and CPUs. The delay of the Wallance tree is quite short.

Dadda multiplier

Dadda multiplier is a binary multiplier in hardware. It employs a variety of full and half adders to sum the partial results in phases until only two numbers remain. In comparison to all other multipliers, the Dadda multiplier requires the fewest amount of adders. As a result, the area of the multiplier is decreased, as is the speed, due to the reduction of partial products required at each level. The number of full and half adders required for the Dadda multiplier is determined on the size of the operands. Because of the serial multiplication procedure, the Dadda multiplier approach is sluggish. This design employs the Ripple Carry Adder (RCA).

Sequential multiplier

A Sequential multiplier is one of a design for multiplying two numbers which does include a clock signal and a reset signal. For an n-bit multiplicand and multiplier, the resulting product will be 2n-bits.

II. EARLIER WORKS

[1] The work presents a thorough investigation of the effect of contact thickness on the electrical properties of OTFTs. It includes the findings of experiments and

analyses carried out to better understand the link between contact thickness and device performance. The research investigates the adjustment of source and drain contact thickness to increase OTFT performance. The authors most likely carried out a series of experiments including the manufacture of OTFT devices with varying thicknesses of the source and drain contacts. To assess the effect of contact thickness on transistor behaviour, several electrical performance characteristics such as mobility, threshold voltage, and on/off ratio were measured and studied. Based on the information in the literature review, the study appears to add to the body of knowledge in the subject of organic electronics. The work gives useful insights for enhancing the design and manufacturing of organic electronic devices by examining the influence of contact thickness on OTFT performance. It is vital to remember that the evaluation is restricted to the material supplied because the entire document is not available. A more in-depth examination of the research methods, experimental design, and particular findings given in the publication may provide more insights into the study's importance and contributions to the area.

[2] The paper presents a prevalent show execution of a Wallace tree multiplier by utilizing a superior snake. The Wallace tree multiplier is a comprehensively used multiplier designing known for its useful and high speed duplication limits. The makers mean to overhaul the introduction of the Wallace tree multiplier by smoothing out the snake component. The paper most likely integrates an organized depiction of the proposed prevalent snake setup, including the progressions made to work on its efficiency and speed. The exploratory results, assessments, and examination are acquainted with show the show upgrades achieved by coordinating the predominant snake into the Wallace tree multiplier architecture .As a journal conveyance, the paper likely integrates a working study to spread out the interesting circumstance and meaning of the assessment. It is typical to give a total discussion of related works and component the outstanding responsibilities of the proposed first class show Wallace tree multiplier. Based on the gave information, the paper seems to address a huge point in the field of modernized circuit plan, expressly in the space of unrivalled execution duplication. The usage of a prevalent snake in the Wallace tree multiplier could achieve basic redesigns in speed and viability. In any case, without permission to the full paper, it is trying to give a more unmistakable assessment of the framework, preliminary game plan, and unequivocal revelations presented in the paper.

[4] The paper looks at the arrangement and execution of a prevalent show display multiplier using reversible reasoning structure. The makers plan to deal with the introduction of group multipliers by utilizing reversible reasoning, which thinks about the estimation of both the forward and in switch errands. Reversible reasoning has procured thought recently in view of its actual limit with respect to low power usage and unimportant force dispersal.

The paper most likely presents a point by point depiction of the proposed reversible reasoning based show multiplier plan. It could recollect discussions for the essential guidelines of reversible reasoning, the specific changes made to the display multiplier designing, and the connected benefits with respect to

control use, speed, or other execution metrics. Experimental results and examination are sensible given to show the show upgrades achieved by the proposed plan. The designers could have pondered the introduction of their reversible reasoning based bunch multiplier with conventional CMOS-based plans or other existing multiplier architectures. Given the information open, the paper appears to address a huge assessment district associated with capable increment circuits. Reversible reasoning offers promising advantages with respect to control viability, and the paper's responsibility lies in its application to the bunch multiplier designing. Regardless, without permission to the full paper, it is trying to give a more unequivocal overview of the methodology, preliminary game plan, and express disclosures presented in the paper.

[5] The paper bases on the arrangement and execution of a low-power display multiplier by utilizing a changed full adder. The makers mean to diminish the power use of bunch multipliers, which are routinely used for duplication errands in modernized circuits. By changing the full snake part, which is an essential piece of the multiplier, they hope to update power viability without making due with less on performance. The paper likely presents a low down portrayal of the proposed changed full snake plan and its compromise inside the group multiplier plan. The changes made to the full snake could integrate changes to the semiconductor estimating, reasoning entryways, or other circuit-level upgrades to reduce power consumption. Experimental results and assessment are sensible given to display the sufficiency of the proposed low-power bunch multiplier. The designers could have taken a gander at the power usage, delay, and other execution estimations of their changed arrangement with traditional group multipliers or other low-power multiplier architectures. Based on the open information, the paper keeps an eye on a critical point in mechanized circuit setup by focusing in on power improvement in show multipliers. Decreasing power usage in multipliers is critical for overall circuit capability, especially in flexible devices or applications where power prerequisites are significant. However, without permission to the full paper, it is attempting to give a more bare essential study of the procedure, exploratory game plan, and unequivocal revelations presented in the paper. Coincidentally, the paper's accentuation on low-power plan and the utilization of a changed full snake for bunch duplication prescribes its reasonable obligation to the field of successful modernized equipment.

[6] The maker keeps an eye on the necessity for fast duplication in electronic laptops and proposes a cunning method for managing further foster the duplication cycle. The paper presumably looks at the limitations of ordinary duplication techniques and highlights the upsides of the suggested Wallace tree multiplier. The paper likely gives an organized portrayal of the proposed multiplier configuration, getting a handle on its development, movement, and advantages. The Wallace tree multiplier means to chip away at the speed of duplication by diminishing the amount of fragmentary thing terms and redesigning the development process. As the paper was dispersed in 1964, it is seen as a leading work in the field of fast duplication. The Wallace tree multiplier has since transformed into a

comprehensively elaborate methodology in modernized circuit plan and basically influences further creating duplication performance. While the specifics of the framework and exploratory results may not be generally analyzed in this paper, it is a convincing obligation to the field. The Wallace tree multiplier is at this point alluded to and focused on in present day research, and its impact on the improvement of fast duplication computations is comprehensively recognized. Overall, the paper holds certain importance as it presents the possibility of the Wallace tree multiplier, which has transformed into a fundamental construction block in various duplication circuits. Its conveyance in a regarded IEEE journal shows its significance in the field of electronic laptops and automated circuit plan.

III. EXISTING METHOD

We explain Full Adder in the present way by designing in PTL logic. We use a suggested Full Adder (FA) circuit using Pass Transistor Logic (PTL) and a Half Adder (HA) circuit to handle the addition of intermediate bits in the multiplier. The FA circuit, which is based on PTL, is particularly intended to use just 10 transistors, as illustrated. Utilizing pass transistor logic.

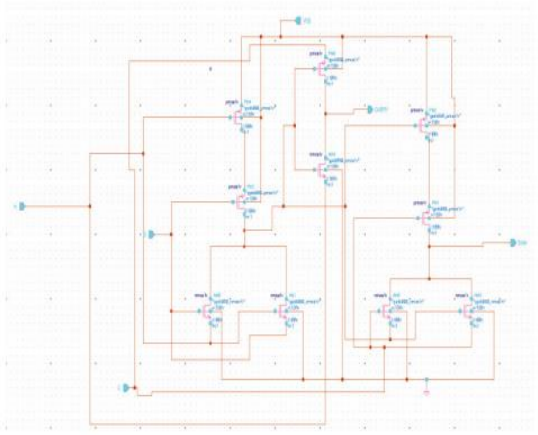

Fig 2 Proposed design PTL logic design of full adder

A complete adder is a digital circuit that adds three input bits: A, B, and a carry input (C_in), yielding a sum output (S) and a carry output (C_out). We may utilize a mix of NMOS (n-channel metal-oxide-semiconductor) and PMOS (p-channel metal-oxide-semiconductor) transistors to create a complete adder utilizing PTL technology. The main concept is to employ NMOS transistors for ground connections and PMOS transistors for V_dd connections..

IV. PROPOSED METHOD

We introduce unique multiplier structures that outperform conventional CMOS-based multiplier structures in terms of performance. We do simulations with the Tanner toolbox and 90nm technology. To handle the addition of intermediate bits in the multiplier, we suggest a Full Adder (FA) circuit that uses Pass Transistor Logic (PTL) and the DTMOS approach to decrease power consumption.

"Low power techniques" relate to numerous tactics and approaches used to reduce power consumption in

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the design and operation of electronic circuits and systems. These strategies are critical for battery-powered or power-constrained devices, as well as for lowering the environmental effect of electronic systems.

Dynamic Threshold MOS (DTMOS) is a CMOS (Complementary Metal-Oxide-Semiconductor) approach for dynamically controlling the threshold voltage of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). The threshold voltage is a critical characteristic that determines whether a MOSFET is ON or OFF. DTMOS enables this threshold voltage to be adjusted during operation, enabling flexibility in regulating power consumption and performance in integrated circuits.

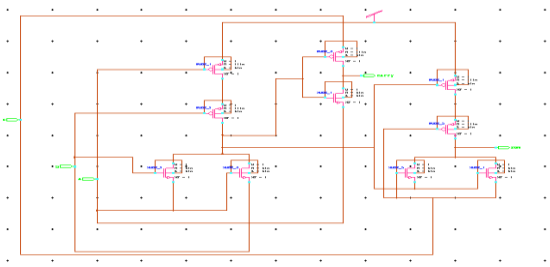

Fig 3 FULL ADDER USING DTMOS

While DTMOS has benefits in terms of performance and power optimization, its implementation might increase design complexity. Designers must carefully weigh the benefits of dynamic threshold modification against the added circuitry and associated production constraints. DTMOS is frequently used in high-performance computing, where the trade-off between power consumption and speed is critical..

The FA circuit, which is based on PTL, is especially intended to use just 10 transistors, and we are employing DTMOS without increasing the number of transistors. We accomplish a large decrease in the number of transistors by leveraging pass transistor logic, resulting in a lower total area.

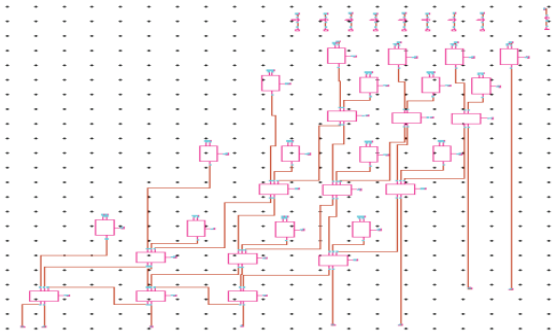

Fig 4 4x4 array multiplier

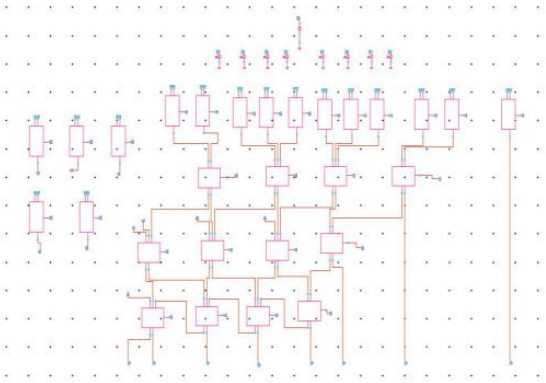

Fig 5 4x4 wallace tree multiplier

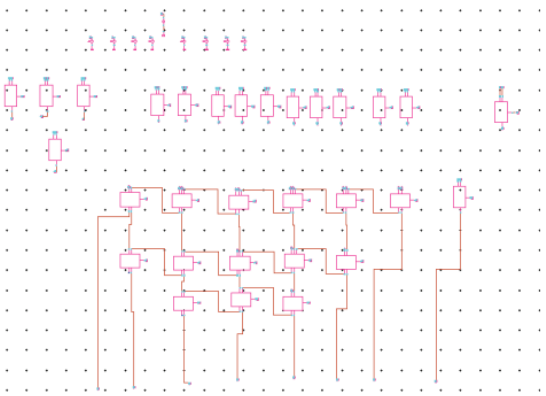

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Fig 6 4x4 dadda multiplier

A Full Adder (FA) is a digital circuit that takes three binary inputs (A, B, and a carry-in, C_in) and outputs two results: a sum output (S) and a carry output (C_out). Pass Transistor Logic (PTL) is a logic-implementation design approach that employs pass transistors.

V. RESULTS AND ANALYSIS

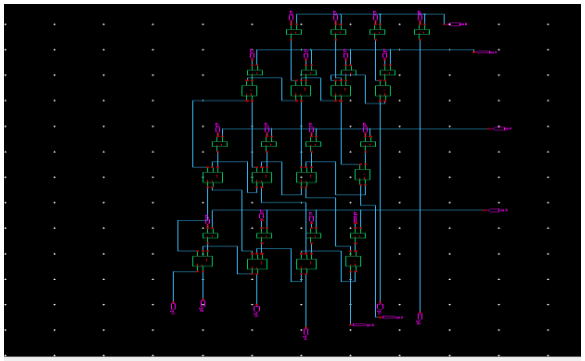

Fig 7 Schematic of 4x4 array multiplier

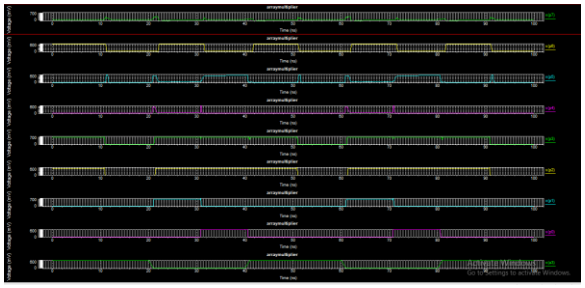

Fig 8 Waveforms of 4x4 array multiplier

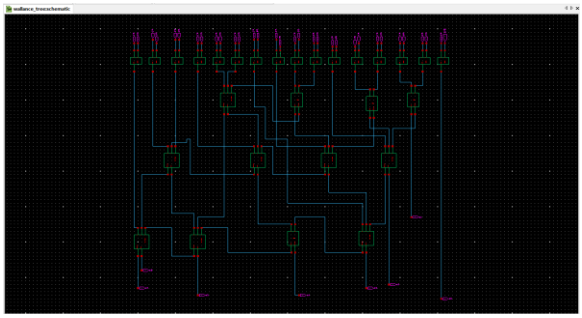

Fig 9 4x4 Wallace tree multiplier

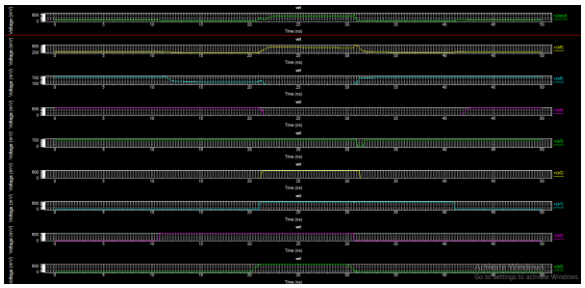

Fig 10 Wave form of 4x4 Wallace multiplier

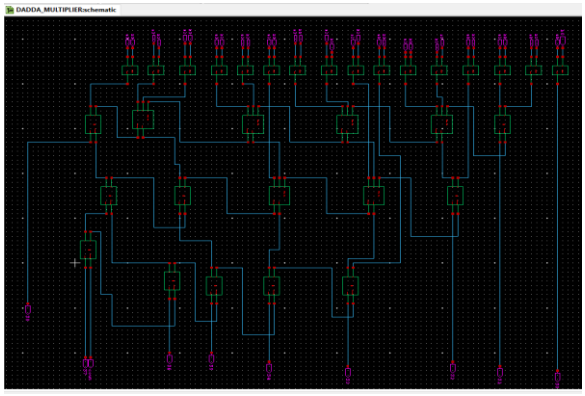

Fig 11 Schematic of 4x4 dadda multiplier

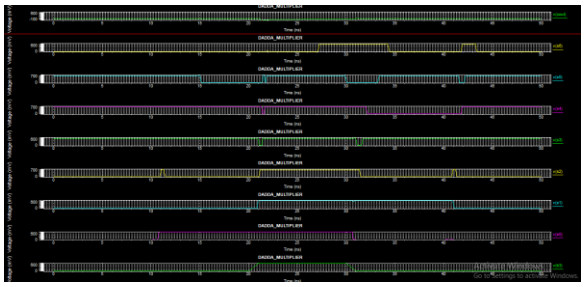

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Fig 12 Waveforms of 4x4 dadda multiplier

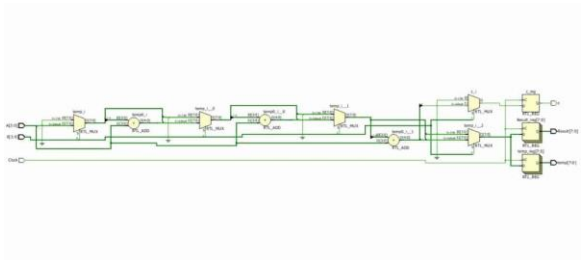

Fig 13 test Schematic of 4x4 sequential multiplier

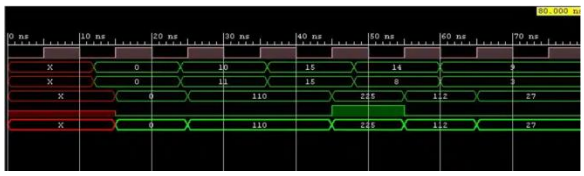

Fig 14 test Waveforms of 4x4 sequential multiplier

COMPARISON TABLE

Multipliers	Proposed -power	Extention- power	area	delay
Array	2.221345 e-003 w	5.383501 e-004 w	256	0
Wallace tree	1.936563 e-003 w	4.643622 e-004 w	256	0
Dadda	4.200127 e-003 w	6.393441 e-004 w	346	0/5.7314 e-010

CONCLUSION

We provide an analysis of three unique 4-bit multipliers developed by DTMOS TECHNOLOGY utilizing 90nm technology. Our investigation shows that the suggested array multiplier consumes the least amount of power, whereas the DADDA and Wallace tree multipliers have less latency. Additionally, the Wallace tree and array multipliers use less transistors. These results show the benefits of our suggested architectures, particularly in cases where multipliers are critical components of the circuit. Because of their adaptability, these structures may be used in a variety of applications, including Arithmetic Logic Units (ALUs) and Digital Signal Processors (DSPs).

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