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HIGH STEP-UP DUAL SWITCH CONVERTER WITH COUPLED INDUCTOR AND VOLTAGE MULTIPLIER FOR GRID CONNECTED SYSTEM

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ABSTRACT:

A novel high step-up converter, which is suitable for a PV cell is proposed in this paper. The proposed converter is composed of the dual switches structure, the coupled inductor, and voltage multiplier cells in order to achieve the high step-up voltage gain. The dual switches structure is beneficial to reduce the voltage stress and current stress of the switch. In addition, two multiplier capacitors are, respectively, charged during the switch-on period and switch-off period, which increases the voltage conversion gain. Meanwhile, the energy stored in the leakage inductor is recycled with the use of clamped capacitors. Thus, two main power switches with low on-resistance and low current stress are available. As the leakage inductor, diode reverse-recovery problem is also alleviated. Therefore, the efficiency is improved. This paper illustrates the operation principle of the proposed converter; discusses the effect of the leakage inductor; analyzes the influence of parasitic parameters on the voltage gain and efficiency, the voltage stresses and current stresses of power devices; and a comparison between the performance of the proposed converter and the previous high step-up converters is performed. In the ordinary voltage step-up situation, the conventional step-up converters, such as the boost converter can satisfy the voltage step-up requirement. However, in the high step-up situation, the conventional converter cannot achieve a high step-up conversion with high efficiency by extreme duty cycle or high turns ratio because of the parasitic parameters or leakage inductance.

Key Words: Dual switches, high step-up converter, switched capacitor, three-winding coupled inductor, Photo Voltaic System.

I. INTRODUCTION

In recent years, the boost dc/dc converters have been widely used to step up the renewable energy sources in various industrial applications such as ESS, UPS, and EV etc. In those applications, boost dc/dc converters generally step up the voltage to the high output. For that reason, to obtain a high voltage gain, many converter topologies were reported [3]-[6] for this application. Direct voltage step up using high frequency transformer is a Simple and easily controllable converter providing high gain. Isolated current
fed dc-dc converters [7]-[9] are example of this category. However, these topologies result in high voltage spikes across the switch (due to leakage inductance) and large ripple in primary side transformer current as the turn’s ratio in the high frequency transformer increases. Most of the non-isolated high voltage gain dc–dc power converters employ coupled inductor (to achieve higher voltage gain) [11] in contrast to a high frequency transformer used by the isolated versions. The coupled inductor-based dc–dc converter has advantages over isolated transformer-based dc–dc converter in minimizing current stress, using lower rating components and simple winding structure. Modeling procedure of the coupled inductor is described in [12]. For high power converter applications, interleaved coupled inductor-based boost converters [13]–[15] have also been proposed. Voltage gain of the converter can be increased without increasing the duty cycle of the switch by connecting an intermediate capacitor in series with the inductor [6]. The intermediate energy storage capacitor with coupled inductor charges in parallel and discharges in series with the coupled inductor secondary.

A demerit of coupled inductor-based systems is that they have to deal with higher leakage inductance, which causes voltage spikes across the main switch during turn-OFF time and current spike during turn-ON time, resulting in a reduction of the overall circuit efficiency. The effects of leakage inductance can be eliminated by using an active clamp network shown in [9], which provides an alternate path to recover leakage energy. But active clamp network is not as efficient as a passive clamp because of conduction losses across the power switch of the active clamp network. Active clamp network consists of a switch with passive components while passive clamp network [4] consists of passive components such as diode, capacitor, and resistor. The passive clamp circuit is more popular to reduce voltage stress across the converter switch by recycling leakage energy. To overcome such disadvantages of the conventional converters. A closed-loop control system, a sensor monitors the system output and feeds the data to a controller that adjusts the control to maintain the desired system output and hence remain unaffected to the external noise sources. A closed loop control has high reliability, easy implementation and output short circuit and overload protection.

In this paper, we propose coupled inductor boost converter that features low switch voltage stress and high gain. To achieves high voltage through a coupled inductor connected in interleaved manner that charges an intermediate buffer capacitor and a passive clamp network to recover the leakage energy. Coupled inductor leads to the incorporation of “turn’s ratio” into the gain expression that leads to high efficiency without increasing the duty ratio. As compared to existing high-gain dc–dc converters, the number of passive components used in the proposed converter is less, which reduces the cost and improves the efficiency. Though the proposed converter is applicable to any low voltage source applications such as solar PV, fuel cell stack, battery, etc. The typical renewable energy system is shown in Fig.1. The system can convert the low voltage from
the fuel cells source and photovoltaic cells source into the high voltage via the high step-up converter, and, then, the renewable energy is transformed into the load and utility through the inverter. Therefore, the high step-up converter is indispensable.

![Fig.1. Typical renewable energy system](image)

**II. OPERATION PRINCIPLE OF THE DUAL SWITCHES CONVERTER**

Fig.2 shows the circuit topology of the proposed converter. The equivalent circuit model of the three-winding coupled inductor includes the magnetizing inductance $L_m$, the leakage inductance $L_k$, and an ideal transformer with primary winding $N_1$ turns and two secondary windings $N_2$ and $N_3$ turns. The proposed converter consists of two active switches, five diodes, and five capacitors. The switches $S_1$ and $S_2$ share the same operation signal and one control circuit is needed. The leakage inductor energy of the coupled inductor is recycled to the capacitors $C_1$ and $C_2$, and the voltage spikes on the switches are significantly reduced. This makes low conducting resistance $R_{ds(on)}$ of the switches available. Thus, the efficiency is upgraded and the high step-up conversion gain can be achieved. Also, the voltages across the capacitors $C_3$ and $C_4$ can be adjusted by the turns ratio of the coupled inductor. To simplify the circuit analysis of the proposed converter, the following assumptions are made:

1) The Capacitors $C_1$, $C_2$, $C_3$, $C_4$, and $C_0$ is large enough; thus, $V_{C1}$, $V_{C2}$, $V_{C3}$, $V_{C4}$, and $V_0$ are regarded as constant values;
2) The power devices are ideal, but the parasitic capacitors of the switches are considered;
3) The coupling coefficient of the coupled inductor $k$ is equal to $L_m / (L_m + L_k)$, and the turns ratio of the coupled inductor is $N_1 : N_2 : N_3 = 1 : 1 : N$. The primary winding with $N_1$ turns, two secondary windings with $N_2$ and $N_3$ turns of the ideal transformer with are, respectively, represented by $L_1$, $L_2$ and $L_3 (L_1 : L_2 : L_3 = 1 : 1 : N_2)$.

![Fig.2. Circuit configuration of the proposed converter](image)
The operating principles for the continuous conduction mode (CCM) are analyzed in detail herein. Fig.3 shows the typical waveforms of the proposed converter during one switching period. Fig.4 shows the topological stages of the proposed converter.

The eight operating modes are described as follows.

**A. CCM Operation**

**Mode I \([t_0, t_1]\):** In this transition interval, the switches \(S_1\) and \(S_2\) start to conduct. Diodes \(D_1, D_2, D_3,\) and \(D_0\) are reverse biased. Diode \(D_4\) is forward biased. The current flow path is shown in Fig.4 (a). The leakage inductance \(L_k\) and magnetizing inductance \(L_m\) are charged by the input source \(V_{in}\). The inductor \(L_2\) is also charged by the input source. The leakage inductor current \(i_{L_k}\) increases linearly. Due to the leakage inductance, the inductor current \(i_{L_3}\) and diode current \(i_{D_4}\) decrease slowly. Therefore, the voltage of diode \(D_3\) is clamped by input source \(V_{in}\), clamped voltages \(V_{C1}\) and \(V_{C4}\); the voltage of diode \(D_0\) is clamped by blocking voltages \(V_{C3}, V_{C4},\) and \(V_{C2}\). The voltage steps are formed. The output capacitor \(C_o\) provides the energy to load \(R\). When the current \(i_{D_4}\) becomes zero (i.e., \(i_{L_k} = i_{L_m}\)), this operating mode ends.
Mode II \([t_1, t_2]\): In this transition interval, the switches are still turned on. Diode \(D_3\) is forward biased. Diodes \(D_1, D_2, D_4\), and \(D_0\) are reverse biased. The current flow path is shown in Fig.4 (b). The magnetizing inductance \(L_m\) and inductor \(L_2\) are charged in parallel by the input source \(V_{in}\). Some of the energy from the input source \(V_{in}\) transfer to the inductor \(L_3\) to charge blocking capacitor \(C_4\) with the input source \(V_{in}\), blocking voltages \(V_{C1}, V_{C3}\) together. The output capacitor \(C_o\) provides the energy to load \(R\). When the switches are turned off at \(t = t_2\), this interval is finished.

Mode III \([t_2, t_3]\): In this transition interval, the switches are turned off. Diodes \(D_1, D_2, D_3\) are forward biased. Diode \(D_0\) is reverse biased. Fig.4(c) shows the current-flow path. The energies of the leakage inductance \(L_k\) and magnetizing inductance \(L_m\) are released to the parasitic capacitors of the switches, respectively. The blocking capacitor \(C_4\) is still charged. The output capacitor \(C_o\) provides the energy to load \(R\). When the diodes \(D_1\) and \(D_2\) are forward biased at \(t = t_3\), this operating mode ends.

Mode IV \([t_3, t_4]\): In this transition interval, the switches are turned off. Diodes \(D_1, D_2, D_3\) are forward biased. Diode \(D_0\) is reverse biased. The current flow path is shown in Fig.4 (h).
reverse biased. Fig.4 (d) shows the current-flow path. The energies of the leakage inductance $L_k$ and magnetizing inductance $L_m$ are released to the clamped capacitor $C_1$ and energy of the inductor $L_2$ is transferred to the clamped capacitor $C_2$. The blocking capacitor $C_4$ keeps charging. In addition, due to the leakage inductance, and the diode current $i_{D3}$ keeps flowing through diode $D_1$; therefore, the voltage across the diode $D_4$ is clamped by the blocking voltage $V_{C4}$. The output capacitor $C_0$ provides the energy to load $R$. When the currents $i_{D3}$, $i_{C3}$, and $i_{L3}$ decrease to zero at $t = t_4$, this operating mode ends.

**Mode V** [$t_4$, $t_5$]: In this transition interval, the switches are turned off. Diodes $D_1$, $D_2$, and $D_0$ are forward biased. Diodes $D_3$ and $D_4$ are reverse biased. The current-flow path is shown in Fig.4 (e). The energies of the leakage inductance $L_k$ and the magnetizing inductance $L_m$ are released to the clamped capacitor $C_1$ and the energy of inductor $L_2$ is transferred to the clamped capacitor $C_2$. The diode current $i_{D0}$ increases almost at a constant slope. The input source $V_{in}$, three-winding coupled inductor, and the blocking voltage $V_{C4}$ are connected in series to charge the output capacitor $C_0$ and provide energy to the load $R$. When the diode current $i_{D0}$ is equal to diode current $i_{D2}$ (i.e., capacitor current decreases to zero) at $t = t_5$, this operating mode is finished.

**Mode VI** [$t_5$, $t_6$]: In this transition interval, the switches are turned off. Diodes $D_1$, $D_2$, and $D_0$ are forward biased. Diodes $D_3$ and $D_4$ are reverse biased. The current-flow path is shown in Fig.4 (f). The operating mode is almost the same as Mode V except that the capacitor $C_2$ is discharged instead of charged. When the diode $D_4$ is forward biased at $t = t_6$, this operating mode ends.

**Mode VII** [$t_6$, $t_7$]: In this transition interval, the switches are turned off. Diodes $D_1$, $D_2$, $D_3$, and $D_0$ are forward biased. Diode $D_4$ is reverse biased. The current-flow path is shown in Fig.4 (g). The energies of the leakage inductance $L_k$ and the magnetizing inductance $L_m$ are released to the clamped capacitor $C_1$. The inductor $L_2$ and the capacitor $C_2$ are connected in parallel to discharge the energies to the load and the output capacitor $C_0$.

Meanwhile, the input source $V_{in}$, inductors $L_1$ and $L_2$, as well as the blocking voltage $V_{C4}$ provide energy to the output capacitor $C_0$ and the load $R$. The output diode current $i_{D0}$ drops almost at a constant slope. In addition, the part energy of the inductor $L_2$ is transferred to the capacitor $C_3$. When the diode currents $i_{D1}$ and $i_{D2}$ are equal to zero at $t = t_7$, this operating mode ends.

**Mode VIII** [$t_7$, $t_8$]: In this transition interval, the switches are turned off. Diodes $D_3$ and $D_0$ are forward biased. Diodes $D_1$, $D_2$, and $D_4$ are reverse biased. The current-flow path is shown in Fig.4 (h). The leakage inductance $L_k$, the magnetizing inductance $L_m$, the input source $V_{in}$, the inductor $L_3$, the blocking voltage $V_{C4}$, and the clamped capacitor voltage $V_{C2}$ are connected in series to provide energy to the output capacitor $C_0$ and the load $R$. Meanwhile, capacitor $C_3$ keeps charging.

The voltages across the diodes $D_1$ and $D_2$ are clamped by the windings of the coupled inductor and the clamped capacitors $C_1$ and $C_2$. Therefore, the voltage steps of diodes $D_1$ and $D_2$ are formed, and the voltage drops of the switches are obtained. The output diode current $i_{D0}$ drops linearly. When the output diode $D_0$ is
reverse biased at \( t = t_8 \), this operating mode ends. When the switches are turned on, the new switching period begins.

### III. PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

#### A. Voltage Gain Expression

When the proposed converter operates in the switching-on state, the following equations can be found in Fig.4 (b):

1. \[ V_{L_{im}} = kV_{in} \quad (1) \]
2. \[ V_{L_k} = (1 - k) V_{in} \quad (2) \]

At modes V–VII, the energies of the leakage inductors are released to the capacitors \( C_1 \) and \( C_2 \). According to Tang et al, the duty cycle of the released energy can be approximately obtained

3. \[ D_c = \frac{2(1 - D)}{(N + 1)} \quad (3) \]

By using the volt–second balance principle on the leakage inductance \( L_k \) and magnetizing inductor \( L_m \), the voltages of \( L_k \) and \( L_m \) are found as

4. \[ V_{L_{im}} = \frac{DkV_{in}}{1 - D} \quad (4) \]
5. \[ V_{L_k} = \frac{D(1-k)(N+1)V_{in}}{2(1-D)} \quad (5) \]
6. \[ V_{N_3} = \frac{NDkV_{in}}{1 - D} \quad (6) \]

The voltages of capacitors \( C_1, C_2, C_3, \) and \( C_4 \) can be expressed as

7. \[ V_{C_3} = \frac{NDkV_{in}}{1 - D} \quad (7) \]
8. \[ V_{C_1} = V_{C_2} = V_{L_k} + V_{L_{im}} = \frac{V_{in}D(1 + k) + N(1 - k)}{2(1 - D)} \quad (8) \]
9. \[ V_{C_4} = V_{in} + V_{C_1} + V_{C_3} + V_{N_3} \]

Then, based on the capacitor charge balance, during the time interval \([t_0, t_2]\), the average current of capacitor \( C_1 \) can be written as

10. \[ I_{C1}[t_0, t_2] = I_o/D \quad (17) \]

Therefore, the currents of secondary-side \( N_3 \) of the coupled inductor can be obtained

11. \[ I_{N3}[t_0, t_2] = \frac{I_o}{D} \quad (18) \]
12. \[ I_{N3}[t_2, t_8] = \frac{I_o}{1 - D} \quad (19) \]

During the time interval \([t_2, t_8]\), while using KCL, at junction points of the primary side \( N_1 \) of the coupled inductor, diode \( D_1 \) and capacitor \( C_4 \), the average current of the leakage inductor can be expressed

\[ G_k = \frac{V_o}{V_{in}} = \frac{V_{C_1} + V_{C_2} + V_{C_3} + V_{C_4} + V_{in}}{V_{in}} \]

According to (7)–(9), collecting the terms, the voltage gain can be expressed as

\[ G = \frac{V_o}{V_{in}} = \frac{2 + Nk + D(N(1.5 - 0.5k) + (1.5k - 0.5))}{1 - D} \quad (10) \]

\[ V_{S_1} = V_{S_2} = V_{D1} = V_{D2} = \frac{V_{in} = \frac{V_0}{1 - D} + \frac{D(N + 1)}{1 - D}}{2 + N + (N + 1)D} \quad (11) \]

\[ V_{D4} = \frac{NV_{in}}{1 - D} = NV_0 / (2 + N + (N + 1)D) \quad (12) \]

\[ V_{D3} = V_{D0} = \frac{(N + 1)V_{in}}{1 - D} = \frac{(N + 1)V_0}{2 + N + (N + 1)D} \quad (13) \]

\[ I_{D0(t_2, t_8)} = I_o / (1 - D) \quad (14) \]

\[ I_{D1(t_2, t_7)} = I_{D2(t_2, t_7)} = I_o / D_c \quad (15) \]

Using KCL, at junction points of the primary side \( N_1 \) of the coupled inductor, diode \( D_1 \) and capacitor \( C_4 \), the average current of the leakage inductor can be expressed
Then, the RMS values of the switches $S_1$ and $S_2$ are

\[
I_{\text{RMS-}S_1} = \sqrt{\frac{1}{T_S} \int_0^{DT_S} \left( I_{N_1[t_0,t_2]} + \frac{I_o}{D} - 0.5\Delta I_L + \frac{\Delta I_L}{DT_S}t \right)^2 dt}
\]

\[
I_{\text{RMS-}S_2} = \sqrt{\frac{1}{T_S} \int_0^{DT_S} \left( I_{N_2[t_0,t_2]} - 0.5\Delta I_L + \frac{\Delta I_L}{DT_S}t \right)^2 dt}
\]

\[
dl = \frac{2D + N + DN}{2D(1-D)} I_o \sqrt{\frac{K^2}{12} + 1}
\]

(23)

Where

\[
M = \frac{2 + N + D(N+1)}{1-D} \frac{V_{th}}{V_{th}} - \frac{\frac{4R_D + (4N+6)R_L}{R(1-D)}}{R + N + R_L}
\]

(24)

IV. MATLAB/SIMULINK RESULTS

Fig.5 shows the matlab/Simulink model of the proposed system.

Fig.6 shows the simulation waveforms of the proposed system like diode voltages and switch voltages.

Fig.7 shows the output voltage of the proposed converter.
V. CONCLUSION

The paper introduces closed loop control of high step up dual switch converter with coupled inductor and voltage multiplier cell for secondary grid connected applications. An additional control freedom is provided by the voltage multiplier cell to achieve extremely high voltage conversion ratio and to minimize the current ripple. The energy stored in the leakage inductance of the coupled inductor is recycled by using switched capacitors. The voltage stress across the main switch is reduced. Here the gate signals are generated using PWM control schemes. The proposed converter operated under open-loop & closed loop manner. The proposed converter has successfully implemented an efficient high step-up conversion through the voltage multiplier module. The interleaved structure reduces the input current ripple and distributes the current through each component. In addition, the lossless passive clamp function recycles the leakage energy and constrains a large voltage spike across the power switch. Meanwhile, the voltage stress on the power switch is restricted and much lower than the output voltage.

REFERENCES


Fig.8 shows the proposed converter with grid connected system

Fig.9 shows the grid outputs of grid voltage and gris current

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