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FPGA Implementation of Fault Tolerant & High Speed Reversible Systolic Multiplier

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Abstract—Multiplier is one of the essential components in the digital world such as in digital signal processing, quantum computing, microprocessor and widely used in arithmetic unit. The Reversible rationale is a used to decrease heat scattering and data misfortune. Contrasted with all essential math activities, multiplication requests all the more preparing time and look for complex equipment. This paper presents a plan of low power Systolic Array Multiplier utilizing Reversible logic gates which performs information handling in parallel. In this paper, we present a high speed 4x4 Systolic Multiplier design by using peres gate and toffoli gates and source code written in verilog and also implemented on FPGA Spartan 3s50pq208-4. The synthesis and simulation is done on Xilinx ISE 14.7. The delay is 17.642ns and static power dissipation is 24mW.

Keywords– FPGA, Reversible Logic, Systolic Multiplier, Verilog, Xilinx ISE 14.7, Spartan 3, Peres Full Adder(PF), Toffoli Gate(TG).

INTRODUCTION

In the region of advanced sign handling, systolic exhibit are perceived as a standard intended for rapid execution. A systolic array created by interconnecting a set of similar data-processing cells in a uniform manner and is closely related conceptually to arithmetic pipeline [1].

Equal cluster multipliers are utilized to accomplish low force and rapid. Multipliers are lapsed to address the issues in different DSP frameworks [2]. Reversible logic has an incredible consideration in the current years because of diminished power dispersal which assumes the principle part in low power VLSI plan. It is utilized in wide applications in low power CMOS and optical data preparing, nano innovation and quantum figuring. Irreversible calculation brings about energy dispersal because of the data misfortune. The warmth scatters since loss of the slightest bit of data is exceptionally little at room temperature however when more number of pieces are builds then in the circuits of fast computational works the warmth dispersed by them will

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influences the presentation and results in the failure of segments. The main importance's of adopting reversible logic makes fault tolerant and less power dissipation.

In 1973, Bennett demonstrated that to dodge energy setback it is crucial that all the computations must be acted in a reversible way [3]. In like manner to take out power dispersal, circuits should be created from reversible gates. In this manner each future advancement needs reversible logic to minimize the dissipation of power. Standard logic gates are irreversible. The reversible logic information vector can be recovered from the yield vector.

PROPOSED SYSTOLIC MULTIPLIER USING REVERSIBLE LOGIC

Systolic exhibits are frequently hard-wired for specific activities, as increase and gather, to perform particularly especially parallel integration, correlation, convolution, matrix multiplication or data sorting tasks. This type of systolic multipliers is used for Machine Learning (ML) applications. The proposed systolic array multiplier has designed by using reversible logic gates like toffoli gate and peres gate as shown in fig.4. The top module of toffoli gate is shown in fig.1. The peres full adder is designed using two peres gate is shown in fig.2. This peres full adder produces two garbage outputs.

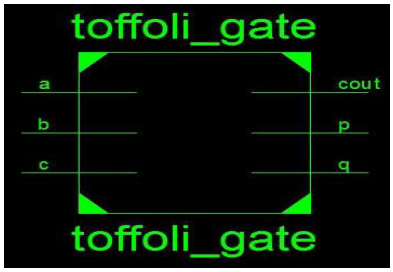

Fig. 1 Top module of Toffoli Gate (TG)
Where, p=a, q=b, cout=(a&b)^c

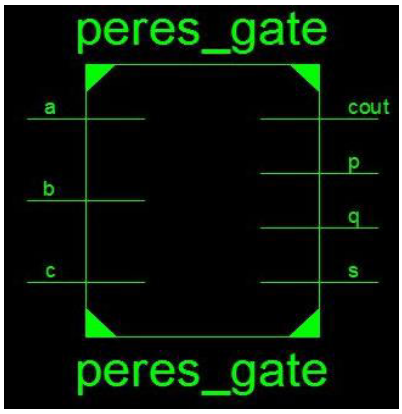

Fig.2 Top module of Peres Full Adder (PF)
Where, p=a, q=a^b, s=a^b^c, cout=((a^b)&c)^(a&b)

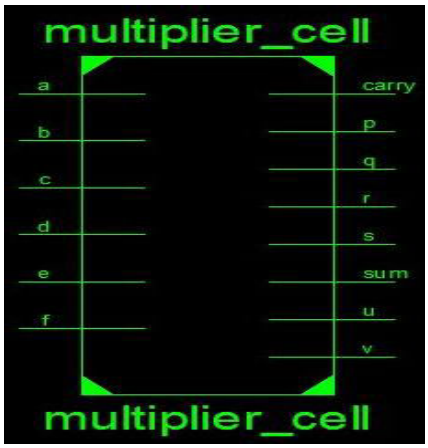

Fig.3 Top Module of Multiplier Cell

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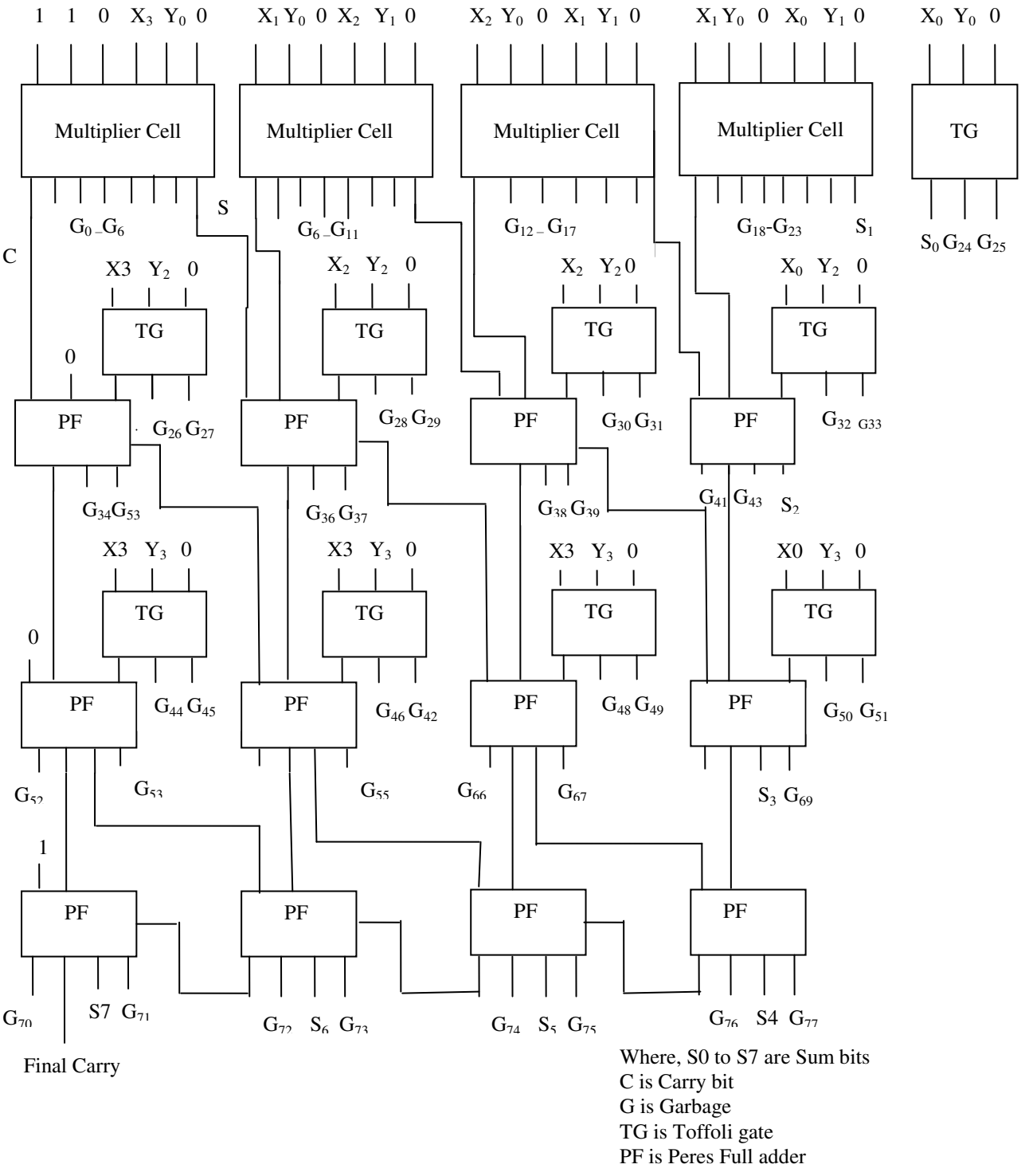

Fig.4 Block diagram of Systolic Multiplier using Reversible Logic

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Where, p=a
q=b
r=e
s=(d&e)^f
u=(a&b)^c
v=(a&b)^c
sum=(a&b)^(d&e)
carry=(a&b)&(d&e)

The multiplier cell is shown in above fig. 3. Internally it consists of 2 toffoli gate and 1 peres full adder(PF).

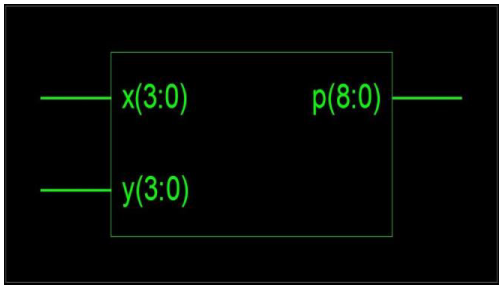

Fig.5 Top module of systolic multiplier

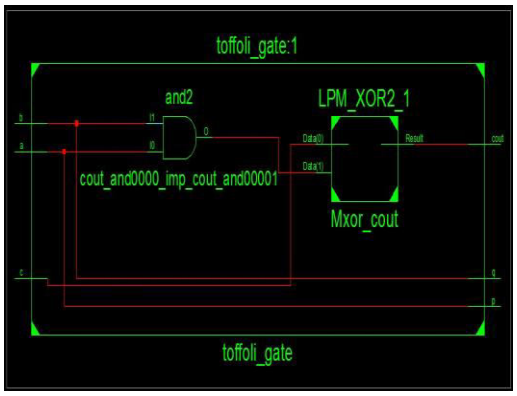

Fig.6 RTL Schematic of Toffoli gate(TG)

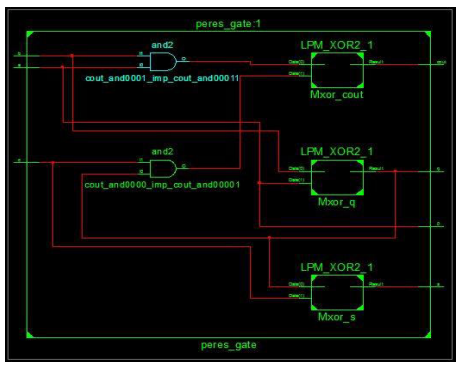

Fig.7 RTL Schematic of Peres Full Adder(PF)

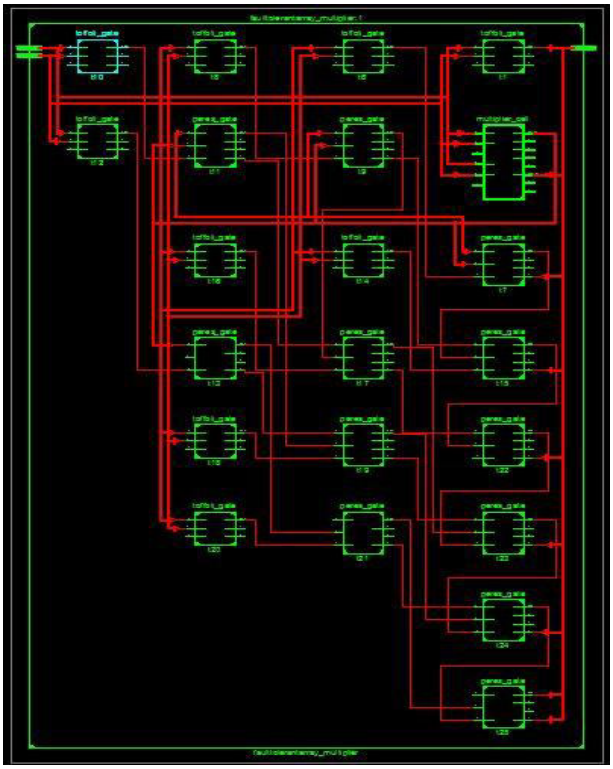

Fig.8 RTL Schematic of Systolic Multiplier based on reversible logic

Simulation Results

Fig.9 Simulation of Systolic multiplier in radix-binary

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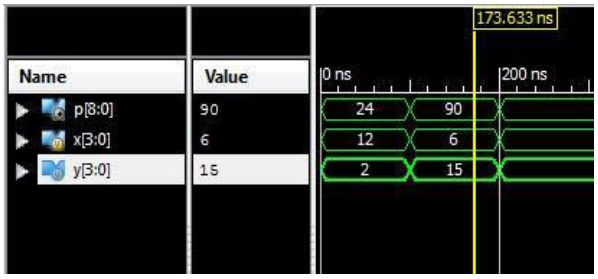

Fig.10 Simulation of Systolic multiplier in radix-decimal

FPGA IMPLEMENTATION RESULTS

Design Object List - I/O Pins

I/O Name	I/O Direction	Loc	Bank	I/O
p<0>	Output	p20	BANK7	
p<1>	Output	p26	BANK7	
p<2>	Output	p28	BANK6	
p<3>	Output	p34	BANK6	
p<4>	Output	p36	BANK6	
p<5>	Output	p39	BANK6	
p<6>	Output	p42	BANK6	
p<7>	Output	p44	BANK6	
p<8>	Output	p46	BANK6	
x<0>	Input	p21	BANK7	
x<1>	Input	p27	BANK7	
x<2>	Input	p29	BANK6	
x<3>	Input	p35	BANK6	
y<0>	Input	p37	BANK6	
y<1>	Input	p40	BANK6	
y<2>	Input	p43	BANK6	
y<3>	Input	p45	BANK6	

Fig.11 UCF file generation

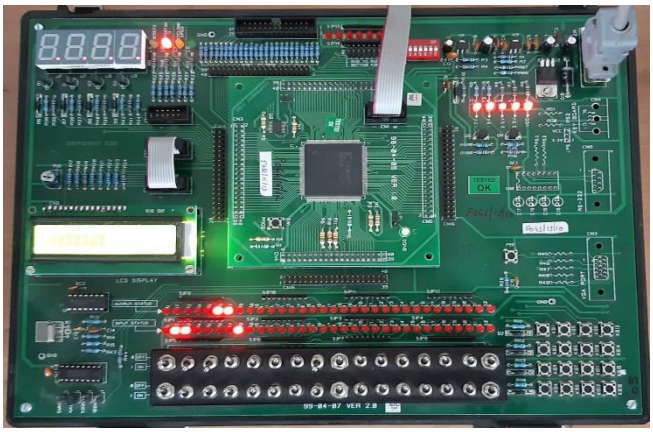

Fig.12 FPGA Implementation Results(i) Case 1. Here, Inputs are x=0110 and y=0001, the output of systolic multiplier is p=00000110.

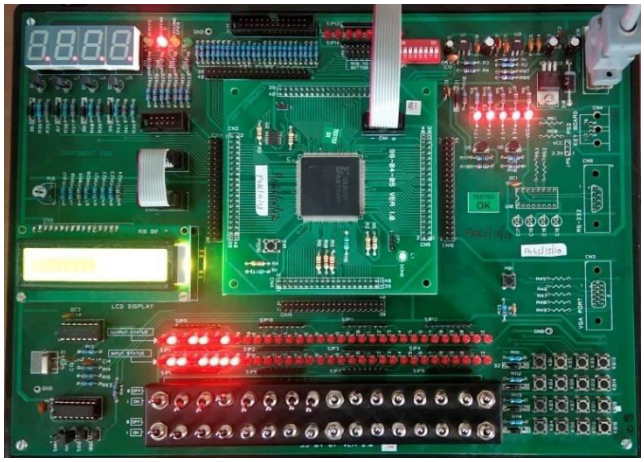

Fig.13 FPGA Implementation Results(ii) Case 2. Here, Inputs are x=0110 and y=1111, the output of systolic multiplier is p=01011010.

SYNTHESIS RESULTS

Power summary		I(mA)	P(mW)
Total estimated power consumption			24
Total Vccint	1.20V	5	6
Total Vccaux	2.50V	7	18
Total Vcco25	2.50V	0	0

Device utilization

Device	:	3s50pq208-4		
Slices	:	16	out of 768	2%
4 input LUTs	:	27	out of 1536	1%
IOBs	:	17	out of 124	13%

Timing Report

Speed Grade: -4

Total 17.642ns (9.771ns logic, 7.871ns route)

Total Memory Usage is 235488 kilobytes.

Table1: Comparison of Delay

Performance Parameter	Proposed Work	S. Subathradevi [4]
Delay (ns)	17.642	42.809

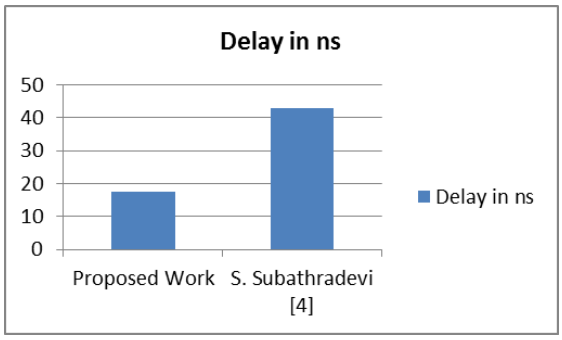

Fig.14 Delay comparison

CONCLUSION

This paper provides the design of high speed systolic multiplier based on reversible logic gates using verilog coding. This design implemented on FPGA Spartan 3s50pq208-4 and verified the outputs. The delay is minimized (17.642ns) and static power consumption is 24mW.

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