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MULTI LEVEL INVERTER TOPOLOGIES WITH REDUCED DEVICE COUNT FOR INDUCTION MOTOR APLLICATIONS

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Abstract-Multilevel inverter offer high power capability, associated with lower output harmonics and lower commutation losses. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. This paper proposes a multilevel inverter with reduced number of switches for induction motor drive application, multilevel inverter with reduced number of switches. The inverter is capable of producing levels of output-voltage levels from the dc supply voltage. This paper proposes a new multilevel inverter topology using reduced number of auxiliary switches. The new topology produces a significant reduction in the number of power devices and switches required to implement a multilevel output using the induction motor applications. The inverter is capable of producing levels of output-voltage levels from the dc supply voltage. This paper proposes a new multilevel inverter topology using reduced number of auxiliary switches. Reduction in overall part count as compared to the classical topologies has been an important objective in the recently introduced topologies. In this paper, some of the recently proposed multilevel inverter topologies with reduced power switch count are reviewed and analyzed. The paper will serve as an introduction and an update to these topologies, both in terms of the qualitative and quantitative parameters. Multilevel inverters are used in high voltage AC motor drive, distributive generation, high voltage direct transmission as well as SVC applications. The concept of an MLI to achieve higher power is to use power semiconductor switches along with several lower voltage dc levels to perform the power conversion by synthesizing a staircase voltage levels. And also Extension of this paper is Single phase topology is extended to three phase topology and fed with an induction motor drive.

Index Terms—Even power distribution, fundamental switching frequency operation, multilevel inverters (MLI), reduced device count, source configuration.

(I) Introduction

From many years, Induction motor drives have been popularly used for variable speed control applications in industries. This is because the induction motor is simple in construction and requires less maintenance. In recent times, multilevel inverters (MLI) are gaining popularity and widely used for induction motor drive applications [1-3]. It is especially used for medium to high voltage and high current drive applications. There are many advantages of multilevel inverters as compared to conventional inverters. Main advantages are low total harmonics distortion (THD), low switching losses, good power quality and reduced electromagnetic interference (EMI). Main feature of multilevel inverter is that it reduces voltage stress on each component [4-8]. The topologies of multilevel inverters are classified into three types. They are flying capacitor, diode clamped and H-bridge cascaded multilevel inverters.

H-bridge multilevel inverter is one of the most popular inverter topology used in high-power medium voltage (MV) drives. It is composed of a multiple units of single-phase H-bridge power cells. In practice, the number of power cells in an H-Bridge inverter is mainly determined by its operating voltage and manufacturing cost. H-bridge multilevel inverter requires the least number of components for the same voltage level as compared to all three types of inverter [9-11].

More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission and most recently for medium voltage induction motor variable speed

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drives [12-15].Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, Flexible AC Transmission System (FACTS) and traction drive systems.

In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, static VAR compensators and renewable energy systems. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters. This paper presents an optimized configuration of a3-phase MLI with minimum number of switches. To overcome the disadvantages this paper proposes anew multilevel inverter topology with reduced switches compared to conventional MLIs. Finally the induction motor fed by the proposed MLI is presented in this paper.

(i) Multilevel DC to AC Conversion and Classical Topologies

The multilevel approach for dc to ac conversion offers many advantages such as [5]–[10]:

1) The staircase waveform not only exhibits a better harmonic profile but also reduces the *dv/dt* stresses. Thus, the filter requirements can be greatly brought down (or even eliminated), while electromagnetic compatibility problems can be reduced.

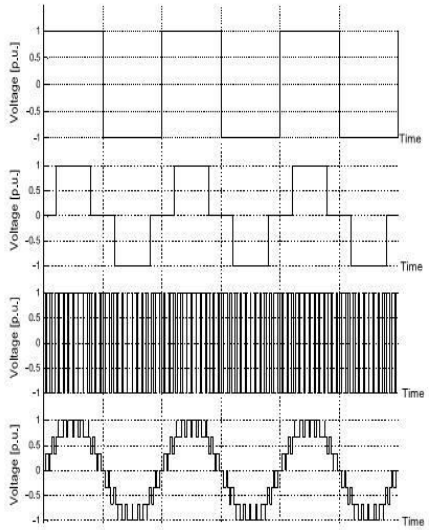

Fig.1. Typical inverter waveforms: (a) Square wave. (b) Quasi-square wave.
(c) Two-level PWM waveform. (d) Multilevel PWM waveform.

2) The voltage stresses on the semiconductor devices are much lesser as compared to the overall operating voltage. Thus, a high-voltage waveform can be obtained with comparatively low-voltage rated switches.

3) MLIs produce much smaller common mode voltage and thus, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.

4) Many multilevel topologies offer the possibility to obtain a given voltage level with multiple switching combinations. These redundant states can be utilized to program a fault tolerant operation.

5) MLIs can draw input current with low distortion.

6) Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system and can be controlled for equal load sharing amongst the input sources.

Over the past few decades, MLIs have attracted wide interest both in the research community and in the industry, as they are becoming a viable technology for many applications. In the mid 1970s, the first patent describing a converter topology capable of producing multilevel voltage from various dc voltage sources was published by Baker and Bannister [11]. The topology consists of single-phase inverters connected in series as depicted in Fig.2, and it is known as series-connected H-bridge inverter, or cascaded H-bridge (CHB) inverter.

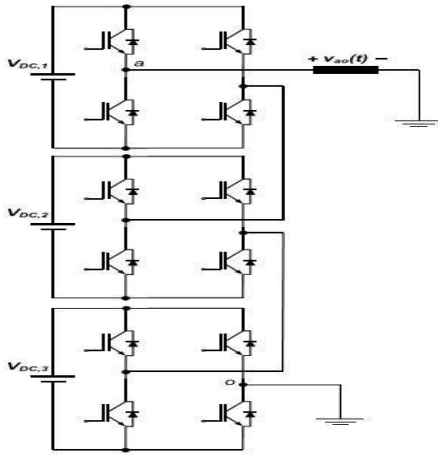

Fig.2. CHB structure for MLIs.

In another patent by Baker [12] in 1980, a modified multilevel topology was introduced, for which three-level and five-level versions are illustrated in Fig.3 (a) and (b), respectively. In contrast to the CHB inverters, this converter can produce multilevel voltage from a single dc source with extra diodes connected to the neutral point. This topology is now widely referred to as the neutral point clamped (NPC) inverter and/or diode clamped topology. In 1980, Nabae et al. [13] demonstrated the implementation of NPC inverter using a PWM scheme. In the 1980s, much of the research was focused only on three-level inverters. The so-called flying capacitor (FC) was introduced in the 1990s by Meynard and Foch [14] and Lavieville et al. [15]. The topology of the FC inverter is depicted in Fig.4 (a) for three-level and in Fig.4 (b) for five-level

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applications. Much of the literature published in past few decades have shown intense focus in studying the diode clamped, FCs and CHB topologies with regards to their respective pros and cons [5], [16]–[34], and these topologies are now widely referred to as the "classical topologies."

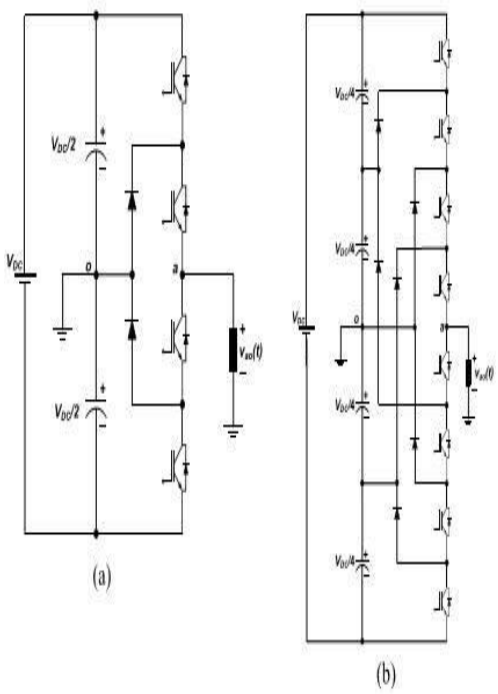

Fig.3. One leg of neutral-point /diode-clamped structure; (a) three-level; and (b) five-level.

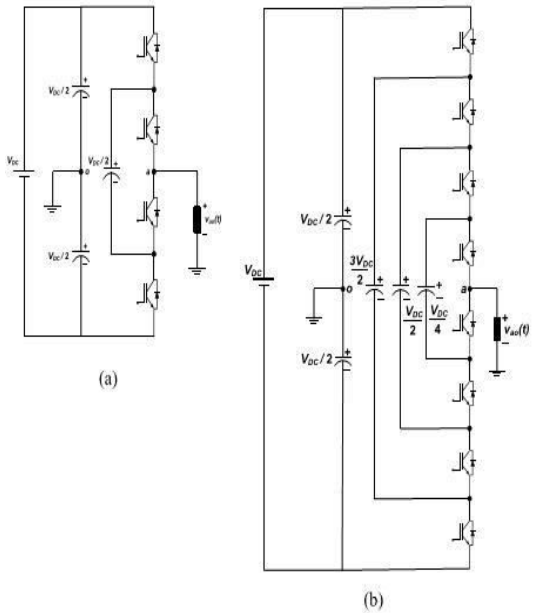

Fig.4. One leg of flying capacitor structure; (a) three-level; and (b) five-level.

(ii) Advent of New Topologies With Application-Oriented Approach

The so-called "classical topologies" have attracted maximum attention both from the academia and industry. Still, no specific topology seems to be absolutely advantageous as multilevel solutions are heavily influenced by application and cost considerations. Because of its intrinsic characteristics, a given topology can be very well adapted in some cases and totally unsuitable in some others. Therefore, the optimal solution is often recommended on case-to-case basis. Hence, along with the exploration of classical topologies, researchers continued (and still continue) to evolve newer topologies with an application oriented approach. In this subsection, some of such contributions are discussed.

(iii) Topologies with Reduced Device Count and Scope of This Paper

In view of their many advantages, MLIs are receiving much more and wider attention both in terms of topologies and control schemes. MLIs, however, exhibit an important limitation—for an increased number of output levels, they require a large number of power semiconductor switches, thereby increasing the cost, volume, and control complexity. Although low-voltage rated switches can be utilized in an MLI, each switch requires a related gate driver unit, protection circuit, and heat sink. This may cause the overall system to be more expensive, bulky, and complex. Consequently, for past few years, efforts are being directed to reduce the power switch count in MLIs and a large number of topologies have appeared in the literature [50]–[68]. These topologies have their own merits and demerits from the point of view of application requirements. As of now, no literature is available which comprehensively reviews the aforementioned topologies, thereby stipulating their comparative advantages and limitations. This paper aims at presenting a review of MLI topologies proposed with the exclusive objective of reducing the power switch count. Analysis of these topologies has been specifically carried out in terms of: count of power semiconductor components, total voltage blocking capability requirement, possibility of even power distribution amongst the input dc sources, possibility of optimal distribution of switching frequency amongst the power switches, and possibility of employing asymmetric sources. In addition, this paper provides a list of appropriate references in relation to MLI topologies and their control. Although the development of topologies has been accompanied with advancement in modulation

schemes [5]–[7], this paper focuses only on the topological features and their consequences.

(II) Terminology, Assessment Parameters, and Classification of Topologies

Prior to a comparative analysis of topologies, some terms pertaining to the assessment criteria are defined. Thereafter, various criteria to assess reduced device count topologies are discussed, and a classification of the topologies is presented so that a broad outline can be drawn.

(A) Terminology

1) Reduced Device Count Multilevel Inverter (RDC-MLI) Topologies: Topologies which are proposed/presented with an exclusive claim of reducing the number of controlled switching power semiconductor devices for a given number of phase voltage levels are referred to as RDC-MLI topologies. In this paper, nine such topologies [50]–[68] are reviewed.

2) Total Voltage Blocking Capability: For a topology, the total sum of the voltage blocking capability requirement for all its power switches is referred to as the "total voltage blocking capability" [65]. For example, if a structure consists of four switches rated at V_{DC} and six switches rated at $2V_{DC}$, the total voltage blocking capability requirement would be:

$$[(4 \times V_{DC}) + (6 \times 2V_{DC}) = 16V_{DC}]$$

3) Symmetric and Asymmetric Source Configuration: When the voltages of the input dc levels to an MLI are all equal, the source configuration is known as "symmetric," otherwise "asymmetric" [59]. Two popular asymmetric source configurations are: binary and trinary. In binary configuration, values of voltage levels are in geometric progression (GP) with a factor of "2" (i.e. V_{DC}, $2V_{DC}$, $4V_{DC}$, $8V_{DC}$...), while in trinary configuration the GP factor is "3" (i.e., V_{DC}, $3V_{DC}$, $9V_{DC}$, $27V_{DC}$...). There are many other asymmetric source configurations proposed by various researchers [44]. An asymmetric source configuration is employed to synthesize more number of output levels with the same count of power switches.

4) Even Power Distribution: When the multilevel dc to ac conversion is carried out in such a way that each input source contributes equal power to the load, the "power distribution" amongst the sources is said to be "even." Some authors also refer to it as "charge balance control" or "equal load sharing" [49]. "Even power distribution" is a feature of control aspect, only when the topology permits so. When the source configuration is symmetric, the control algorithm is designed such that the average current drawn from each source is equal, thereby making average powers equal. For a given topology, even power distribution is possible if each input source contributes toward all the output levels in one or more output cycles. For example, if a topology has three symmetric input dc sources $V_{DC,1}$, $V_{DC,2}$, and $V_{DC,3}$ ($V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC}$), then even power distribution is possible if all the combinations.

5) Level-Generation and Polarity-Generation: An MLI synthesizes a stepped waveform consisting of the input dc levels and their additive and/or subtractive combinations. Thus, the voltage waveform consists of multiple "levels" with both "positive" and "negative" polarities (in positive and negative half cycles, respectively). Many a times, an MLI circuit is such that a part of it synthesizes the multiple levels with only one polarity and an H-bridge is used to convert this single polarity waveform to a bipolar one for the ac load. These parts are, respectively, referred to as "level-generation part" and "polarity-generation part" [66].

It is important to mention here that the power switches for the polarity generation part need to have a minimum voltage rating equal to the operating voltage of the MLI.

6) Fundamental Frequency Switching: The switching losses in a converter are proportional to the current, blocking voltage, and switching frequency [68]. To minimize the switching losses, it is preferred to operate higher voltage-rated power switches at a low frequency and if possible, at the power frequency (or fundamental frequency), without compromising the quality of output waveform. A power switch in a topology can operate at fundamental switching frequency if it remains ON for one complete half cycle (either positive or negative) and remains OFF for the next complete half cycle, while the desired multilevel waveform is synthesized at the load terminals. Thus, fundamental frequency switching frequency is a control feature of modulation scheme provided the topology permits so. In addition, when a topology consists of power switches with different voltage ratings, in order to properly distribute the switching losses, the higher voltage rated switches should be operated at comparatively lower switching frequencies while those with lower voltage rating should be operated with comparatively higher switching frequencies. Thus, the switching frequency should be calculatedly "distributed" if the topology offers such a possibility. Also, if the level generation part of a topology can synthesize the zero level, then switches of polarity generation can be operated at the line frequency.

(B) Assessment Parameters

Merit of any given topology can be primarily judged based on the application for which it

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has to be employed. Still, in the context of this paper, the general criteria for an overall assessment of the merit of an RDC-MLI and its comparison with the other topologies can be:

1) The number of power switches used;
2) The total blocking voltage of the converter;
3) The optimal controllability of the topology, in terms of the possibilities of charge-balance control (or "even power distribution" amongst the input sources) and appropriate distribution of switching frequencies amongst the differently voltage-rated switches;
4) Possibility of employing asymmetric sources/capacitor voltage ratios in the topology.

While parameters 1 and 2 affect reliability of the inverter, efficiency is influenced by parameters 1, 2, and 3 and application, performance, and control complexity are governed by parameter 3. Number of redundant states and consequently, programmability of fault tolerant operation, is directly influenced by 1 and 4. In addition, apart from 1 and 2, the cost of a converter also depends on the dispersion of power switching ratings (e.g., using one 400 V switch and one 800 V switch would be, in principle, more expensive than using two 600 V switches).

(C) Categorization of RDC-MLI Topologies

In this paper, nine different RDC-MLI topologies, as proposed in [50]–[68], are evaluated. These topologies are enlisted as follows.

1) cascaded half-bridge-based multilevel dc-Link (MLDCL) inverter [50], [51];
2) T-type Inverter [52]–[54];
3) switched series/parallel sources (SSPS)-based MLI [55], [56];
4) series-connected switched sources (SCSS)-based MLI [57], [58];
5) Cascaded "bipolar switched cells" (CBSC)-based MLI [59];
6) packed-U cell (PUC) topology [60]–[64];
7) Multilevel module (MLM)-based MLI [65];
8) Reversing voltage (RV) topology [66], [67];
9) two-switch enabled level-generation (2SELG)-based MLI [68].

While a detailed analysis of these topologies is presented, it is important to appreciate that there are several similarities between the different RDC-MLI topologies which can be clearly seen if they are drawn with a similar structure, without taking into account the actual power switch configurations. For example, as shown in Fig.5 (a) and (b), it can be observed that the PUC topology is equivalent to the FC structure without dc sources. As indicated in Fig.5 (c) and (d), the T-type inverter [52]–[54] and CBSC-based MLI [59] have similar units. The 2SELG-based MLI [68] consists of repeated connection of the units used in MLM-based MLI [65] as shown in Fig.5 (e) and (f). Similarly, the topologies proposed in [50], [55], [57], and [66] consist of similar arrays of sources and switches connected in various fashions, as depicted in Fig.5 (g), (h), (i), and (j). With the help of Fig.5, it can be observed that the RDC-MLI topologies can be classified as those with H-bridge and those without H-bridge. In addition, these topologies may need isolated input dc levels or non isolated input dc levels. Thus, a broad categorization of RDC-MLI topologies is presented in Fig.6.

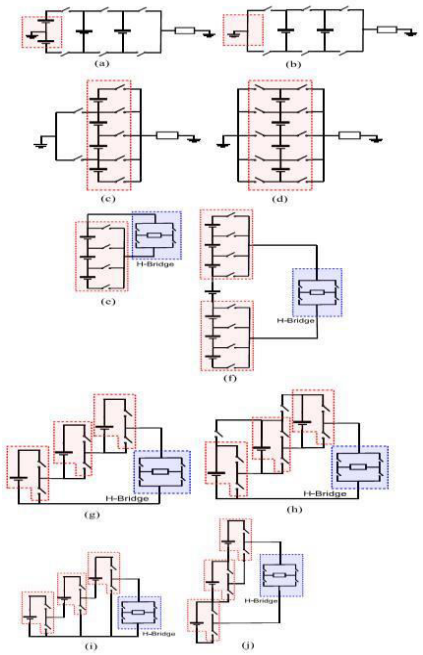

Fig..5. Similarities in the structures of various topologies.

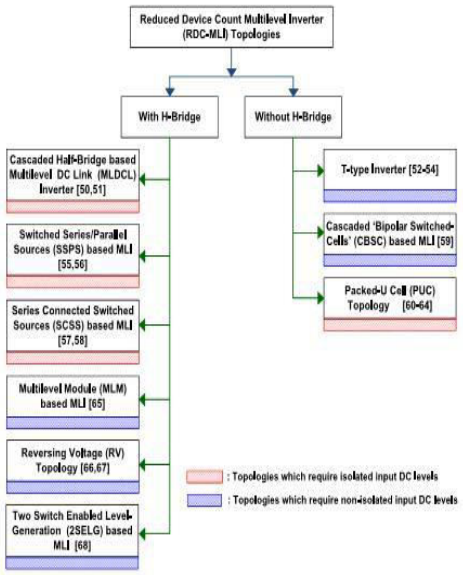

Fig.6 Categorization of RDC-MLI topologies.

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(III) review of MLI Topologies with Reduced Device Count

In this section, nine RDC-MLIs are reviewed and based on the parameters mentioned; topologies with reduced device count are discussed in this section. The topologies are presented in their single-phase form for the sake of simplicity. Their overall comparison, however, is carried out in terms of three-phase implementation, because MLIs are mostly administered in three-phase configurations. In addition, the illustrations for these topologies are indicated with four input sources and various valid switching states are tabulated. For the TCSMLDCL inverter, however, seven sources are shown so that its general structure can be comprehended.

(A) Cascaded Half-Bridge-Based MLDCL Inverter

Su [50], [51] has presented a new MLI named as "Cascaded Half-Bridge-based MLDCL inverter." An MLDCL inverter with four input dc levels is shown in Fig.7. It comprises of cascaded half-bridge cells, with each cell having its own dc source. It has separate "level-generation" and "polarity generation" parts. The level-generation part comprises of the sources $V_{DC,j}\{j=1,2,3,4\}$and the power switches $S_j\{j= 1to8\}$. This part synthesizes a multilevel dc voltage, $v_{bus}(t)$, fed to the "polarity-generation" part, comprising of switches $Q_j\{j=1to4\}$, which in turn alternates the polarity to produce a multilevel ac waveform.

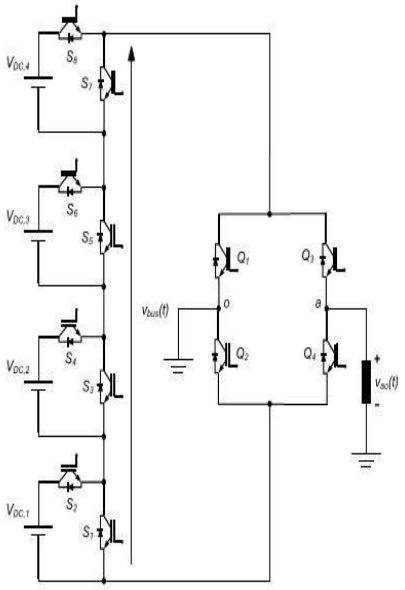

Fig.7 Cascaded half-bridge-based MLDCL inverter as proposed.

The level-generation part and two switches conduct for the polarity-generation part (switches Q_1 and Q_4 for the positive half cycle, Q_2 and Q_3 for the negative half cycle, and Q_1, Q_3/Q_2, Q_4 for the zero level). It can be observed from the topology that each power switch of polarity-generation part must possess a minimum voltage blocking capability equal to the sum of the input voltage values. Thus, these switches are rated higher as compared to the switches in the level-generation part. However, since the zero level can be synthesized using switches of the polarity-generation part, the higher rated switches $Q_j\{j=1to4\}$can be operated at fundamental switching frequency.

For a symmetric source configuration with $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$, it can be observed that the switches $S_j\{j=1to8\}$need to block a voltage of V_{DC} and need to conduct a current equal to the load current while the switches $Q_j\{j=1to4\}$need to block a voltage equal to $4V_{DC}$ and conduct a current equal to the load current. Moreover, it can be observed from Table II that since voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$, and $4V_{DC}$ can be synthesized combining all the input sources in groups of one, two, and three, respectively, equal load sharing amongst them is possible. These redundancies also provide flexibility in voltage balancing, in case capacitors are used.

Regarding asymmetric source configurations in the MLDCL topology, no comments are offered in [50] and [51]. Since subtractive combinations of the input dc levels cannot be synthesized, the trinary source configuration cannot be employed for this topology. As it can be observed from Table II, a binary source configuration with $V_{DC,1} = V_{DC}$, $v_{DC,2} = 2V_{DC}$, $V_{DC,3} = 4V_{DC}$, and $V_{DC,4} = 8V_{DC}$ is possible since the voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$, $5V_{DC}$, $6V_{DC}$,...,$15V_{DC}$ can be synthesized by utilizing the states presented.

As suggested by the author in [50] and [51], one application area in the low-power range (<100 kW) for the MLDCL inverters is in the permanent-magnet (PM) motor drives employing a PM motor of very low inductance. The level-generation part can utilize the fast-switching low-cost low-voltage MOSFETs and the polarity-generation part can use IGBTs so as to dramatically reduce the current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. The MLDCL inverter can also be applied in distributed power generation involving fuel cells and photovoltaic cells.

(B) T-Type Inverter

Cegliaet al. [52]–[54] reported a new MLI topology, herewith referred to as the "T-type inverter." The primary introduction to the topology is described in [52] with the help of a five-level single-phase inverter which results in a significant reduction in the number of power devices as compared to the conventional topologies. A single-phase structure of the topology with four input voltage sources is shown

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in Fig.8. It comprises of three switches $S_j\{j=1,2,3\}$which are bidirectional blocking-bidirectional-conducting while four switches $Q_j\{j=1to4\}$are unidirectional-blocking-bidirectional-conducting.

Thus, this topology inadvertently requires a mix of unidirectional and bidirectional power switches. Valid switching states for the inverter are summarized, and it can be seen that the input dc values are required to be symmetric, i.e. $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$. This is so because not all the additive/subtractive combinations of the input voltage levels can be synthesized at the load terminals and many times either a positive or negative combination can be synthesized but not both. For example, while a voltage level $-V_{DC,4}$ can be synthesized at the load terminals, the level $+V_{DC,4}$ cannot be synthesized. Thus, it is imperative that the input sources are symmetric. Also, lack of sufficient redundancies goes against an effective voltage balancing.

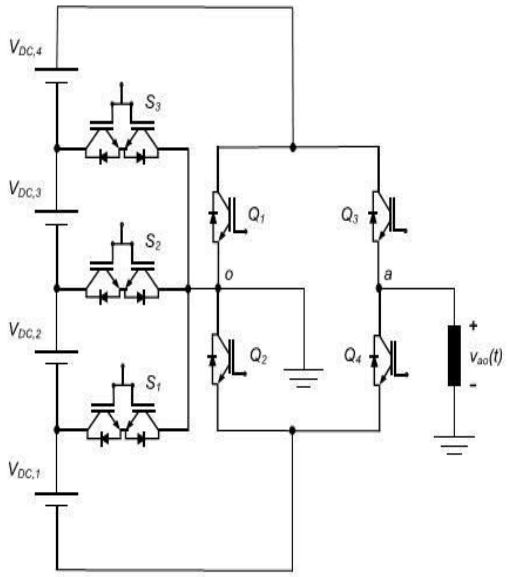

Fig.8. T-type inverter as proposed

(C) SSPS-Based MLI

Hinago and Koizumi [55], [56] proposed a single-phase MLI consisting of an H-bridge and DC sources which can be switched in series and in parallel. The topology is herewith referred to as "SSPS-based MLI." The topology requires the same of number of voltage sources as required by a CHB topology but it synthesizes same number of output levels with lesser number of power switches. An important application suggested is for electric vehicular applications where a single battery composed of a number of series-connected battery cells is available, which can be rearranged using the switched sources topology, hence reducing the requirement of switching devices. More importantly, possibility of combining two or more sources in series and parallel gives enough flexibility for meeting voltage/power requirements in the vehicle drive system.

The aforesaid topology with four input dc sources is shown in Fig.9, consisting of two parts: level-generation part which consists of the switched sources and synthesizes a bus voltage $v_{bus}(t)$ and the polarity-generation part which synthesizes positive and negative cycles of voltage v_{bus} (t) to feed an ac load. Four sources $V_{DC,j}$ {j=1to4} and power switches $S_j\{j=1to9\}$constitute the level-generation part while power switches $Q_j\{j=1to4\}$constitute the polarity generation part. The voltage levels which can be synthesized by the switched sources part are summarized.

For a symmetric source configuration, i.e., $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$, it can be observed that the voltage levels V_{DC} and $2V_{DC}$ can be synthesized with three states each while one state is available for voltage level $3V_{DC}$. Moreover, the voltage stress experienced by the switches $S_j\{j=1to9\}$ in this case would be equal to VDC each. An important limitation of this topology is that the switches $Q_j\{j=1to4\}$need to have a minimum blocking capability equal to summation of voltages of all voltage sources. Thus, for the symmetric source configuration with four sources, the switches of polarity-generation part should possess voltage blocking capability of $4V_{DC}$. Another important limitation is that these switches with higher blocking capability cannot be operated at fundamental switching frequency because the zero voltage level is not synthesized by the switched sources part, as can be observed. It can also be inferred from the table that, with input sources of equal voltages, equal load sharing amongst them is possible as the sources can be combined in all additive configurations.

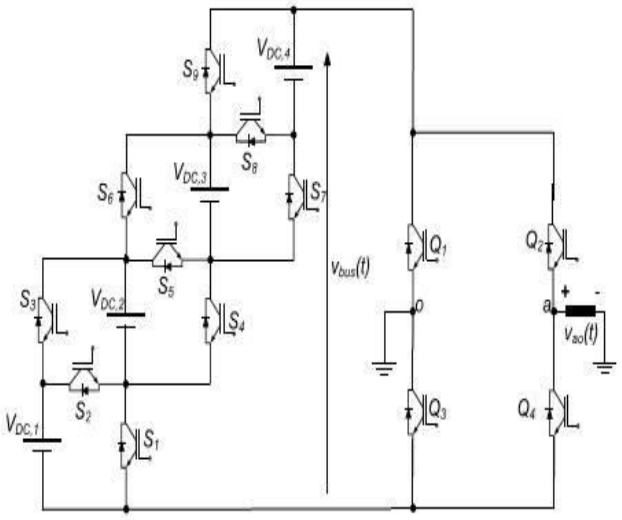

Fig.9. SSPS-based MLI as proposed

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(D) SCSS-Based MLI

A topology with sources connected in series through power switches is described in the literature [57], [58]. The topology with four input dc sources $V_{DC,j}$ {j=1to4}is shown in Fig.10. The low potential terminals of the sources are all connected through power switches while being also connected to the higher potential terminal of the preceding source through power switches, as illustrated in Fig.10 with S_j{j=1to8}.This interconnection is capable of synthesizing a multilevel rectified wave form $v_{bus}(t)$(the level-generation part), which is imparted positive and negative polarities using the H-bridge comprising of switches Q_j{j=1to4}(the polarity-generation part).

It can be seen that the structure, though simple, allows very restricted possibilities of synthesis of various levels at the bus end. In fact, not even the individual levels offered by the sources can all be obtained as $v_{bus}(t)$, except that of VDC,1. Thus, this topology does not offer any possibility of employing asymmetric source configurations for further reducing the switch count. The source configuration mandatorily needs to be symmetric, i.e., $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$. With such configuration, various switches would be differently voltage rated, that is to say, switches Q_j{j=1to4} should be minimally rated at $4V_{DC}$, S_1 should be rated minimally at $4V_{DC}$, while S_3, S_5, and S_7 should be minimally rated at $3V_{DC}$, $2V_{DC}$, and V_{DC}, respectively. Moreover, as it can be observed V, for symmetric input sources, equal load sharing is not possible as there are many combinations of input dc levels which are not feasible. Also, since the zero level can be obtained as $v_{bus}(t)$, the higher rated switches Q_j{j=1to4}can be operated at the fundamental switching frequency.

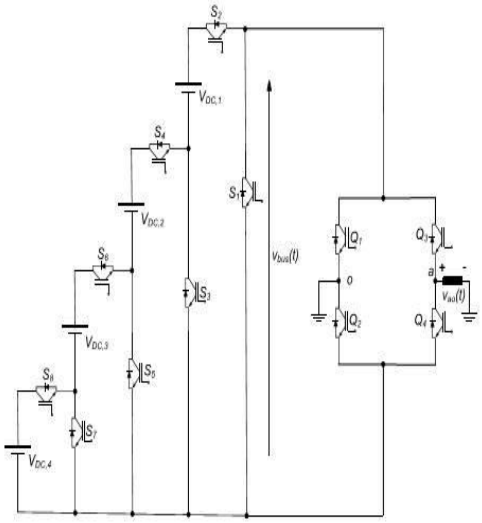

Fig.10. SCSS- based MLI as proposed

(E) CBSC-Based MLI

Babaeiet al.in [59] introduced a new class of MLI topology, here referred to as "CBSC-based MLI." Fig.11 shows the single phase structure of the topology with four input voltage sources. The topology requires all the switches to be bidirectional blocking-bidirectional-conducting in order to synthesize the required voltage levels at the output. The structure is such that each "cell" consisting of a source and power switches can synthesize voltage levels with both its polarities at the load terminals. Although each bidirectional switch requires two IGBTs, the total number of gate drive circuits is equal to the number of bidirectional switches. This results in reducing the cost and overall complexity of the converter.

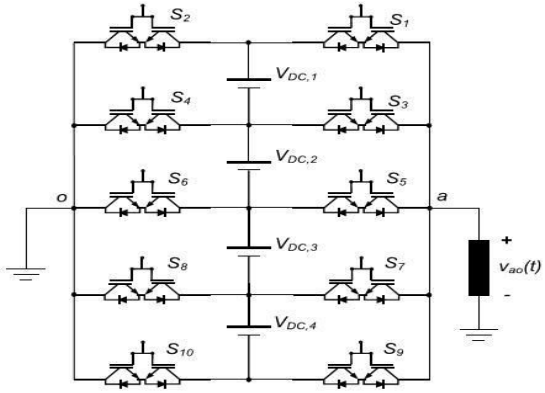

Fig.11. CBSC-based MLI as proposed

It should also be noted that the topology can only work with a symmetric source configuration. Asymmetric source configurations (binary or trinary) are not possible, since many subtractive and additive combinations of the input dc levels cannot be synthesized. Considering a symmetric source configuration with all input sources equal to V_{DC}, it can be observed that while synthesizing $2V_{DC}$ and $-2V_{DC}$, not all possible combinations of input voltage sources are utilized. Similar is the case for synthesis of voltage levels $3V_{DC}$ and$-3V_{DC}$. As a result, equal utilization of the input voltage sources is not possible in this topology. Moreover, outermost bidirectional switches S_1, S_2, S_9, and S_{10} need to have minimum voltage blocking capability of $4V_{DC}$ each. On the other hand, the inner switches S_3, S_4, S_7, and S_8 need to have minimum voltage blocking capability of $3V_{DC}$. Similarly, switches S_5 and S_6 need to bear a voltage stress of $2V_{DC}$.One can also observe that for synthesizing each voltage level, only two switches need to conduct simultaneously. This may result in equal conduction and switching losses. In addition, the topology requires non isolated dc sources.

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(F) PUC Topology

In [60]–[64], Ounejjar et al. proposed a new power multilevel converter topology that is very competitive compared to the classical topologies. The topology is named as the "PUC" topology. It consists of the so-called "packed U-cells." Each Ucell consists of an arrangement of two power switches and one dc input level (obtained with a voltage source or a floating capacitor). Authors claim that the topology offers high energy conversion quality using a small number of active and passive devices and consequently, has very low production cost. A single-phase structure of the packed U-cell topology with four input dc levels, $V_{DC,j}\{j=1to4\}$, and ten switches $S_j\{j= 1 to 10\}$, is shown in Fig.12.

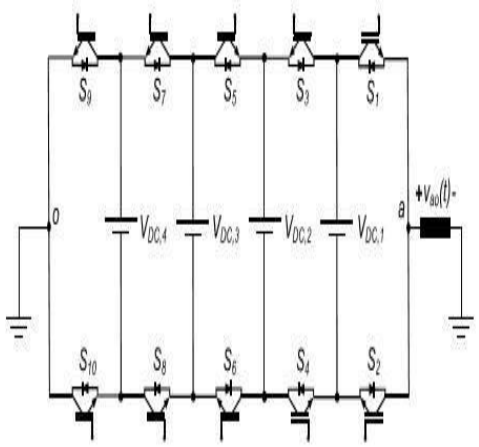

Fig.12. PUC MLI topology as proposed

The PUC topology is very simple in terms of interconnection of components. The minimal voltage blocking capability required for the switches are: $V_{DC,1}$ for S_1 and S_2, ($V_{DC,\ 1}-V_{DC,2}$) for S_3 and S_4, ($V_{DC,2}-V_{DC,3}$) for S_5 and S_6, ($V_{DC,3}-V_{DC,4}$) for S_7 and S_8,and $V_{DC,4}$ for S_9 and S_{10}. All the switches, when conducting, should be able to carry the load current. Thus, with four input levels, only five switches conduct simultaneously to obtain a desired voltage level.

In fact, in [64], the authors have proposed an elaborate methodology to calculate the asymmetric voltage levels. For a structure with two input sources, switching of middle two switches can be performed at fundamental frequency as demonstrated in [64]. This feature, however, is not feasible for the PUC topology with more than two number of input dc levels. In [64], the authors have described the PUC topology with two input sources. One source is taken as a floating capacitor in which the voltage is maintained at one-third of the voltage level of the other source (obtained with the rectification of input ac). The control scheme, though, is fairly complex in nature.

(G) MLM-Based MLI

Babaei [65] presented another multilevel converter topology, known as "MLM"-based MLI. The topology consists of separate "level-generation" and "polarity-generation" parts. The level-generation part consists of input dc sources and bidirectional-blocking-bidirectional-conducting switches. The voltage stress on these switches is not distributed uniformly. The switches in the polarity-generation part are unidirectional blocking-bidirectional-conducting and have to withstand the maximum voltage generated by the level generation part. However, these switches can be operated at line frequency as the level generation part is able to generate the zero level. Thus, these switches are high-voltage low-frequency switches.

A single-phase MLM-MLI with four input sources is shown in Fig.13. All the valid operating states are listed. The proposed topology does not facilitate asymmetrical source configuration (binary or trinary) because it is not possible to synthesize all subtractive and additive combination of the input voltage levels. For $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$, it is evident that all the possible combinations of the input voltage levels are not utilized. Thus in this topology, equal load sharing amongst the input sources is not possible. Also, the switches in the polarity-generation part are subjected to the voltage stress of $4V_{DC}$ each. For the level-generation part, switches S_1 and S_5 need to have minimum voltage blocking capability of $4V_{DC}$ whereas switches S_2 and S_4 should be selected to bear the voltage stress of $3V_{DC}$. Switch S_3 needs to bear voltage stress of $2V_{DC}$. However, only one switch in the level-generation part and two switches in the polarity-generation part need to conduct simultaneously to synthesize the required voltage level at the output.

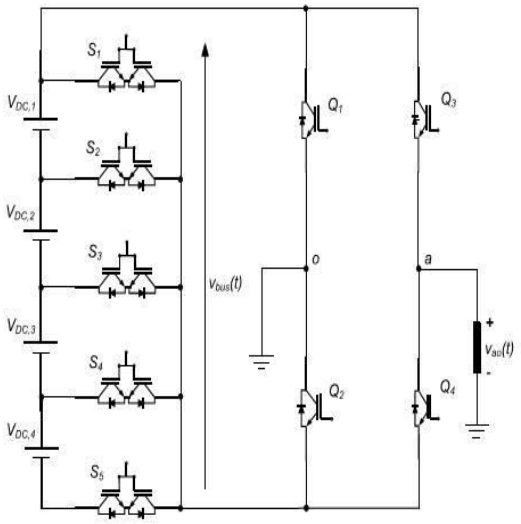

Fig.13. MLM-based MLI as proposed

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(H) RV Topology

In [66] and [67], Najafi et al. have proposed a so-called "reversing voltage" MLI (RV-MLI) topology which separates the output voltage into two parts: "level-generation" and "polarity-generation." A single-phase RV-MLI with four input dc sources, $V_{DC,j}$ {j=1to4}, is shown in Fig.14. The level-generation part comprises of the input dc sources and switches S_j{j=1to8}. The polarity-generation part consists of switches Q_j{j=1to8}, operating at the line frequency. In this way, the components are utilized effectively. The switches in the polarity-generation part need to withstand the total additive voltage of the level generation part. The topology exhibits modularity for the level generation part.

To overcome the issue of voltage balancing, authors in [66] and [67] have proposed use of separate dc sources. It is, however, true for several topologies that separate sources can solve the voltage unbalance problem. If separate sources are not used, balancing will have to be achieved by proper utilization of redundant states. Various valid states for possible combinations of input sources so as to obtain different levels at the level generation part, $v_{bus}(t)$, are summarized in Table IX. It can be noted that the switches with high blocking voltages, Q_j{j=1to4}, can be operated at fundamental switching frequency as the zero level voltage can be synthesized at the level generation part itself. If symmetric sources are used such that $V_{DC,1}$ =$V_{DC,2}$ =$V_{DC,3}$ =VDC,4 =V_{DC}, then all switches of the level generation part experience a voltage stress of V_{DC}, while the four switches of the polarity generation part are required to have minimum voltage blocking capability of 4V_{DC} each.

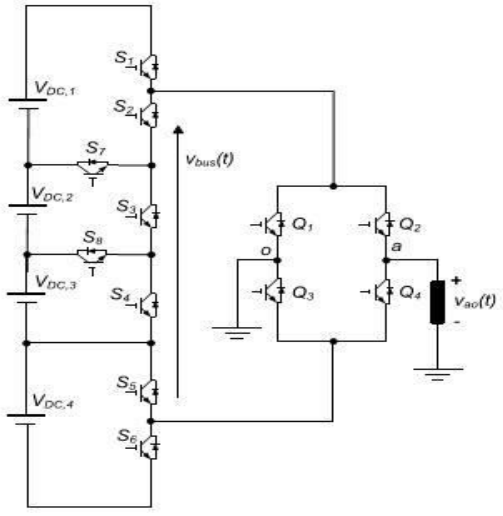

Fig.14. RV topology as proposed

For a dc link created with connected capacitors, this limitation will affect voltage balancing in the capacitors. Moreover, since the topology does not facilitate the synthesis of all additive and subtractive combinations of input voltage sources, trinary source combination cannot be implemented with this topology.

Employing other asymmetric combinations to maximize the number of output levels is seriously hampered by the absence of some states with a single voltage source. However, one important advantage of the topology is that it uses a single dc link for three-phase implementation, thereby offering savings in the number of input voltage sources.

(I) Two-Switch-Enabled Level Generation (2SELG)-Based MLI

The topology presented by Babaei in [68] has separate "level generation" and "polarity-generation" parts. The specialty of this topology is that the level-generation part requires only two conducting switches to synthesize any valid voltage level, irrespective of the number of input sources. Therefore, this topology is referred to as "2SELG-based MLI." A single-phase configuration of 2SELG-MLI with seven input levels, $V_{DC,j}$ {j=1to7}, is shown in Fig.15.

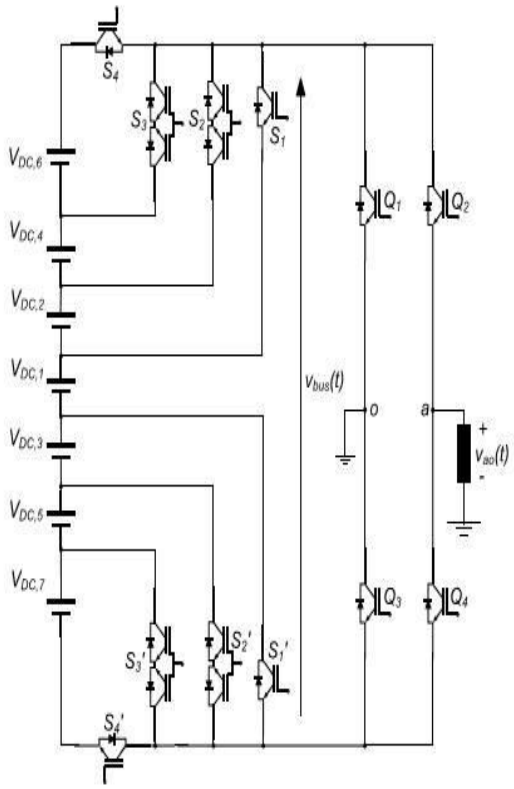

Fig.15. 2SELG-based MLI as proposed

The topology requires a mix of unidirectional and bidirectional switches. The switches of the polarity-generation part, therefore,

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cannot operate with a fundamental switching frequency.

For a symmetrical source configuration, $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC,5} = V_{DC,6} = V_{DC,7} = V_{DC}$, it is not possible to apply the concept of "even power distribution" in this topology, as all the sources do not contribute equally for each level in the $v_{bus}(t)$. Also, the switches in the polarity-generation part need to have minimum voltage blocking capability of $7V_{DC}$. Switches S_1, S_4, S_1, and S_4 needs to have minimum voltage blocking capability of $3V_{DC}$. Rest of the switches need to have minimum voltage blocking capability of $2V_{DC}$. It is also observed that this topology does not support asymmetrical source configuration (binary or trinary) as it is not possible to synthesize all subtractive and additive combinations of the input voltage levels. However, one advantage offered by 2SELG-MLI is that a total of four power electronic switches need to be conducting in all the switching states, thus resulting in lower conduction losses.

III. INDUCTION MOTOR

An asynchronous motor type of an induction motor is an AC electric motor in which the electric current in the rotor needed to produce torque is obtained by electromagnetic induction from the magnetic field of the stator winding. An induction motor can therefore be made without electrical connections to the rotor as are found in universal, DC and synchronous motors. An asynchronous motor's rotor can be either wound type or squirrel-cage type.

Three-phase squirrel-cage asynchronous motors are widely used in industrial drives because they are rugged, reliable and economical. Single-phase induction motors are used extensively for smaller loads, such as household appliances like fans. Although traditionally used in fixed-speed service, induction motors are increasingly being used with variable-frequency drives (VFDs) in variable-speed service. VFDs offer especially important energy savings opportunities for existing and prospective induction motors in variable-torque centrifugal fan, pump and compressor load applications. Squirrel cage induction motors are very widely used in both fixed-speed and variable-frequency drive (VFD) applications. Variable voltage and variable frequency drives are also used in variable-speed service.

In both induction and synchronous motors, the AC power supplied to the motor's stator creates a magnetic field that rotates in time with the AC oscillations. Whereas a synchronous motor's rotor turns at the same rate as the stator field, an induction motor's rotor rotates at a slower speed than the stator field. The induction motor stator's magnetic field is therefore changing or rotating relative to the rotor. This induces an opposing current in the induction motor's rotor, in effect the motor's secondary winding, when the latter is short-circuited or closed through external impedance. The rotating magnetic flux induces currents in the windings of the rotor; in a manner similar to currents induced in a transformer's secondary winding(s). The currents in the rotor windings in turn create magnetic fields in the rotor that react against the stator field. Due to Lenz's Law, the direction of the magnetic field created will be such as to oppose the change in current through the rotor windings. The cause of induced current in the rotor windings is the rotating stator magnetic field, so to oppose the change in rotor-winding currents the rotor will start to rotate in the direction of the rotating stator magnetic field. The rotor accelerates until the magnitude of induced rotor current and torque balances the applied load. Since rotation at synchronous speed would result in no induced rotor current, an induction motor always operates slower than synchronous speed. The difference, or "slip," between actual and synchronous speed varies from about 0.5 to 5.0% for standard Design B torque curve induction motors. The induction machine's essential character is that it is created solely by induction instead of being separately excited as in synchronous or DC machines or being self-magnetized as in permanent magnet motors.

For rotor currents to be induced the speed of the physical rotor must be lower than that of the stator's rotating magnetic field (n_s); otherwise the magnetic field would not be moving relative to the rotor conductors and no currents would be induced. As the speed of the rotor drops below synchronous speed, the rotation rate of the magnetic field in the rotor increases, inducing more current in the windings and creating more torque. The ratio between the rotation rate of the magnetic field induced in the rotor and the rotation rate of the stator's rotating field is called slip. Under load, the speed drops and the slip increases enough to create sufficient torque to turn the load. For this reason, induction motors are sometimes referred to as asynchronous motors. An induction motor can be used as an induction generator, or it can be unrolled to form a linear induction motor which can directly generate linear motion.

Synchronous Speed:

The rotational speed of the rotating magnetic field is called as synchronous speed.

$$Ns = \frac{120 \times f}{P} \quad (RPM) \tag{1}$$

Where, f = frequency of the supply
P = number of poles

Slip:

Rotor tries to catch up the synchronous speed of the stator field, and hence it rotates. But in

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practice, rotor never succeeds in catching up. If rotor catches up the stator speed, there won't be any relative speed between the stator flux and the rotor, hence no induced rotor current and no torque production to maintain the rotation. However, this won't stop the motor, the rotor will slow down due to lost of torque, and the torque will again be exerted due to relative speed. That is why the rotor rotates at speed which is always less the synchronous speed.

The difference between the synchronous speed (Ns) and actual speed (N) of the rotor is called as slip.

$$\% \text{ slip } \quad s = \frac{Ns - N}{Ns} \times 100 \qquad (2)$$

IV. MATLAB/SIMULINK RESULTS

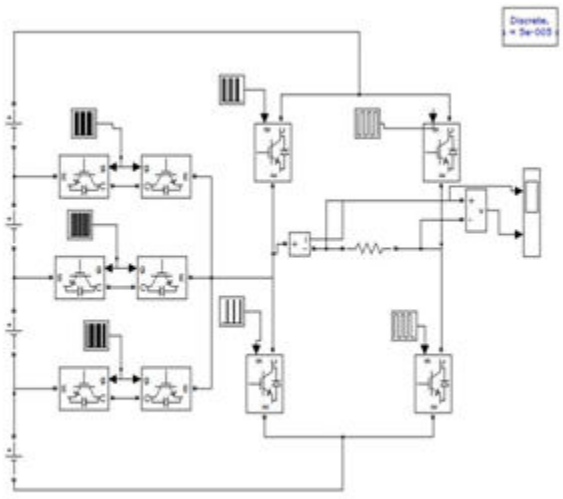

Fig.16 Simulink model diagram for 9 level multi level inverter

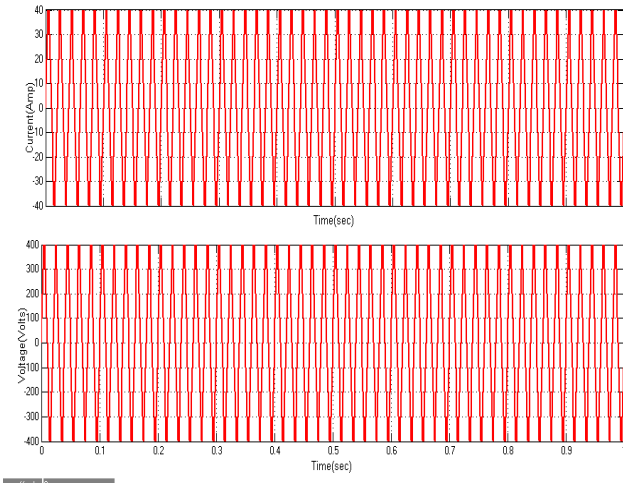

Fig.17 Simulated waveforms of AC output voltage and current of a 9 level multilevel inverter

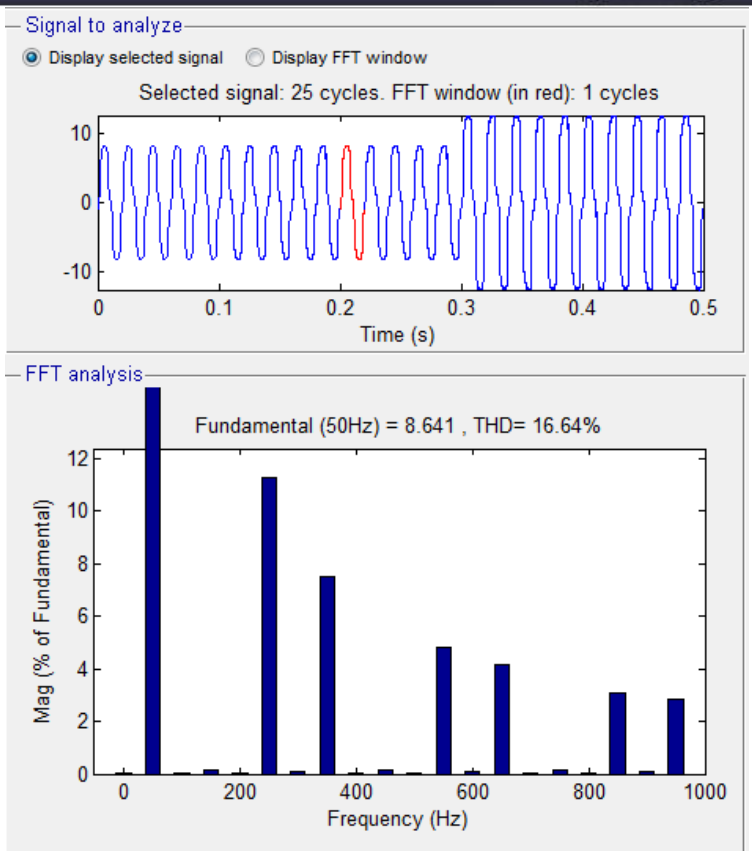

Fig.18 AC Inverter output THD

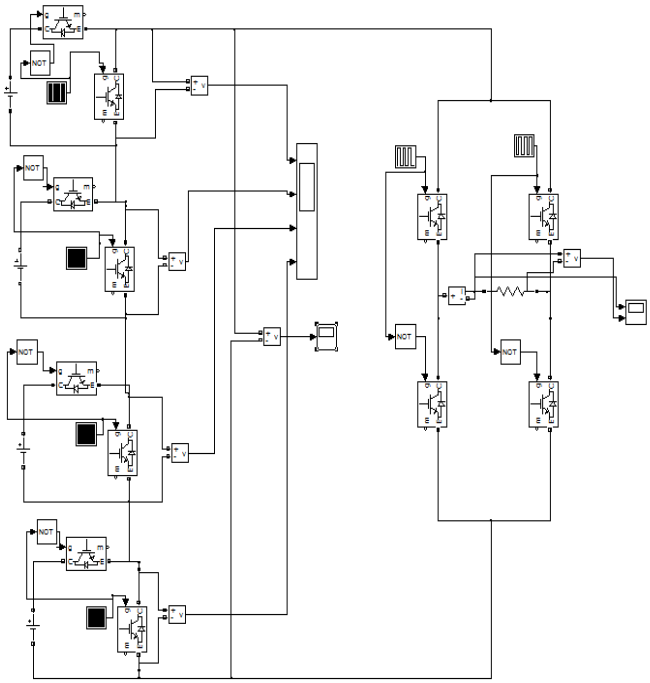

Fig.19 Simulink model diagram for 31 level multi level inverter

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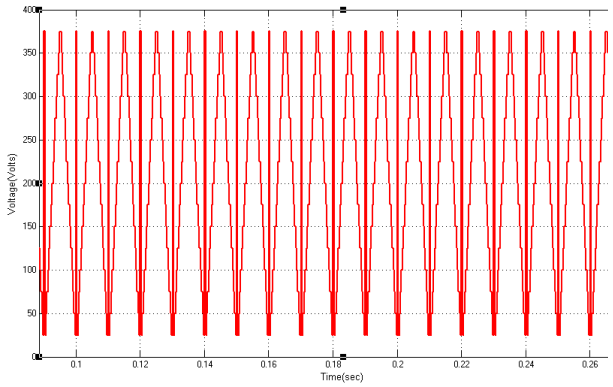

Fig.20 Simulated waveforms of DC bus voltage of a 31 level multilevel inverter

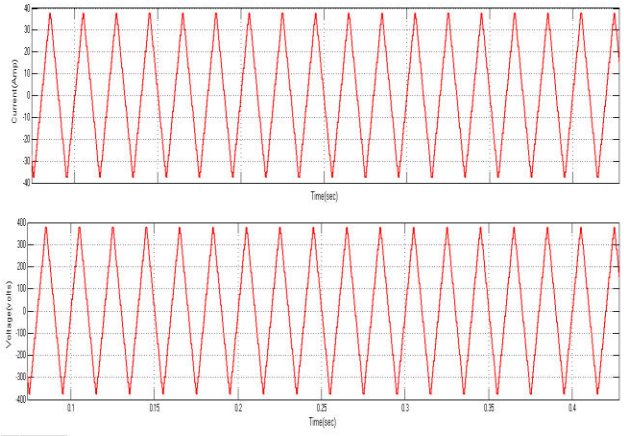

Fig.21 Simulated waveforms of AC output voltage and current of a 31 level multilevel inverter

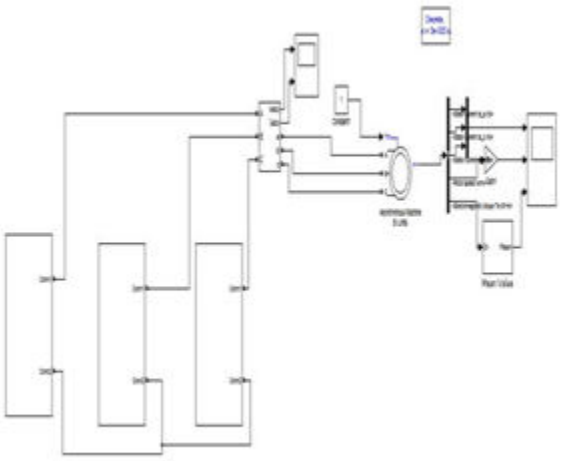

Fig.22 Simulink model connected with Induction motor drive

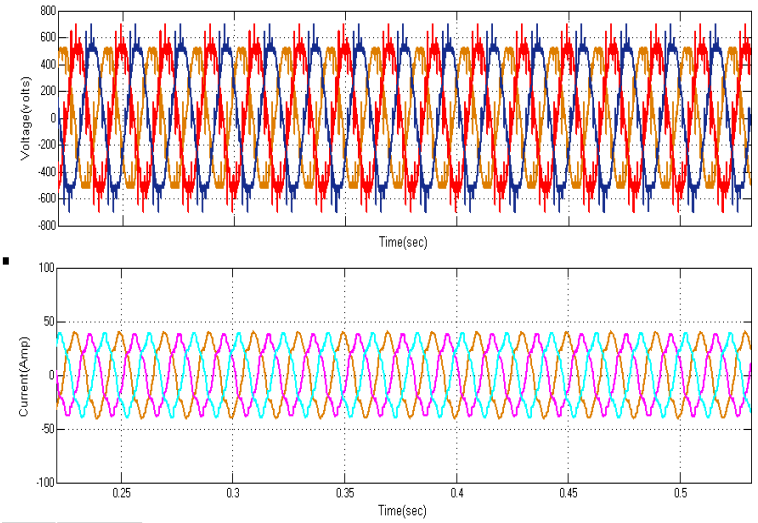

Fig.23 Three-phase supply voltage and current.

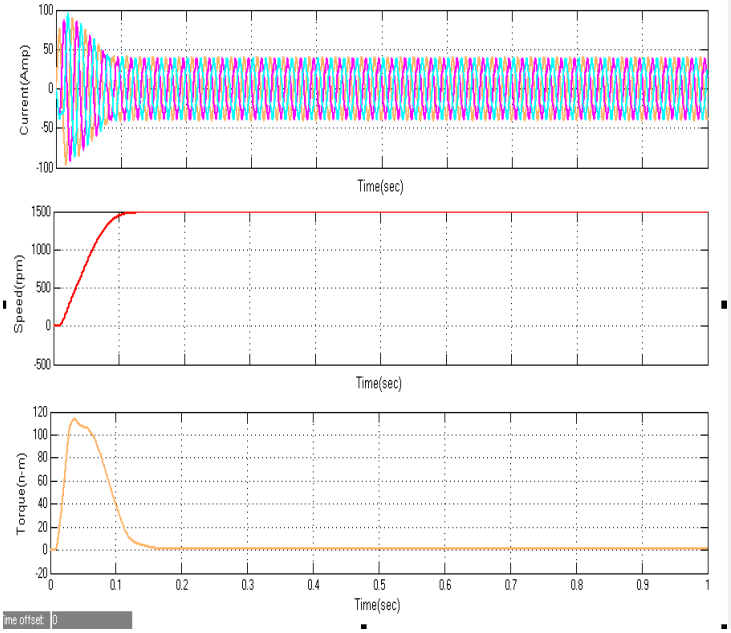

Fig. 24 Stator current, Speed of the induction motor & Torque characteristics of the induction motor.

V. CONCLUSION

A new topology of the three-phase multilevel inverter topology was introduced for induction motor drive applications. The suggested configuration was obtained from reduced number of power electronic components. Therefore, the proposed topology results in reduction of installation area and cost. The proposed circuit is applied to Induction Motor Drive to check the performance of entire system. Simulation results are shown.

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