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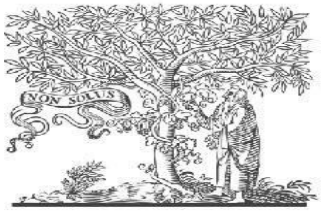

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Quantum Gates Based Carry Select Adder Using VHDL

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Abstract

Quantum computing is indeed a promising technology that utilizes the principles of quantum mechanics to perform computations that are beyond the capabilities of classical computers. In this context, the design of adders using low quantum cost full adder is a significant step towards building practical quantum circuits.

The proposed full adder design based on CNOT and CCNOT gates is a common approach used in many quantum circuits. The parallel adder and carry select adder designed using this full adder are also valuable contributions that demonstrate the potential of quantum computing. The use of CSWAP gates in the proposed carry select adder design is an interesting choice, as CSWAP gates are known to have a low quantum cost compared to other multi-qubit gates. The use of CSWAP gates as 2×1 multiplexers is a clever way to select the output from the two parallel adders that make up the carry select adder.

It is worth noting that the simulation of quantum circuits using tools such as Xilinx Vivado is an essential step in the design process. Simulations provide a means to verify the correctness of the circuit and observe its behavior under different conditions. Overall, the design of adders using low quantum cost full adder is a significant contribution to the field of quantum computing. It paves the way for the development of more complex quantum circuits that can solve real-world problems efficiently.

Keywords: Carry Select Adder, CSWAP Gate, CCNOT Gate, Quantum Circuits, Xilinx Vivado

Introduction

The demand for high-speed information processing and computation in various fields has led to the development of complementary metal oxide semiconductor (CMOS) technology. However, despite its usefulness, CMOS still faces limitations due to high-speed requirements. This has led to the development of quantum computing as an alternative to classical computing systems.

Quantum computing is advantageous due to its properties of interference, entanglement, superposition, and reversibility. These properties make it suitable for various applications, including communication and complex computational problems. Quantum researchers have been working on developing quantum logic gates, which are the building blocks of quantum circuits. These gates manipulate the state of qubits, which are the basic units of quantum information.

Arithmetic and logical operations are crucial for many practical applications of quantum computing, such as cryptography and optimization. Therefore, researchers have been exploring ways to implement these operations using quantum gates.

Qubit characterization is also an important area of research in quantum computing. Since qubits are susceptible to various sources of noise and errors, it is essential to characterize their properties accurately. This involves measuring various parameters such as coherence time, fidelity, and error rates, which can help researchers optimize the performance of quantum circuits.

Overall, the design of logic systems and improving decision-making abilities using quantum gates and qubit characterization are crucial steps towards building practical quantum computers that can outperform classical computers in specific tasks. In this article, the authors propose a full adder with low quantum cost and garbage output, which is then used to design a 4-bit parallel adder and carry select adder. The authors use a CSWAP gate as a multiplexer for the design of the carry select adder. The proposed quantum circuits are designed and simulated using the open-source Xilinx Vivado software with VHDL programming.

In section I, the discussion on available quantum operators to design logic gates and single bit adders is essential as it provides readers with the necessary background information on quantum gates and their properties. This section can help readers understand the basics of quantum computing and prepare them for the subsequent sections.

Section III, which explains the design of the parallel adder and carry select adder using the full adder, is a crucial part of the article. This section provides readers with a detailed description of the proposed quantum circuits and how they can be built using the full adder. This section can help readers understand how to design more complex quantum circuits using simpler building blocks.

Section IV, which analyzes the outcome of the simulated quantum circuits with respect to metrics, is also an important part of the article. This section provides readers with a quantitative assessment of the proposed quantum circuits' performance, which can help them evaluate the usefulness of the proposed approach.

Finally, section V, which concludes the proposed work, is an essential part of the article as it summarizes the key findings and contributions of the proposed work. This section can help readers understand the overall impact of the proposed work on the field of quantum computing. Overall, the proposed low quantum cost full adder and the resulting parallel adder and carry select adder designs show promise in improving the speed and efficiency of quantum computing systems. Further research and development in this field are needed to improve the design and implementation of quantum circuits for practical applications.

Quantum Gates Based 1-Bit Adders

Two-level qubit systems are the simplest form of quantum systems that are widely used in quantum computing. These systems operate over two states, commonly denoted as $|0\rangle$ and $|1\rangle$, which form the basis for quantum computation. These states are also referred to as the computational basis states.

$$|0\rangle = \begin{pmatrix} 1 \\ 0 \end{pmatrix}, \qquad |1\rangle = \begin{pmatrix} 0 \\ 1 \end{pmatrix} \tag{1}$$

These qubit states are analogous to the binary elements or bits of the classical systems, '0' and '1'. But these states $|0\rangle$ and $|1\rangle$ differ from classical system in another form of state, which is a linear combination or superposition of both.

The article states that only a few operators are described in the later part of the section, which are required for the proposed designs. It is not clear which specific operators are being referred to, as the article does not provide further details.

In quantum mechanics, the state of a qubit can be represented using a complex vector in a two-dimensional Hilbert space. The state vector of a qubit can be expressed as a linear combination of the basis states $|0\rangle$ and $|1\rangle$:

$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$,

where α and β are complex numbers, and $|\alpha|^2 + |\beta|^2 = 1$, which reflects the normalization condition for a quantum state. This superposition property of qubits is one of the fundamental differences between classical and quantum computing.

The ability to manipulate the state of qubits using quantum gates and perform operations on superposed states is what makes quantum computing powerful and capable of solving problems that are intractable for classical computers.

Therefore, understanding two-level qubit systems and their properties is essential for analyzing quantum circuits, defining quantum algorithms, and developing quantum computers.

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A. Unary Gates: I,X and H

According to the article, there are three unary gates commonly used in quantum computing: Identity (I), NOT (X), and Hadamard (H). These gates operate on a single qubit, and their matrix representations are shown in Figure 1 along with their symbols.

The Identity gate, represented by the symbol I, does not change the input qubit and provides the same qubit as an output. The NOT gate, represented by the symbol X, flips the input qubit, changing $|0\rangle$ to $|1\rangle$ and vice versa.

The Hadamard gate, represented by the symbol H, is an important gate in quantum computing and information systems. It transforms a qubit into a superposition of its computational basis states [4]. If an input qubit system is applied with n Hadamard gates, outputs will be produced for all possible input combinations.

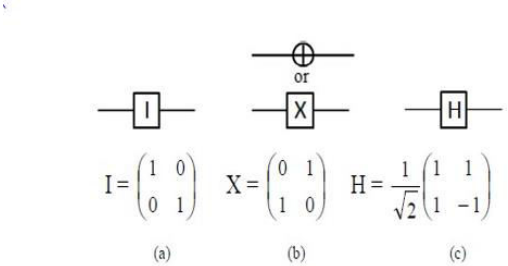

Fig. 1. Symbol and matrix form of a) Identity, b) NOT, and c) Hadamard gates

B. Binary and Ternary Gates:

It is common to represent quantum gates using symbols that depict their functionality. These symbols can help readers understand the operation of quantum gates without going into the details of their underlying quantum mechanics.

In the context of the article, Fig. 2 likely shows the symbols of quantum gates that are relevant to the proposed work. The first gate is likely a binary gate, which operates on two qubits and performs a binary operation, such as the CNOT(Feynman)gate. The remaining two gates are likely ternary gates, which operate on three qubits and perform a ternary operation, such as the CCNOT (Toffoli) gate.

The symbols of these gates can vary depending on the notation used by different authors or in different contexts. However, the logical operations performed by these gates are typically standardized and represented using truth tables or other forms of logical expressions. These logical operations can help readers understand how quantum gates manipulate the state of qubits and perform various arithmetic and logical operations that are relevant to quantum computing.

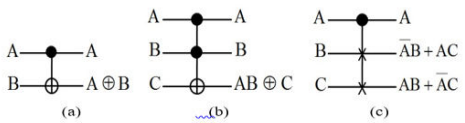

Fig. 2. Symbols of a) CNOT, b) CCNOT, and c) CSWAP gates with their output functions

The CSWAP gate is also named the Fredkin gate and is a controlled SWAP gate that can be used for swapping, AND, and OR operations.

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The design metrics used in the proposed work are Constant Inputs (CI), Garbage Outputs (GO), and Quantum Cost (QC).

Garbage outputs are gate outputs that are not considered as primary outputs and are not connected to any other gate.

Constant inputs are gate inputs that are excited with logic '0' or logic '1' to obtain the required output.

Literature Survey

The paper [1] proposed by Dr.Sk.Enaul Haq consists of the details about Quantum gates and Carry select adder developed using IBM Qiskit.

The paper [2] proposed by T.S Humble contains the details about quantum computing circuits and devices which helps us to develop carry select adder.

The paper [3] proposed by H.Thomas tells us about the programming of the quantum circuits which helps us to write the programms for the quantum circuits.

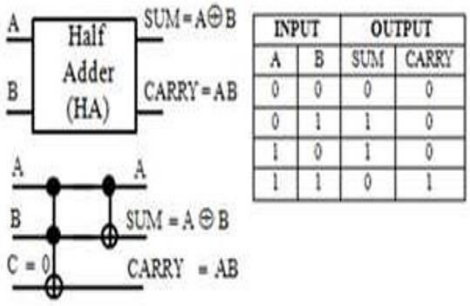
Problem Identification

The Early Model of the Carry Select Adder is developed in python by using IBM Qiskit which is taking more time than expected and requires large circuits hence we want to design the circuit in the low cost which works faster than the earlier version and which takes the less gates to build the circuit.

Methodology

The following are the Design methodology steps to develop Carry select adder:

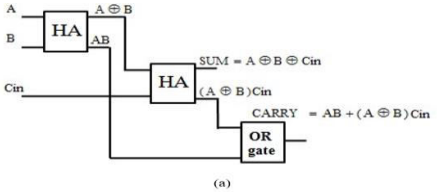
Step 1: Build the Halfadder circuit using the Quantum gates like cnot and ccnot.



INPUT		OUTPUT	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig.3. Half adder a) Logic symbol (top), Quantum Circuit (bottom) and b) Truth table

Step 2: After creating the Half Adder using Quantum gates then try to create the full adder circuit just by cascading the two half adders.



INPUT			OUTPUT	
A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

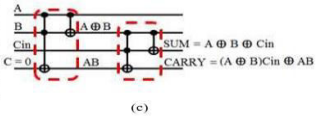


Fig. 4. Full adder a) Block diagram, b)Truth table and c) Quantum circuit with Half adders(red)

Step 3: After creating the full adder then we have to cascade the four full adders to generate the parallel adder.It will generate 4 bit parallel adder.

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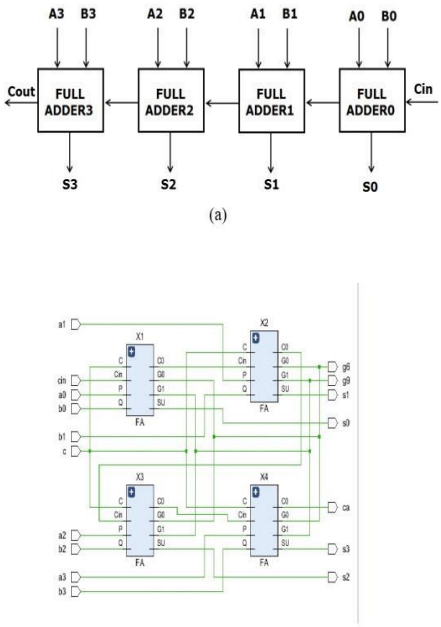


Fig. 5. Parallel Adder (a) Block diagram and (b) Quantum Circuit

Step 4: After creating the 4 bit parallel adder then the next step is to create the multiplexer which is used for selection lines.

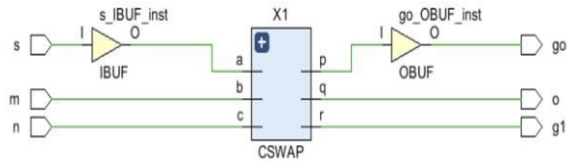
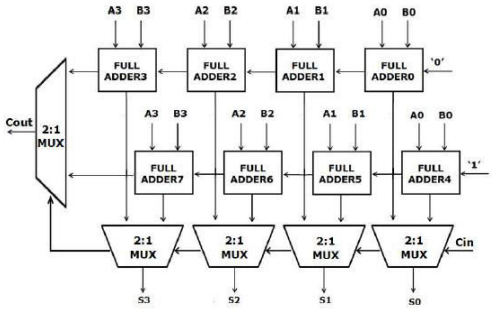


Fig.6.Multiplexer Schematic Diagram

Step 5: After creating multiplexer then cascade two 4 bit parallel adder and 5 multiplexers to get the carry select adder which will be our final circuit design.

To select the required output of the carry select adder multiplexers are used in the circuit.

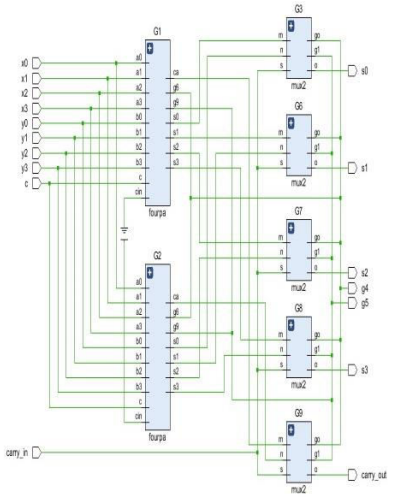
Hence the required carry select adder using full adder and multiplexer is designed and is shown in Figure.



Block diagram of carry select adder

Results:

The simulated Results and schematic quantum circuit of the generated carry select adder is given in the below diagrams.



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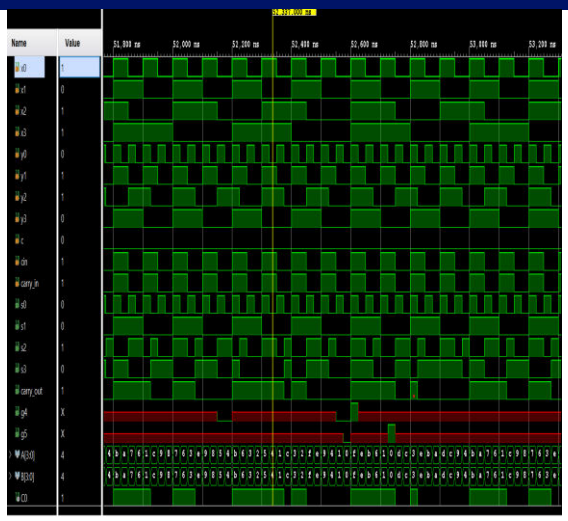

Carry select adder simulation

Conclusion

It's interesting to see how quantum computing is being explored as a potential solution to the limitations of classical computing. The use of quantum gates to design adder circuits is a promising area of research as it has the potential to significantly speed up arithmetic operations.

The low quantum cost of the proposed full adder circuits is also noteworthy as it indicates that they require fewer quantum resources to execute, making them more efficient.

It would be interesting to see further research in this area to explore the potential of quantum computing in solving other complex computational problems.

The use of Xilinx Vivado for simulation is also a common practice in digital circuit design and verification.

Quantum Gates based Carry Select Adder can also be implemented using FPGA Kit.

Future scope:

There is a scope to improve the effeciency and the speed of the circuits by decresing the delay in the gates.

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