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Title: **GRID CONNECTED SNUBBER LESS SOFT SWITCHING THREE-PHASE PUSH-PULL DC-DC CONVERTER FOR DC-MICRO GRID APPLICATION**

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## GRID CONNECTED SNUBBER LESS SOFT SWITCHING THREE-PHASE PUSH-PULL DC-DC CONVERTER FOR DC-MICRO GRID APPLICATION

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**ABSTRACT-** A bidirectional current-fed three-phase push-pull dc/dc converter is proposed for DC micro-grid application. The proposed converter is analyzed and designed to interface two dc buses of 48 V and 380 V in a micro grid. An innovative novel modulation technique is proposed to clamp the device voltage spike across primary side current-fed devices at turn-off solving traditional problem. The proposed modulation helps achieve natural zero current commutation of low voltage side (LVS) devices and zero voltage switching (ZVS) turn-on of high voltage side (HVS) devices. This eliminates the use of passive/active snubbersless in conventional current-fed topologies to mitigate the voltage-spike across the devices. The steady-state operation, analysis, and design of the converter with proposed modulation are explained. Soft-switching conditions are derived. It eliminates the use of passive/active clamp circuits to mitigate the turnoff voltage spike across the devices, a traditional problem associated with current-fed topologies. Additionally, the higher ripple frequency reduces the volume of the transformer and the input inductor, making it suitable for high-power applications. The micro grid on the other hand, although not a replacement of the national grid, aids the grid by decentralized generation incorporating environmental friendly distributed energy resources. Also, the bidirectional functionality makes the grid structure smart and interactive where traditional central control is shifted to decentralized control and energy storage plays a vital role in grid support. The proposed converter fed with an inverter and integrated with AC grid.

### I INTRODUCTION

Even though the centralized transmission grid system is the backbone of the distribution system, it encompasses the huge transmission loss of almost 8%–10% owing to the geographic separation of the generation and demand. The micro grid on

the other hand, although not a replacement of the national grid, aids the grid by decentralized generation incorporating environmental friendly distributed energy resources. Dual-active-bridge converters have attracted high attention mainly because

of its ability of bidirectional power flow between two dc buses or dc-ac buses along with galvanic isolation, compactness, and higher power density [1]–[3]. Also, the bidirectional functionality makes the grid structure smart and interactive where traditional central control is shifted to decentralized control and energy storage plays a vital role in grid support. For example, it has been implemented in hybrid electric vehicles for energy exchange between batteries/ultra capacitors and drive motors, in line interactive uninterruptible power supply for battery charging and discharging, in fuel cell energy system, and also in renewable energy system for energy storage. Among the basic topologies, the current-fed topology is preferred over the voltage-fed one [4]–[9] for the aforementioned application because the former shows better efficiency for high voltage amplification requiring lower turns ratio. The advantages of the current-fed topology over the latter are listed as follows:

- 1) Lower turn's ratio leading to lower leakage inductance and lower copper loss attributed by the transformer;
- 2) The inherent short-circuit protection during high-current application;
- 3) lower duty cycle loss;
- 4) Utilization of leakage inductance for power transfer and soft switching, thus giving the flexibility of higher leakage inductance; and
- 5) Reduced circulating current and, hence, lower rms and peak current through the switches. Usually, the current-fed topologies in the literature implement active/passive snubbers to clamp the voltage and avoid the

voltage spike across the switch during turnoff. However, the passive snubbers result in low efficiency and increased converter size, whereas active snubbers require floating active devices and large high frequency (HF) capacitors and are less reliable. Hence, a new modulation technique, secondary-side modulation [10], [11], is implemented which utilizes the secondary active switches to achieve soft switching in the primary switches during turnoff and also soft switching in the secondary active switches during turn-on.

Hence, the natural voltage clamping of devices is obtained employing the proposed modulation that solves a traditional problem associated with current-fed circuit topologies. Thus, the modulation method addresses the voltage-spike issue without increasing any component count and realizes the high reliability of the system. In current source converters, the three-phase topologies [12]–[15] are superior to the single-phase ones for high-power application due to the following:

- Reduced current stress on the MOSFETs due to lower rms current through them;
- Higher power transfer with better utilization of the transformer;
- Higher efficiency; and
- Improved power density and reduced passive components' size.

The increase in the ripple frequency of passive components to three times of the switching frequency improves the power density of the converter. Of all the conventional topologies of current-fed three-phase converters, the push-pull topology is

advantageous over others because of only having low side switches and a simple gate driver circuit, which reduces the cost of the system and increases the reliability of the converter, and only having one input dc inductor with the ripple frequency three times the switching frequency. Hence, an optimal choice between power density and efficiency has to be made considering the aforementioned factors based on the application [16], [17]. The objectives of this paper are to present the steady-state analysis and operation of the proposed novel and innovative modulation technique and the design of the converter along with experimental results. This paper has been organized as follows.

## II OPERATING PRINCIPLE OF THE CONVERTER

### A. Topology Description

The circuit of the single inductor bidirectional snubberless current-fed three-phase push-pull dc-dc converter is shown in Fig. 1. A low voltage (LV) energy source or dc bus is connected to the low voltage side (LVS) current-fed port, and the high voltage side (HVS) is connected to the dc grid to feed the dc load and/or for dc/ac inverter interface. In the boost mode, the boost function is achieved by the dc input inductor and three LV side switches connected in push-pull configuration.

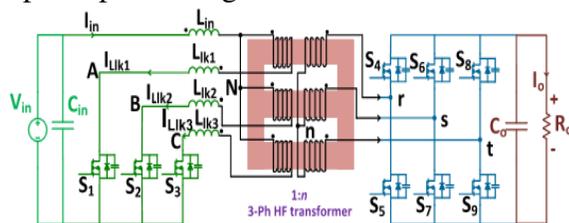


Fig.1. Three-phase current-fed push-pull bidirectional dc-dc converter

In the buck mode, the high voltage (HV) six-pack switches are used for power transfer, and the dc inductor acts as a filter. Three single-phase transformers connected in Y-Y configurations are implemented to reduce the circulating current and reduce the phase current imbalance. Inductances  $L_{lk1}$ ,  $L_{lk2}$ , and  $L_{lk3}$  represent the sum of the leakage inductances of the transformer and external inductances added to each phase as per the required power transfer if needed. The leakage inductances are utilized to achieve the soft switching of the HF switching devices. The steady-state analytical waveforms are shown in Fig. 2. The steady-state operation of the converter has been divided into eight modes of operation for one-third of the HF cycle.

### B. Modulation Technique

The gating signals to the active devices on the three legs on both LV and HV sides are  $120^\circ$  phase shifted. For 8x voltage gain with low turns ratio, the duty ratio is kept high. For full load condition, the duty cycle (d) of each switch on the LV side is set at 73% with an overlap of nearly 42%. On the HV side, most of the time, antiparallel diodes of active switches are utilized for rectification. They are turned on for a short duration to obtain the LV side switches' soft turnoff. The HV active switches are turned on for  $2\pi/3$  with diagonal switches having the same gating pulses. To reduce the degrees of freedom of operation, the HV side active switches' gating pulses are kept fixed, and the power transfer equation is obtained as a function of the LV side duty and the phase shift between LVS and HVS.

A maximum power is transferred for a phase shift of  $d/3$ , keeping all other parameters constant. For full-load condition, the phase shift is kept at  $d/6$  to achieve the required power transfer. When the HV side device is turned on, it causes a negative voltage to impress across the corresponding phase leakage inductance of the transformer, which forces the current in the LV side to change its direction. Thus, the anti parallel body diode of the LV switch in that phase takes over the current and turns off naturally with zero current switching (ZCS). Also, an HV side device is triggered and conducts current when its body diode is doing rectification, thus causing zero voltage (ZV) across the device and turning on with zero voltage switching (ZVS). Hence, the soft turn-on of HV side active devices and the soft turn-off of LV side active devices are achieved.

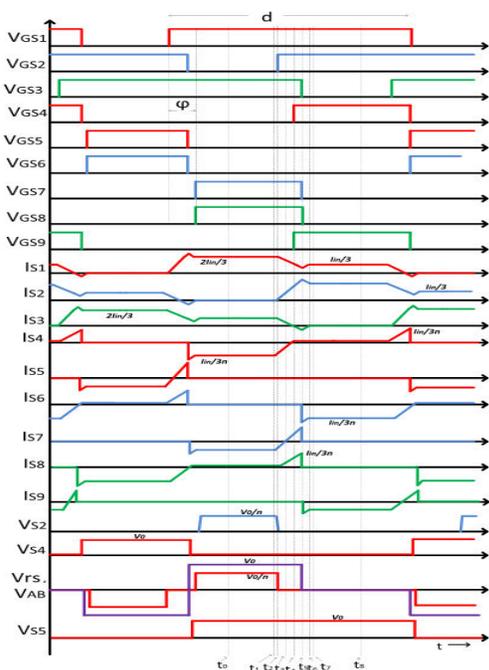


Fig.2. Steady-state theoretical waveforms of the proposed converter

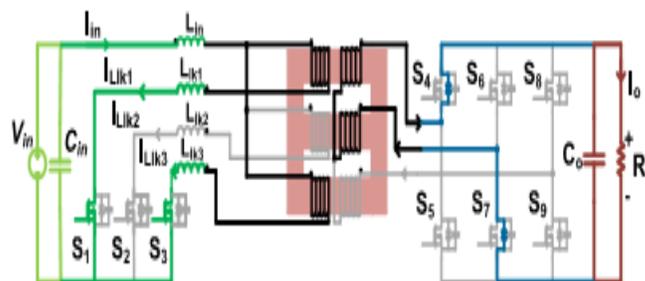
### C. Principle of Operation

**Mode I :** (Fig. 3.3(a);  $t_0-t_1$ ): At  $t=t_0$ , LV switches  $S_1$  and  $S_3$  and the antiparallel body diodes  $D_{S4}$  and  $D_{S7}$  of HV switches  $S_4$  and  $S_7$ , respectively, are conducting to transfer power. Nonconducting HV devices  $S_6$ ,  $S_9$ , and  $S_5$  block the output voltage  $V_0$ , and on the LV side, switch  $S_2$  is naturally clamped at  $V_0/n$ . The steady-state current values through different components at  $t=t_1$  are as follows.

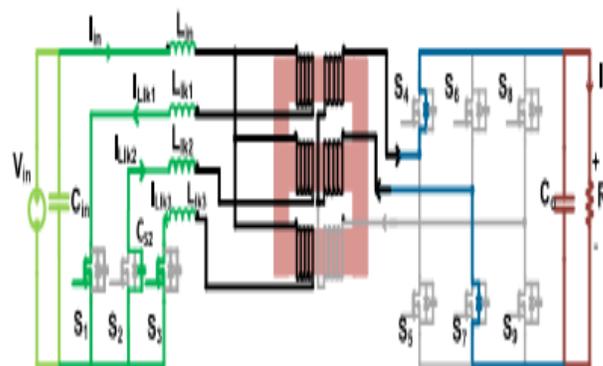
On the LV side:  $I_{S1}=I_{Lk1}=2I_{in}/3$ ;  $I_{S3}=I_{Lk3}=I_{in}/3$ ;  $I_{S2}=0$ .

On the HV side:  $I_{DS4}=I_{in}/3n$ ;  $I_{DS7}=I_{in}/3n$ ;  $I_{S5}=I_{S6}=I_{S8}=I_{S9}=0$ .

**Mode II :** (Fig. 3.3(b);  $t_1-t_2$ ): This mode persists for short duration. This mode ends when the parasitic capacitance of  $S_2$  is fully discharged. The currents through all other components and the voltages across them remain the same.



(a)



(b)

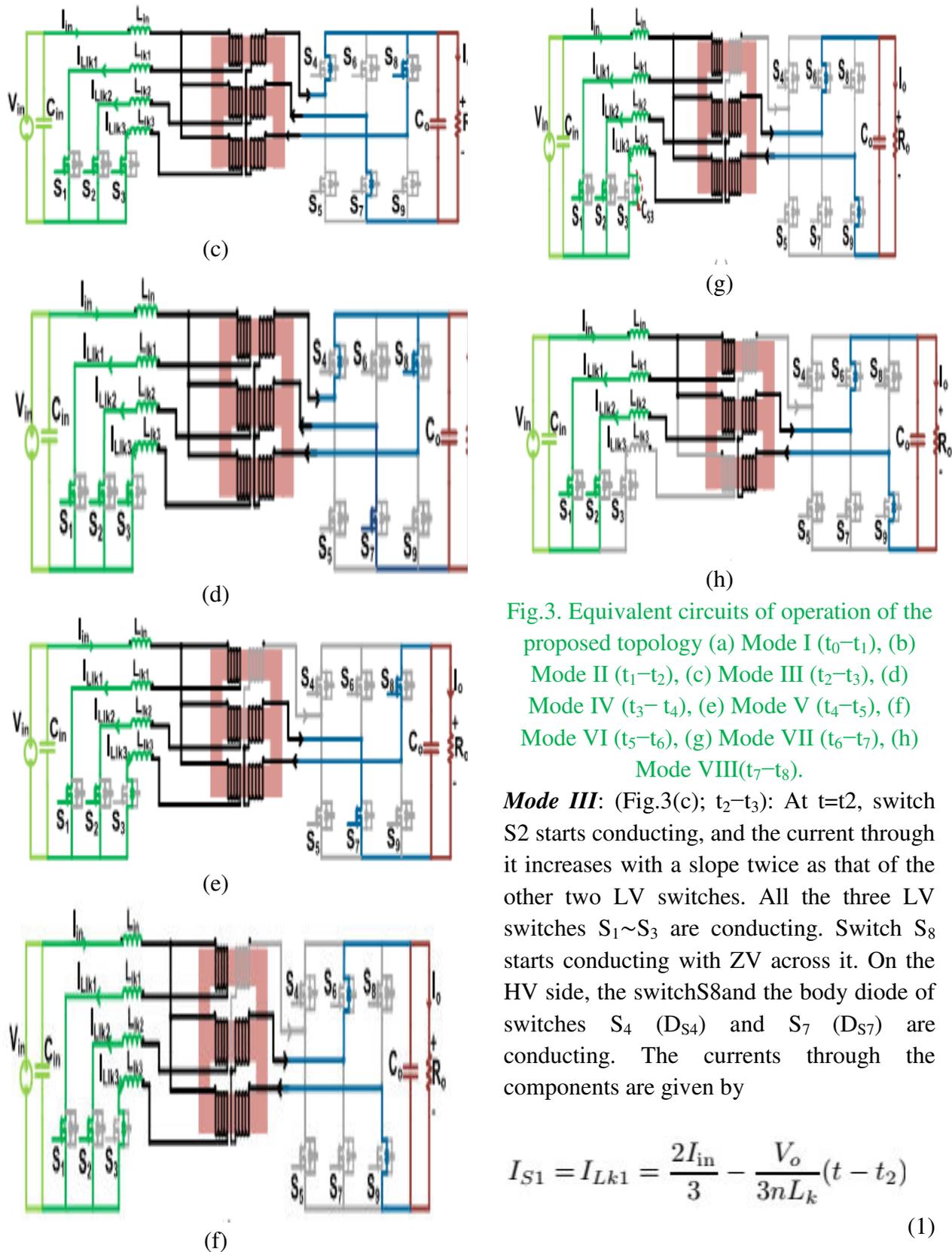


Fig.3. Equivalent circuits of operation of the proposed topology (a) Mode I ( $t_0-t_1$ ), (b) Mode II ( $t_1-t_2$ ), (c) Mode III ( $t_2-t_3$ ), (d) Mode IV ( $t_3-t_4$ ), (e) Mode V ( $t_4-t_5$ ), (f) Mode VI ( $t_5-t_6$ ), (g) Mode VII ( $t_6-t_7$ ), (h) Mode VIII( $t_7-t_8$ ).

**Mode III:** (Fig.3(c);  $t_2-t_3$ ): At  $t=t_2$ , switch S2 starts conducting, and the current through it increases with a slope twice as that of the other two LV switches. All the three LV switches  $S_1 \sim S_3$  are conducting. Switch  $S_8$  starts conducting with ZV across it. On the HV side, the switch  $S_8$  and the body diode of switches  $S_4$  ( $D_{S4}$ ) and  $S_7$  ( $D_{S7}$ ) are conducting. The currents through the components are given by

$$I_{S1} = I_{Lk1} = \frac{2I_{in}}{3} - \frac{V_o}{3nL_k}(t - t_2) \quad (1)$$

$$I_{S2} = I_{Lk2} = \frac{2V_o}{3nL_k}(t - t_2) \quad (2)$$

$$I_{S3} = I_{Lk3} = \frac{I_{in}}{3} - \frac{V_o}{3nL_k}(t - t_2) \quad (3)$$

$$I_{DS4} = \frac{I_{in}}{3n} - \frac{V_o}{3n^2L_k}(t - t_2) \quad (4)$$

$$I_{S8} = \frac{V_o}{3n^2L_k}(t - t_2) \quad (5)$$

$$I_{DS7} = \frac{I_{in}}{3n} - \frac{2V_o}{3n^2L_k}(t - t_2) \quad (6)$$

The components' current and voltage values at instant  $t_3$  are as follows.

On the LV side:  $I_{S1}=I_{Lk1}=I_{in}/2$ ;  $I_{S2}=I_{Lk2}=I_{in}/3$ ;  $I_{S3}=I_{Lk3}=I_{in}/6$ .

On the HV side:  $I_{DS4}=I_{in}/6n$ ;  $I_{DS8}=I_{in}/6n$ ;  $I_{S5}=I_{S6}=I_{S7}=I_{S9}=0$ ;  $V_5=V_6=V_9=V_0$ .

**Mode IV:** (Fig. 3(d);  $t_3-t_4$ ): In this interval, the slopes of the currents through the components remain the same. The HV side switch  $S_7$  takes over the current immediately by ZVS turn on by the end of the interval. This mode ends when the switch  $S_3$  current reaches zero and the diode conducts naturally.

**Mode V:** (Fig.3 (e);  $t_4-t_5$ ): At  $t_4$ , the body diode of switch  $S_3$  ( $D_{S3}$ ) starts conducting, causing extended ZV to appear across the switch to ensure ZCS turnoff. The slope of the currents through the switches remains the same. Hence, the current through  $S_1$  reduces below  $I_{in}/3$ . This mode lasts for a short duration of time to avoid the conduction loss through the body diode and

limit the peak current through the switches and transformers and their kVA rating. This mode ends with the following.

On the LV side:  $I_{S1}=I_{Lk1}=(I_{in}/3-I_{DS, peak})$ ;  $I_{S2}=I_{Lk2}=(2I_{in}/3+2I_{DS, peak})$ ;  $I_{S3}=I_{Lk3}=-I_{DS, peak}$ .

On the HV side:  $I_{S8}=I_{S7}=I_{in}/3n+2I_{DS, peak}/n$ ;  $I_{S4}=I_{S5}=I_{S6}=I_{S9}=0$ ;  $V_5=V_6=V_9=V_0$ .

The governing equations for this mode are

$$I_{S1} = I_{Lk1} = \frac{I_{in}}{3} - \frac{V_o}{3nL_k}(t - t_4) \quad (7)$$

$$I_{S2} = I_{Lk2} = \frac{2I_{in}}{3} + \frac{2V_o}{3nL_k}(t - t_4) \quad (8)$$

$$I_{S3} = I_{Lk3} = -\frac{V_o}{3nL_k}(t - t_4) \quad (9)$$

$$I_{S8} = \frac{I_{in}}{3n} + \frac{2V_o}{3n^2L_k}(t - t_4) \quad (10)$$

$$I_{S7} = \frac{I_{in}}{3n} + \frac{2V_o}{3n^2L_k}(t - t_4) \quad (11)$$

**Mode VI:** (Fig.3(f);  $t_5-t_6$ ): During this mode, the currents through the switches  $S_7$  and  $S_8$  drop to zero and are taken over by the ant parallel diodes of switches  $S_6$  and  $S_9$ . The current through the body diode of  $S_3$  reduces to zero with the same slope, thus naturally commutating. The equations during this mode are given by

$$I_{S1} = I_{Lk1} = \frac{I_{in}}{3} - I_{D,peak} + \frac{V_o}{3nL_k}(t - t_5) \quad (12)$$

$$I_{S2} = I_{Lk2} = \frac{2I_{in}}{3} + I_{D,peak} - \frac{2V_o}{3nL_k}(t - t_4) \quad (13)$$

$$I_{S3} = I_{Lk3} = -I_{D,peak} + \frac{V_o}{3nL_k}(t - t_5) \quad (14)$$

The final values at  $t_6$  are as follows.

On the LV side:  $I_{S1}=I_{Lk1}=I_{in}/3$ ;  $I_{S2}=I_{Lk2}=2I_{in}/3$ ;  $I_{S3}=I_{Lk3}=0$ .

On the HV side:  $I_{Ds6}=I_{in}/3n$ ;  $I_{Ds9}=I_{in}/3n$ ;  $I_{S4}=I_{S5}=I_{S7}=I_{S8}=0$ ;  $V_5=V_7=V_8=V_0$ .

**Mode VII:** (Fig.3(g);  $t_6-t_7$ ): The voltage across  $S_3$  clamps to  $V_0/n$  naturally. This mode is for a short duration of time until the switch  $S_3$  enters into forward blocking mode. The values of current and voltage across other switches remain the same.

**Mode VIII:** (Fig.3(h);  $t_7-t_8$ ): In this mode, the currents through the switches, external leakage inductors, and HF transformers are constant. The time interval for this mode is longer compared to other intervals. The currents through the switches  $S_1$  and  $S_2$  are  $I_{in}/3$  and  $2I_{in}/3$ , respectively, and the currents through the antiparallel diodes of  $S_6$  and  $S_9$  are  $I_{in}/3n$ . The voltage across the switch  $S_3$  is clamped to  $V_0/n$  naturally, and the voltage across the non conducting switches on the HV side  $V_8$ ,  $V_5$ , and  $V_7$  is  $V_0$ .

### III CONVERTER DESIGN

#### A. Design of the Converter

The theoretical study of the converter is validated by simulation using PSIM 9.3 for the following system specifications: Input voltage  $V_{in} = 40-59V$ , nominal input voltage  $= 48V$ , nominal output voltage  $V_o = 380V$ , operating switching frequency  $f_s = 70kHz$ , and the output power  $P_o = 1kW$ . The voltage gain equation found by applying

volt-second balance across the boost inductor is given by

$$V_o = \frac{nV_{in}}{1-d} \quad (15)$$

Since the three-phase current-fed converter requires a boost ratio of 1:8, the duty ratio is always greater than 67%. Hence, for a duty ratio of 73%, the turn's ratio is calculated to be  $n \approx 2$ . The formula for voltage gain for varied load condition is given by

$$V_o = \frac{nV_{in}}{1-d-d''} \quad (16)$$

Where  $d''$  is a negative term to reduce the effective duty with decrease in load and given by

$$d'' = \frac{3nL_{lk}I_{in}f}{2V_o} + \frac{2}{3} - d \quad (17)$$

Table I  
Current stress in the switches

Components	Peak Current	RMS Current	Average Current
LV switches $S_1-S_3$	$I_{S1,peak} = \frac{2I_{in}}{3}$ (25A)	$I_{S1,rms} = I_{in} \sqrt{\frac{7-3d}{27}}$	$I_{S1,avg} = \frac{I_{in}}{3}$
HV top switches $S_6, S_9$	$I_{S6,peak} = \frac{I_{in}}{3n}$ (3A)	$I_{S6,rms} = \frac{I_{in}}{9n} \sqrt{3d-2}$	$I_{S6,avg} = \frac{I_{in}}{6n} (d - \frac{2}{3})$
HV top switches body-diode	$I_{D6,peak} = \frac{I_{in}}{3n}$ (3A)	$I_{D6,rms} = \frac{I_{in}}{9n} \sqrt{7-6d}$	$I_{D6,avg} = \frac{I_{in}}{18n} (4-3d)$
HV bottom switches $S_2, S_3$	$I_{S2,peak} = \frac{I_{in}}{3n}$ (3A)	$I_{S2,rms} = \frac{I_{in}}{9n} \sqrt{\frac{3d-2}{2}}$	$I_{S2,avg} = \frac{I_{in}}{36n} (3d-2)$
HV bottom switches body-diode	$I_{D2,peak} = \frac{I_{in}}{3n}$ (3A)	$I_{D2,rms} = \frac{I_{in}}{9n} \sqrt{\frac{16-15d}{2}}$	$I_{D2,avg} = \frac{I_{in}}{36n} (10-9d)$

Switches: The LV side of the transformer has only three switches with a voltage rating

greater than the clamped voltage  $V_0/n$ . The HV side comprises six switches with a voltage rating greater than  $V_0$ . Table I lists the current stress through the nine switches. The selection of switches is based on the clamping voltage, the rms current, the total gate charge ( $Q_{gs}+Q_{gd}$ ) for low turn-on losses in the LV side switches, the low voltage drop across the diode for low conduction losses in the HV switches, and the low parasitic capacitance to reduce loss associated with the snubber circuits [18]. Also, for the paralleling of switches, the heat sinks are designed to ensure that the thermal junction temperature is maintained within  $40^\circ\text{C}$  [19]. The power loss in the switches for temperature calculation is obtained considering two switches in parallel. However, for optimal condition with an aim to improve the efficiency of the converter, more number of switches can be connected in parallel to reduce the conduction losses incurred.

**Boost Inductor:** The value of the boost inductance is given by the formula

$$L = \frac{V_{in} \left(d - \frac{2}{3}\right)}{\Delta I f_s} \quad (18)$$

Assuming a ripple of 1.5 A in the input current, the value is obtained as 26  $\mu\text{H}$ . For the boost inductor with high dc offset current, dc winding losses and core saturation are the main limitations. Hence, the toroidal core MS-250060-2 with a maximum flux density of 1.0 T is chosen for the design. Assuming that  $B_m=0.7\text{T}$ , the practical value of the boost inductor is 140  $\mu\text{H}$  since the inductance value reduces with increase in current in powered core. Three-

**Phase HF Transformer:** Three independent HF ETD cores of ferrite material are connected in Y-Y connection to form the three-phase transformer. The kVA rating of each transformer is given as

$$V A_{1-ph} = \frac{V_0 I_{in}}{3n} \sqrt{\frac{(4-3d)(7-3d)}{27}} \quad (19)$$

The required area product of the core can be obtained as

$$A_p = \frac{\pi \cdot P_{out}}{9 B_m \cdot K_w \cdot J (1-d)} \left\{ \sqrt{\frac{7-3d}{27}} + \frac{1}{9} \sqrt{\frac{3d+10}{2}} \right\} \quad (20)$$

In the push-pull topology with three single-phase transformers, at any given instant, one transformer delivers the power to the output (forward behavior), another phase transformer stores the energy in its magnetizing inductance (flyback behavior), and the third phase transformer's magnetizing inductance delivers the power to the output (flyback behavior). Hence, the  $B_m$  is chosen very less to avoid core saturation. With  $B_m=0.1\text{T}$ ,  $J=4\text{A/mm}^2$ , and  $k_w=0.3$ , the area product is calculated to be 8.05  $\text{cm}^4$ . Allowing some margin, the ferrite core 3C95ETD49 of  $A_p=16.9\text{cm}^4$  is preferred. The leakage inductance of the converter is given by the slope through the transformer as

$$L_k = \frac{V_0 \left(d - \frac{2}{3}\right)}{n f I_{in}} \quad (21)$$

$$P_o = \frac{V_o^2}{2\pi n^2 \omega L_{lk}} \left\{ -\frac{13}{16} \varphi^2 + \frac{5\pi}{6} \varphi + d \left( \frac{d}{16} - \frac{\varphi}{4} \right) - \frac{\pi^2}{9} \right\} \quad (22)$$

## B. Soft-Switching Conditions

For secondary-side modulated ZCS turnoff of LVS active switches, the duty ratio of HVS active switches is given as

$$d' \geq d - \frac{1}{3} - \varphi \quad (23)$$

$$i_{lk}(t = \{(2d - 2/3 - \varphi)2\pi\}) > 0, \text{ for upper switches} \quad (24)$$

$$i_{lk}\left(t = \left\{\frac{4\pi}{3} - (2d - 2/3 - \varphi)2\pi\right\}\right) > 0, \text{ for lower switches} \quad (25)$$

This paper presents a single-phase five-level photovoltaic (PV) inverter topology for grid-connected PV systems with a novel pulse width-modulated (PWM) control scheme. Two reference signals identical to each other with an offset equivalent to the amplitude of the triangular carrier signal were used to generate PWM signals for the switches. A digital proportional-integral current control algorithm is implemented in DSP TMS320F2812 to keep the current injected into the grid sinusoidal and to have high dynamic performance with rapidly changing atmospheric conditions. The inverter offers much less total harmonic distortion and can operate at near-unity power factor. The proposed system is verified through simulation and is implemented in a prototype, and the experimental results are compared with that with the conventional single-phase three-level grid-connected PWM inverter.

## IV A grid-connected photovoltaic power system, or grid-connected PV system

A grid-connected photovoltaic power system or grid-connected PV system is

an electricity generating system that is connected to the utility grid. A grid-connected PV system consists of solar panels, one or several inverters, a power conditioning unit and grid connection equipment. They range from small residential and commercial rooftop systems to large utility-scale solar power stations. Unlike stand-alone power systems, a grid-connected system rarely includes an integrated battery solution, as they are still very expensive. When conditions are right, the grid-connected PV system supplies the excess power, beyond consumption by the connected load, Residential, grid-connected rooftop systems which have a capacity more than 10 kilowatts can meet the load of most consumers.<sup>[2]</sup> They can feed excess power to the grid where it is consumed by other users. The feedback is done through a meter to monitor power transferred. Photovoltaic wattage may be less than average consumption, in which case the consumer will continue to purchase grid energy, but a lesser amount than previously. If photovoltaic wattage substantially exceeds average consumption, the energy produced by the panels will be much in excess of the demand. In this case, the excess power can yield revenue by selling it to the grid. Depending on their agreement with their local grid energy company, the consumer only needs to pay the cost of electricity consumed less the value of electricity generated. This will be a negative number if more electricity is generated than consumed.<sup>[3]</sup> Additionally, in some cases, cash incentives are paid from the grid operator to the consumer.

Connection of the photovoltaic power system can be done only through an interconnection agreement between the consumer and the utility company. The agreement details the various safety standards to be followed during the connection.

## V.MATLAB/SIMULATION RESULTS

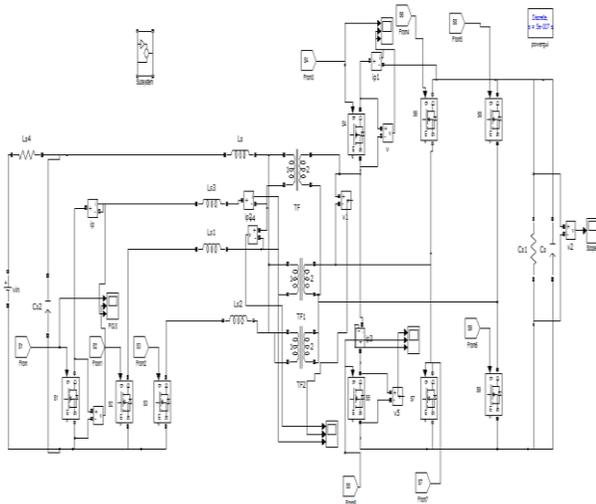


Fig 4 Matlab/simulation circuit current-fed push-pull bidirectional dc-dc converter.



Fig 5 Simulation wave form of the line voltage  $V_{AB}$  across the primary and secondary of the transformer and the line current  $I_{ik1}$

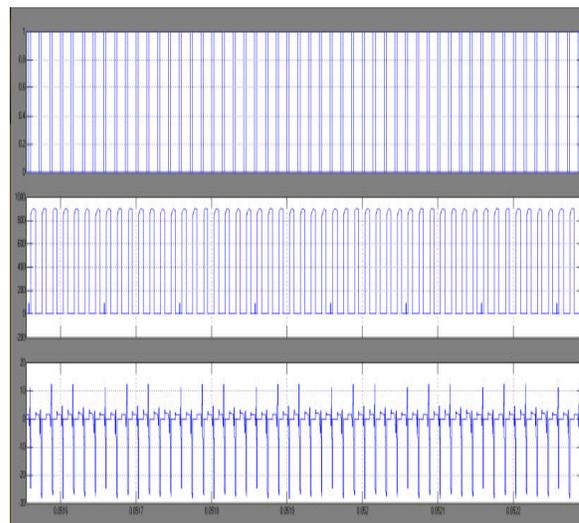


Fig 6 simulation wave form of Voltage, gate pulse, and current for switch  $S_1$ , voltage, gate pulse, and current for switch  $S_4$ , voltage, gate pulse, and current for switch  $S_5$

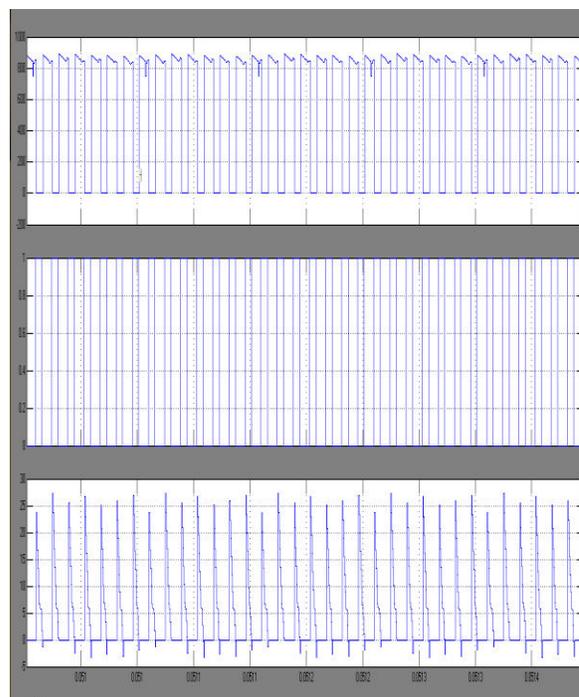


Fig 7 simulation wave form of the line voltage  $V_{AB}$  across the primary and secondary of the transformer and the line current  $I_{ik1}$  at half load (500 W), an voltage, gate pulse, and current for switch  $S_1$

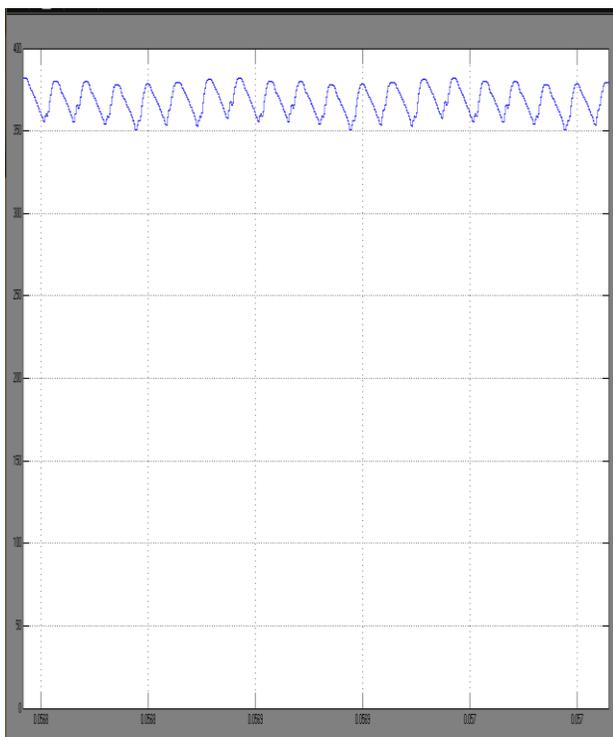


Fig 8 Simulation wave form current-fed push-pull bidirectional dc-dc converter output voltage

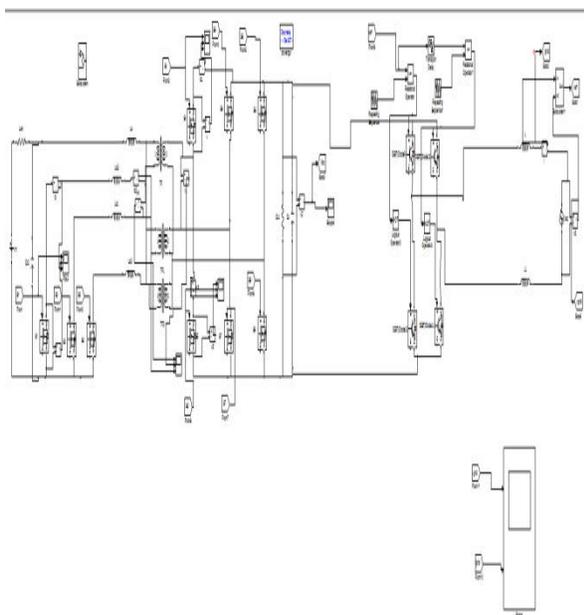


Fig 9 Matlab/simulation circuit current-fed push-pull bidirectional dc-dc converter with Grid connection

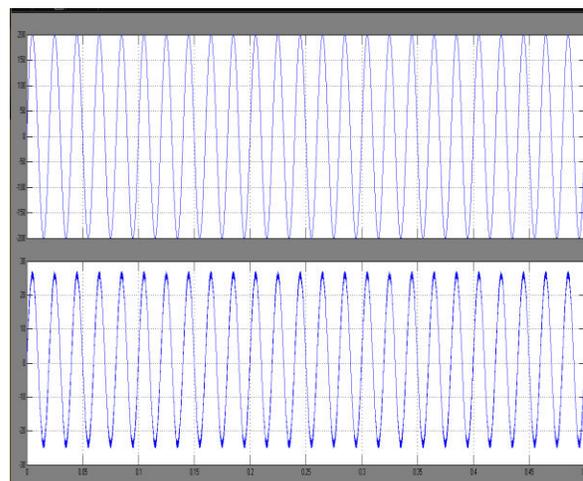


Fig 10 Simulation wave form of current-fed push-pull bidirectional dc-dc converter with Grid voltage and current

## CONCLUSION

A current-fed three-phase push-pull bidirectional dc-dc converter is proposed with Grid connected system. A novel innovative modulation is implemented for the natural zero current commutation of LVS devices with natural device voltage clamping eliminating the traditional active-clamp or dissipative snubber circuit, making the topology snubberless. The ZVS turn-on of HVS devices is obtained. These merits and unique features are inherent and maintained with variation in input voltage and load current. Higher switching ripple frequency (three times the device switching frequency) enhances the power density, making it suitable for high-power application. The complete steady-state analysis, operation, and design with the proposed modulation scheme are explained. High efficiency for wide variation in source/dc bus voltage and validate the claims grid connected system. Peak efficiencies of 95.8% and 93.8% are

obtained at half-load condition for an input voltage of 59 V and nominal voltage (48 V), respectively. Along with it, the experiment of the reverse direction of power flow, i.e., charging of battery, is demonstrated with DPSP.

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