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CMOS REALIZATION OF LOW POWER MIXING DRIVERS IN CLOCK TREE

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Abstract—In today's process technologies, power supply noise may cause serious clock jitter and circuit malfunction. Noise occurs by the fast and simultaneous voltage switching. A primary contributor to the noise is the clock-tree and the underlying sequential circuits that switch simultaneously, thus causing high current peaks. This work proposes to spread the switching of the clock-tree drivers, while maintaining low skew at the sinks of the tree, where the clocked circuits are connected. Driver switching characterization has been used for fast computation of peak currents, delays and slopes, integrated in a two-phase algorithm. It first constructs the clock-tree in a top-down traversal, employing a mix of high threshold voltage (HVT) and weak low threshold voltage (LVT) clock-drivers. A bottom-up delay correction phase then takes place, aiming at clock skew minimization. The algorithm was implemented in 40 nanometers TSMC process technology, achieving 35% to 70% clock-tree peak current reduction, translated to similar reduction in power supply noise. The proposed method can easily be combined with other existing methods to further reduce the noise.

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I.INTRODUCTION

The power supply instantaneous voltage drop in today's VLSI designs, known as power supply noise (henceforth noise for short), is a major concern [1]. Noise of a very few hundreds milli volts causes clock jitter and circuit malfunction [2]. Process technology scaling escalates the fluctuations occurring in and . There, the underlying resistance, capacitance, and peak current switching are growing up, thus increasing the noise. The voltage drop incurred by the power supply in today's VLSI chips is a major concern known as power noise [1]. With the increase of design complexity, moving from Application Specific Integrated Circuits (ASIC) to System on a Chip (SoC), and due to the sub-1volt supply voltage, noise of very few hundreds milli volts causes circuit malfunction [2]. The fluctuations occurring in the high power supply Vdd and the low power supply Vgnd voltages are escalated by the process technology scaling. There, the underlying resistance, capacitance and peak current are increasing, and the current switching becomes faster, namely dI dt grows up, thus increasing the power noise. A typical model of power delivery network is illustrated in Fig. 1 [1].

The network consists of a power supply located on the board, power consumers (system's logic circuits), and power and ground supply network (PDN). The power supply is assumed to behave as an ideal voltage source providing nominal Vdd and Vgnd . The power consumers are modeled as time-dependent current sources, denoted by I(t). Ordinary logic and sequential circuits are designed to work in nominal power supply voltage. Unfortunately maintaining constant voltage during operation is practically impossible. It all comes to the simple Ohm low of multiplying peak current by the power network impedance. The power network is an RLC circuit and high current peaks will thus cause various voltage drops at various points of the network. The noise can therefore be reduced by lowering the impedance, or avoiding high current peaks.

Constructing proper power supply network having low-resistance and inductance, and high capacitance has been treated by many research papers [3-5], and its discussion is beyond the scope of this work, focusing on reducing the peak current. Power noise can be controlled by reducing the PDN parasitic resistance R and inductance L , and by lowering the current I and its density dI dt . Both techniques were extensively studied in the literature. In [4] PDN parasitic resistance and inductance reduction were studied.

Peak current reduction achieves the following goals. 1. Reduction of the on-die IR drop, where the resistance dominates the impedance. 2. Reduction of the) (L dI dt term occurring at the package level, where the inductance factor dominates the impedance. 3 3. Reduction of the clock jitter which is directly affected by IR drop [7]. 4. Improving the utilization of the de-coupling capacitors by increasing the effective distance of the capacitors, that is inversely proportional to dI dt [6]. In [6] it was proposed to employ decoupling capacitors, hence reducing the effective R and L (and also the resonance factors). The reduction of dI dt is obtained by improving the current sources. That can also be achieved by decoupling capacitors (though the reduction mechanism is different). The clock related voltage switching is the primary contributor to power supply noise [8]. While the logic signal switching is spread across the entire clock cycle, the switching of the clock-tree and the sequential circuits is occurring simultaneously, causing high current peaks.

The clock network is therefore a natural candidate to treat for reducing peak current. A well-structured clock-tree should deliver high quality clock signal to the underlying sequential circuits connected at the tree's leaves. To obtain proper and robust sequencing of the logic, the clock skew must stay within prescribed limits, usually not exceeding 5% of the clock cycle [9]. To ensure fast switching of the logic, the slope of the signal at tree's leaves must also be sufficiently small. Reducing the power supply peak current by clock-tree treatment is therefore a delicate task that must be handled carefully to ensure clock signal integrity. For that, three approaches have

been proposed in the literature. The first aims at reducing the power network impedance. Though it does not change the peak current, the voltage drop does reduce. This approach comprises well established techniques such as reducing the resistance of the power network by widening the power rails, increasing their density, and extensive usage of vias. Another technique is using decoupling capacitors, to effectively shorten the distance of the current sinks from their sources. Such techniques are being used since the early days of VLSI design. An excellent review of those methods is found in [6].

A second technique [10] proposed to reduce the peak current by minimizing its component caused by the flip-flops (FFs) switching. Its underlying idea is illustrated in Fig. 2. In (a) the clock signals of the FFs are aligned, causing a large and narrow supply current pulse, compared to (b) where the clock signals are displaced, and the resulting current pulse is smaller and spread over time. To account for the peak current, the signal switching [10] accounted only the first level of the combinational logic, assuming that the switching factor at deeper levels is far smaller than at the first level. Peak current reduction was achieved by clock scheduling procedure which utilized the allowable clock skew, a technique first proposed for timing optimization in a seminal paper [11]. Clock signal rescheduling at FFs' clock inputs may considerably complicate the timing convergence of the underlying design. Peak current minimization by [10] could not be handled by the linear programming solution used in [11], and a heuristic based on genetic algorithm was proposed, yielding 30% of FFs peak current reduction, without sacrificing the clock frequency. A refinement of [10] was presented in [8], which accounted all the switching of deeper logic levels. A more modest, but still significant peak current reduction of 12% was claimed, which lead to 19% reduction of the power supply voltage variation.

A heuristic to enhance the quality of the genetic algorithm solution was presented in [12]. Paper [13] presents another skew spreading optimization technique by dividing the skew time intervals into slots

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and then the 4 clock timing of each FF was allocated to some slot in an attempt to reduce the peak current. 17% peak current reduction was claimed.

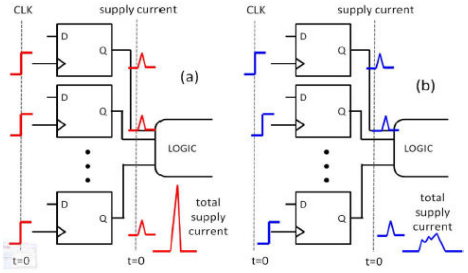

Fig. 1. Peak supply current reduction by clock signal misalignment.

All the above works used current profiling of the gates involved in the combinational logic. While [10] and [12] required full current characterization of the logic gates involved and thus employed extensive SPICE simulations, [8] used only the peak current of those gates, making the CAD solution simpler and easier to maintain on the account of accuracy. All those methods approximated the current waveforms by triangles, which were scheduled according to the switching time of their corresponding gates (see Fig. 2). The entire current profile drawn from the power supply was obtained by a superposition of the individual current profiles. Our work uses similar current profile methodology with full SPICE characterization. For our work SPICE accuracy is essential since unlike the above mentioned methods, we pursue zero-skew. As in [8,10,12,13], our work is flattening the peak supply current by manipulating the timing of the clock signal. There is a major difference though, which avoids the timing

side effects difficulties mentioned before. While the former methods shift the clock signal at the far-end of its distribution network, as shown in Fig. 2, our method does so only at the internal nodes of the clock-tree, while the skew at the its far-end nodes is fully controlled and maintained small. Furthermore, our method is systematic and does not require extra hardware, but rather mixes clock-drivers by of low-threshold (LVT) and high-threshold (HVT) types. The other skew-driven methods add delay elements at the far-end, a reason for further design complication and extra hardware overheads.

It should be noted that the main difference among former skew spreading methods is in their spreading algorithms and current

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profiling modeling, namely, in their design flow aspects or CAD approaches. Other than that, they all use the same paradigm of skew spreading. Though skew spreading techniques deliver the premise of peak supply current reduction, they impose significant burden on the design. That follows from the consumption of the skew margin for purposes other than solving delay violations, which may make the timing convergence very difficult. Techniques as time-borrowing [14] may be not applicable, as their main resource, namely, allowable clock-skew, is being consumed for another purpose. All in all, peak supply current reduction and time-borrowing conflict with each other. A third type of methods is reducing the peak supply current by mixing clock driver polarities within the clock-tree distribution networks, claiming for 50% peak supply current reduction [15]. The idea is illustrate in Fig. 3, where the power supply current is shown for a buffer in (a) and an inverter in (b). In Fig. 4(a) an ordinary network is using positive polarity drivers (buffers), presented with underlying FFs connected at the leaves.

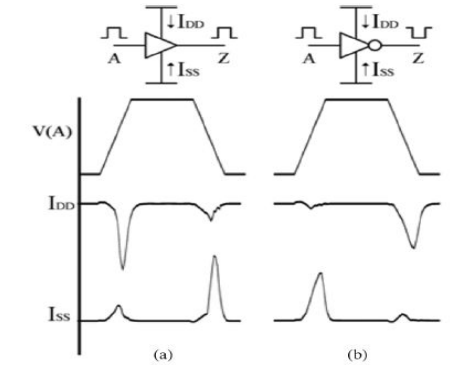

Fig. 2. The idea of buffer polarity assignment. In (a), the buffer exhibits high I_{dd} (I_{ss}) current at the rising (falling) edge of the clock signal. In (b), an opposite situation occurs for an inverter [16].

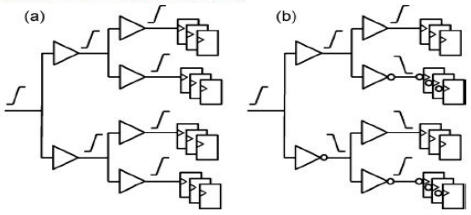

Fig. 3. Mixing polarities of clock-drivers and FFs.

A second type of methods is reducing the peak current by mixing clock-driver polarities, claiming for 50% reduction [15]. The idea is illustrate in Fig. 2, where the power supply current is shown for a buffer in (a) and an inverter in (b). In Fig. 3(a) an ordinary network is using only buffers. In Fig. 3(b), the polarities of the drivers are systematically mixed, substantially reducing the peak current. Local current peaks still exist due to the uniformity of the clock-drivers in local regions (either inverters or buffers). To remedy those peaks, [17] proposed to use the physical placement

information of the clock-drivers so that in local regions about half of the drivers are inverters and half are buffers.

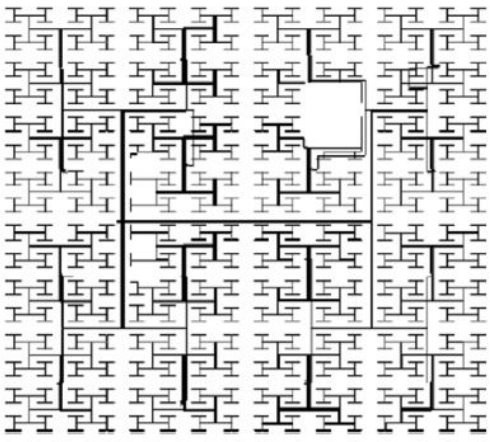

Fig. 4. An H-tree network used by IBM\Motorola PowerPC processor [24]

A problem arising by the clock-driver polarity method is the uncontrolled skew occurring by different delays of inverters and buffers residing along root-to-sink clock paths, as shown in Fig. 3(b). [18] solved the problem by sizing the clock-drivers. Clock skew aware polarity assignment was also proposed in [19]–[21] which still used single size clock-drivers. A solution of noise reduction combining sizing and polarity was described in [22]. It was lately enhanced in [16] to support multiple power modes, by dynamically controlling the internal delay of the clock-drivers. Though clock-driver polarity mix is elegant, it may impose considerable difficulties on the design. It was claimed in [15]–[22] that timing is not hurt, which is true only for logic paths connected between FFs of same polarity. Logic paths connected between different polarities unfortunately cannot be avoided. Such paths can use only half clock cycle for the logic to compute, a huge design burden.

Considerable noise reduction was lately described in [26] by using resonant clock distribution networks, generating sinusoidal signal. Its applicability to ordinary CMOS design is questionable as the short-circuit power in the clocked devices is significantly increased. The rest of the paper is organized as follows. Section II describes the clock-tree structure and how noise builds-up. Section III presents the clock-driver characterization technique for achieving computational efficiency of the algorithm. Section IV elaborates on mixing HVT and LVT drivers, followed by wire delay modeling in Section V. Section VI describes the clock-tree construction algorithm.

Section VII presents experimental results and Section VIII concludes the discussion.

II. CLOCK-TREE AND POWER SUPPLY NOISE

The construction of clock networks as a part of a SoC design offers various topologies, such as spine, mesh, grid, and trees [9]. No matter what network topology is used at the system-level, the far-end local networks are implemented as trees. Shown in Fig. 4, an H-tree topology is very popular due to its symmetry and layout efficiency. It has been used by the PowerPC processors family [23], [24], and it is supported by most clock-tree synthesis EDA tools. The elegancy of H-tree is also a source of considerable

power-noise. Due to its symmetry, all the drivers at a given level of the tree will switch simultaneously [see Figs. 1(a) and 3(a)]. This results in a progressive sequence of coherent current peaks, cumulating to a large pulse as shown by the red waveform in Fig. 5. Flattening it will reduce both IR and voltage drops. The green waveform in Fig. 5 is resulted by the clock-tree proposed in our work, showing 40% peak reduction and smaller.

To ensure a robust signal, clock-trees usually employ LVT drivers, though those consume high leakage current. The coherence of the clock signal at tree's internal nodes ensures small skew at the sinks. An important question is whether the driver uniformity and symmetry of the clock-tree is necessary for small skew, or maybe it can be differently achieved. Our proposal breaks the clock-tree symmetry and uniformity paradigm as follows.

1) It replaces half of the LVT drivers by HVT ones.

2) It “disorders” the local peaks by locally mixing HVT and LVT drivers, thus spreading and smoothing the local current waveform.

3) It maintains acceptable clock signal slope and small skew at the sinks.

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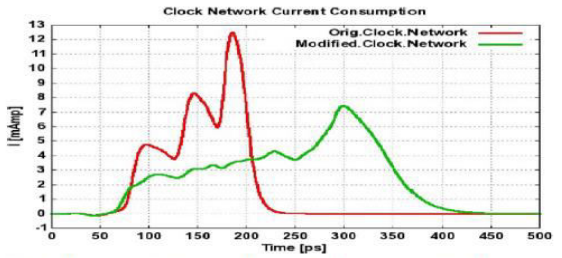

Fig. 5. Peak current flattening (SPICE simulation). An ordinary LVT tree in shown in red, while the green is produced by the tree proposed in this work.

III. CHARACTERIZATION OF CLOCK-DRIVERS

The terms nodes and drivers are used interchangeably. The clock-tree construction algorithm employs a top-down and bottom-up traversals. The visit at a node requires iterative equation solution, which involves extensive delay and slope calculations. Using in-traversal SPICE simulations is unacceptably time consuming. We rather characterize each clock-driver beforehand and then use characteristics data instead of simulations. This is far computationally efficient, whereas accuracy is hardly hurt. For an -level tree with sinks, the structure proposed in Fig. 11 results in distinct root-to-sink paths, comprising a mix of HVT and LVT/2 drives. The leftmost path is purely LVT/2, whereas the rightmost is purely HVT. An example of 3-level tree is shown in Fig. 12. The clock-tree is assumed to be binary and balanced.

IV.PEAK CURRENT REDUCTION BY CLOCK-DRIVER MIXING

This is a common assumption in the analysis of algorithms, which does not restrict the generality of the approach. A node of the tree is associated with the following parameters, derived along the tree traversal with the aid of the characteristic data of drivers.

The peak current is reduced by misaligning the drivers' switching time, obtained by systematically mixing HVT and weak LVT drivers. The notation LVT/2 denotes a weak (half size) LVT driver. A fork of an ordinary clock-tree comprises only LVT drivers is illustrated in Fig. 11. We use instead thetwo shown configurations, advised by experiments of various configurations. The replacement of an LVT driver by two LVT/2 ones has been shown to nicely spread the

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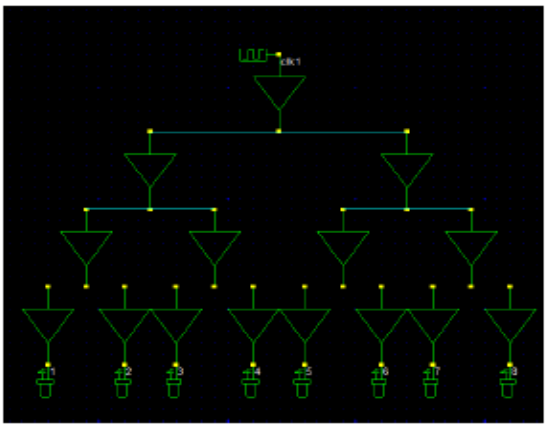
current pulse over time, while yielding sufficient dynamic range to tune-up the delays for achieving nearly zero skew. This is further shown in Figs. 13 and 14. For an - level tree with sinks, the structure proposed in Fig. 11 results in distinct root-to-sink paths, comprising a mix of HVT and LVT/2 drives. The leftmost path is purely LVT/2, whereas the rightmost is purely HVT. An example of 3-level tree is shown in Fig

SIMULATION RESULTS



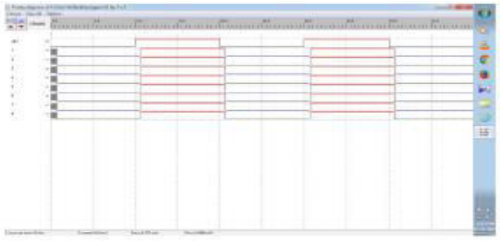


Fig: Delay of the existing system

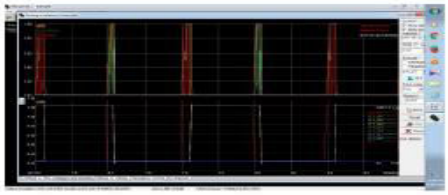


Fig: Peak current of the existing system

PEAK CURRENT REDUCTION:

In the proposed system, we use mixing of both HVT and weak LVT clock drivers in a clock tree. We use either high threshold voltage or the low threshold voltage. Herewe use 3-level mixing of HVT and weak LVT clock drivers in a clock tree[6]. This method proposed to spread the switching of the clock tree drivers, while maintaining low skew at the sinks of the tree where the clocked circuits are connected. First we can use 1-level mixing of the drivers in a clock tree there we observe

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reduction of the delay and the peak current comparing to the existing system[7]. Similarly we use the 2-level mixing of the drivers in a clock tree the delay and the peak current will be reduced comparing to the existing system.

IMPLEMENTATION RESULTS

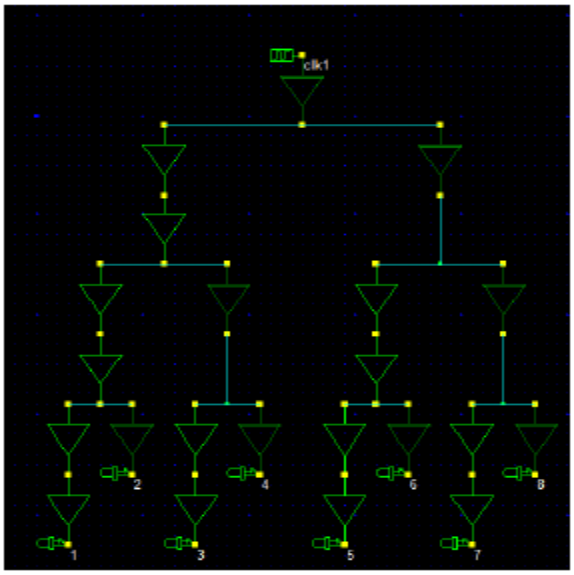

Fig:3-Level mixing of HVT and LVT drivers in clock tree.

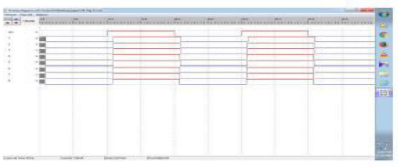

Fig: Delay of the implemented system

RESULT ANALYSIS:

The spreading over time the change of the clock-tree drivers, whereas maintaining low skew at the sinks of the tree.The unfold was achieved by compounding HVT and weak LVT drivers within the clock-tree. It had been enforced in forty nanometers TSMC method technology, achieving 35-70% clock-tree peak current reduction. Hence we can also reduce the peak current by using wire delay modeling.

CONCLUSIONS

We proposed to reduce the peak supply current and its time derivative by spreading over time the switching of the clock-tree drivers, while maintaining low skew at the sinks of the tree. The spread was achieved by mixing HVT and weak LVT drivers in the clock-tree. A two-phase top-down and bottom-up tree construction algorithm was presented. It was implemented in 40 nanometers TSMC process technology, achieving 35% to 70% clock-tree peak current reduction. The method proposed is different than other peak supply current

reduction techniques, but can easily be combined with those to further reduce power supply noise. Using for instance both buffers and inverters as in [15]–[22] will further reduce the peak current, due to the clock opposite phases.

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