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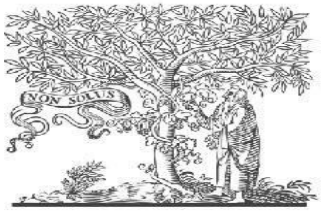

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DESIGN OF 32 BIT VLSI HYBRID ADDER

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ABSTRACT

The Adder circuit is basically required in many application of DSP digital signal processing architecture, Microprocessor, Microcontroller, Filter designing and data Processing units. A system if contains a hybrid adder than it is sure that the system must have low power consumption, high speed (Less delay) and occupies less area space in memory unit. From many years researchers are trying to make devices small in size with high operating speed and Low power consuming so they are trying various techniques In this project different 32 bit adders are studied and design implementation is done and Some 32 bit hybrid adder are proposed by using various adder combinations, Performance analysis in terms of area (according to the number of LUTs) and delay (in ns) Will be performed in Tanner tool.

Keywords: Adders, Hybrid adder, Tanner, Kogge stone adder (KSA), Carry look ahead adder (CLA), Carry Save Adder (CSA).

I. INTRODUCTION

The addition operation is a binary operation. In all calculative systems, it conducts addition, subtraction, division, multiplication, finding complement, encoding, and decoding. It is a fundamental and fundamentally significant operation. Between 1868 and 1869, Charles Webb created many patents for adding machine calculators. Many Adder topologies have been devised and deployed since they were initially introduced in the past. The majority of digital devices, such as laptops, desktop computers, notepads, and cell phones, periodically work poorly, putting users in a jam and making them believe that formatting or updating the item is the best course of action. Therefore, the best possible system is needed. The 32-bit processor architecture of a computer with processors contains, among other things, 32-bit integers, registers, and memory locations, as well as multipliers, subtractors, adders, registers, and cache. The major focus of this study is the adder circuit. Large memory unit needs, greater power consumption, and sluggish performance are the primary drawbacks of very large scale integrated circuits. It has frequently been observed that a system has to be quick, compact, and power efficient. In this study project, we are focusing on the adder circuit. If the delay is reduced, the speed can be increased. All the elements that go into a top-notch system, such as compact size, low power consumption, quick processing, and swift speed, must be prioritised. The complete high-performing system may be built using a hybrid adder structure that is added to the arithmetic unit. These adders were developed utilising various logic approaches to enhance the overall performance of the system. The main goal of hybrid logic is to reduce the number of transistors and power-dissipating nodes in the adder cell.

II. LITERATURE REVIEW

Different electronic devices have issues regarding power consumption, memory space, and data processing delays, therefore research is continuously utilizing multiple techniques and evaluating its effectiveness.

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In 0.25 micro metre CMOS technology, adders have been constructed using transistor gate logic and pass transistor logic, and their performance analysis was recorded. In 180nm technology, adders have been developed using gate diffusion and pass transistor logic. A PMOS Pull up network-based domino logic technique was employed. Parallelism and pipelining were used to design the BCD adder. Reversible logic created a method known as a quantum dot cellular automata 1-bit adder. Performance exploration was done and a redundant binary signed adder was implemented. Based on LUT, a newly developed approximate adder structure was developed and implemented into use. This was accomplished by using different adder topologies, which are also referred to as heterogeneous structures or hybrid structures. A newly designed complete adder cell with internal logic structure was successfully developed in order to reduce overall propagation delayed responses and power consumption. In order to take advantage of each type of adder architecture's advantages and enhance performance, hybrid adders combine each other. Examples include ripple carry adders (RCAs), carry look-ahead adders (CLAs), carry select adders (CSAs), and carry skip adders (CSKAs). Specific performance criteria, such as speed, power usage, or area utilization, are the term that hybrid adders are designed to optimize. Based on the requirements of the design, they are able to achieve a balance between these characteristics through the combination of several adder types.

III. CONVENTIONAL SYSTEM

Adder is an electronic circuit which generates a sum and a carry through the addition of binary values. Different adders' names have been supplied in accordance with carry-generated data. Let's explore some of the adders that have been covered at this point.

Carry Look ahead Adder (CLA)

The fundamental idea underneath this adder is to look into lower adder arguments and addend if higher orders carry generated. As a result, the amount of gates is decreased, and the delay may also be decreased. In this adder, there are two stages: the propagation stage and the generation stage, during which values are encountered along the way. The second stage calculates the carry created, and the third stage calculates the sum value. In hierarchical structures, it is utilized.

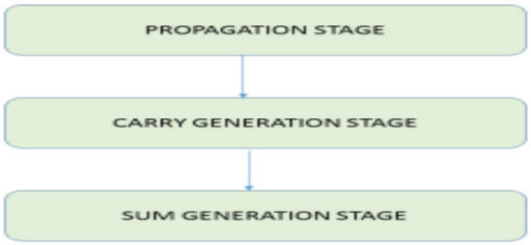

Fig.1: Working flow of CLA

Fig.1 illustrates the normal operation flow of CLA. The generation stage is another name for the propagation stage.

G(i)= a[i].b[i].....(1)

P (i) = a[i] ^ b[i].....(2)

Equations (1) and (2) are formulas of generation part and Propagating part. The internal carry is generated by formula (3)

C (i)=G(i)+ P(i).C(i-1).....(3)

The sum generation is calculated by formula (4)

Sum[i] = a[i] ^ b [i] ^ c [i-1].....(4)

Here i=1,2,3.....

Advantages

1. It is fastest adder
2. It reduce propagating delay
3. It has less number of gates

Disadvatage

1. It has complex carry logic blocks

Kogge stone adder(KSA)

In 1973, Kogge Stone introduced the Kogge Stone Adder. Preprocessing, carry production, and post-processing are each of

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the three stages of its three-stage operation. Calculating the increased are yields carry. They equation used for calculating delay is
2 log n.....(5)
n – Number of input bits

Advantages

1. It has low fan out
2. It has lowest delay
3. It has fast operation

Disadvantage

1. The functioning is very complex

Let us describe the three stages

Preprocessing stage:
Propagation and generation blocks are calculated by formula (6) and (7)
P[i] = A[i]XORB[i].....(6)
G[i] = A[i]ANDB[i].....(7)

Carry generation:
Black cell: To generate and propagate a signal, two pairs will be needed. It
generates and propagates one pair of signals in the form of an output. A generate signal is produced by the grey cell, which also provides two pairs of propagate and generate signal inputs.

Post processing:
Another name for it is final computing. It calculates bit sums. Equation (8) has the formula.
S[i] = P[i]XORC [i-1].....(8)

Advantage

1. It is fastest adder which focus on design time.

Disadvantage

2. It occupy more area in memory cell.

IV. PROPOSED SYSTEM

Hybrid Adder

A hybrid adder is one fact that has been developed by implementing one or more logical processes. Fig.2 illustrates the hybrid adder's block diagram. A and B are the inputs for modules 1, 2, and 3. We can use the same or a different type of adder to give a sum and carry it as an output. The same adder can also be used to form multiple logic values. Both logical values have benefits that indicate they can perform better.

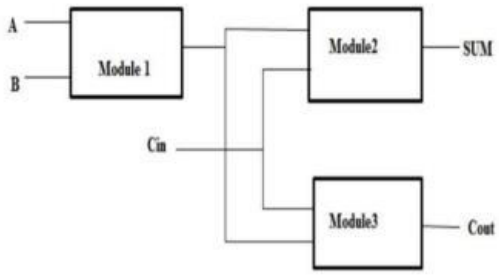

Fig.2: Block diagram of hybrid adder

There is two types of architecture of forming *hybrid adder:*

1. Homogeneous

Homogeneous architecture is created by the combination of two or more adders of the same type.

2. Heterogeneous

Merging of two or more adder forms of different types is proposed by Heterogeneous Architecture.

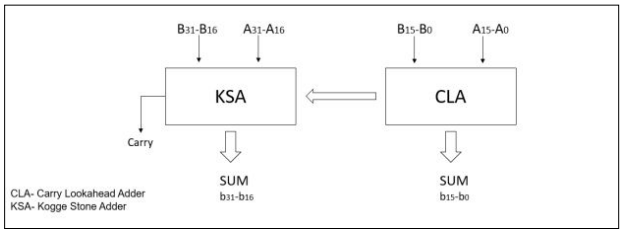

Fig.3: Block Diagram of 32-Bit Hybrid Adder

The concept of bringing together designs in order to develop a hybrid structure results in products featuring high performance and low selling price. Here, CLA and KSA adders have been constructed separately and combined to create a hybrid adder. The two hybrid adders described in this section combine a modified Manchester adder for carry propagation with

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some form of a carry-select adder to compute the sum. Both split the operands into 8-bit groups of equal size.

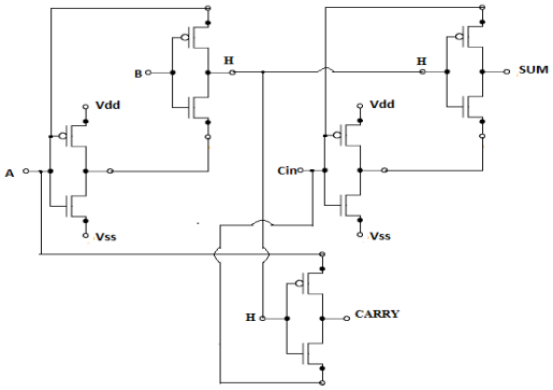

Fig.4: Schematic Diagram

The SUM and CARRY cells in the schematic design were created using the GDI approach. To implement the SUM cell and design the CARRY cell, a total of 8 transistors are required. First, the GDI approach is used to implement the H function, or XOR, after which the overall SUM and CARRY cell are implemented using this H function as input. The Proposed PTL-GDI Adder's CARRY cell shares similarities with the CARRY cell in terms of design. The illustration below represents the entire circuit. In the example, ABCin101, the PMOS transistor (where B is linked as the Gate input) is turned ON considering A is HIGH and B is LOW. This will effectively convey the value of A (i.e. H therefore possesses a value of 1. The SUM cell's NMOS transistor is now ON as the value of H is HIGH. The SUM output is going to result in logic '0' in this case. In contrast, the NMOS transistor is ON in the CARRY cell because H is HIGH. Therefore, it will send Cin's value of 1 to the CARRY output.

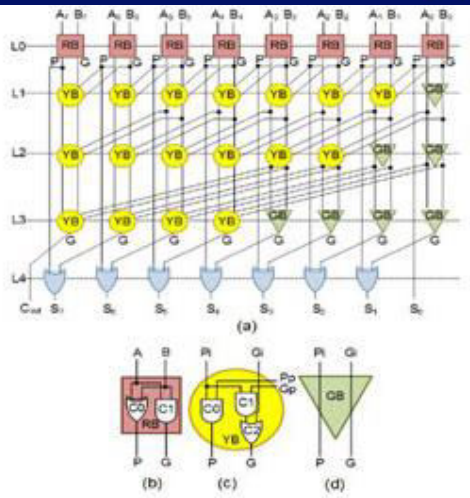

Fig.5: 8-Bit Kogge Stone Adder

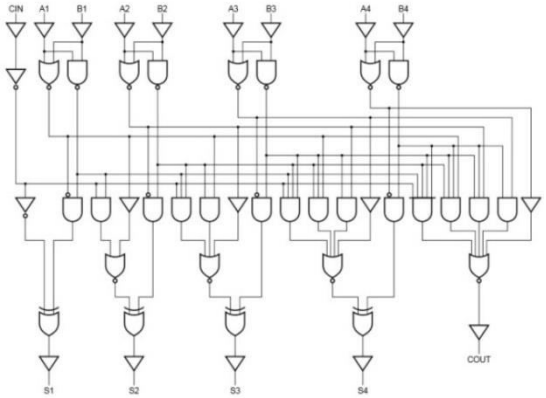

Fig.6: 4-Bit Carry Look ahead Adder

We will construct a CLA adder through an understanding of the GDI technique, where the gates, sum generation, and carry generation all have been generated through the GDI approach. First, we're going to generate a 4-bit CLA, link together it with the help of another 4-bit CLA, and then generate an 8-bit CLA. Following that, we'll construct an 8-bit KSA . By using Hybrid Heterogeneous type we will cascade it with an 8 bit CLA, and construct a 16-bit hybrid adder. subsequently, we'll combine two 16-bit hybrid adders To produce a 32-bit hybrid adder.

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V. SIMULATION RESULTS

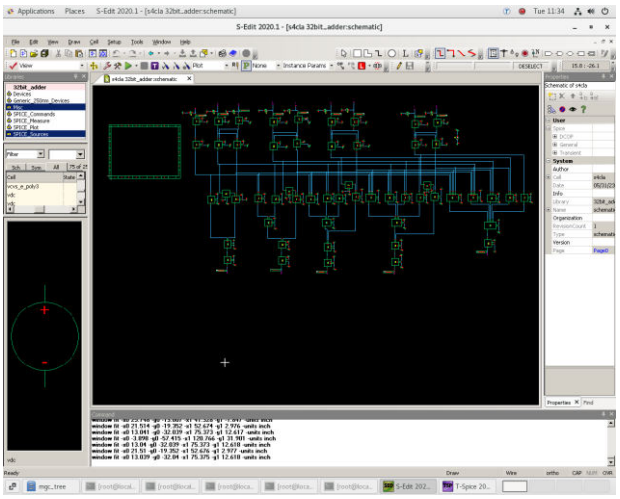

Fig.7: 4-bit CLA Adder Design

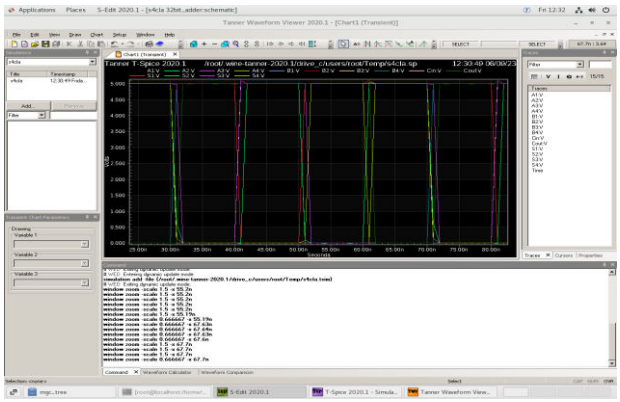

Fig.8: Output Waveform of 4-Bit CLA

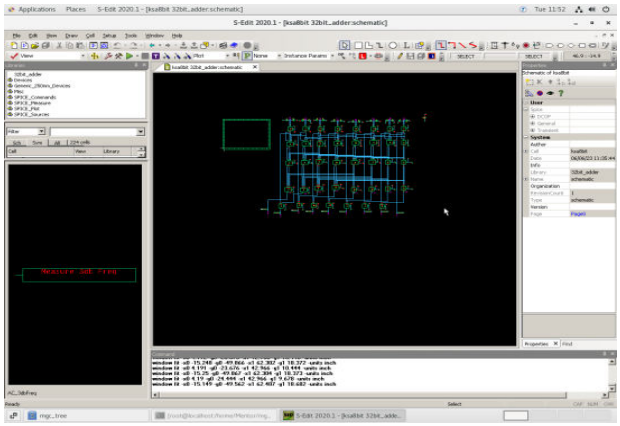

Fig.9: 8-bit KSA Adder Design

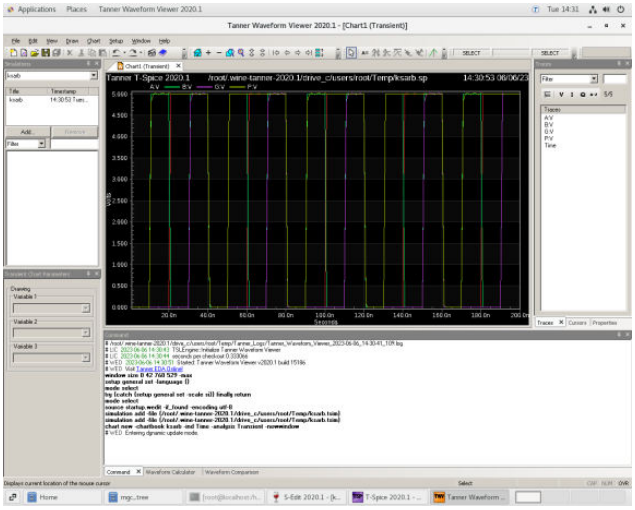

Fig.10: Output Waveform of 8-Bit KSA

VI. APPLICATIONS

The fundamental building blocks of processors and digital systems, ALUs, can use hybrid adders. By combining several adder architectures, such as ripple carry adders (RCAs) and carry look-ahead adders (CLAs), hybrid adders may combine speed and area efficiency.When high-speed arithmetic operations are necessary, such as in scientific simulations, hybrid adders can be utilised to provide calculations that are quicker and more accurate. They can help reduce circuit complexity while accelerating the execution of operations. In DSP applications, complicated mathematical operations like addition and multiplication are routinely employed. By boosting addition operations, which are crucial to many DSP algorithms, hybrid adders can increase the performance of DSP circuits. Compression and filtering are only two of the many mathematical processes utilised in image and video processing techniques. By utilising hybrid adders, these calculations may be performed more quickly and efficiently while consuming less power. As the need for applications utilising artificial intelligence and machine learning grows, neural network

topologies can perform better.

VII. CONCLUSION

Understanding the GDI technique allowed us to build a CLA adder, where the gates, sum generation, and carry generation were all produced using the GDI method. To create an 8-bit CLA, we will first create a 4-bit CLA, link it with the aid of another 4-bit CLA, and then repeat the process. We'll then put together an 8-bit KSA after that. We will build a 16-bit hybrid adder by cascading a hybrid heterogeneous type with an 8-bit CLA. Then, in order to create a 32-bit hybrid adder, we will join two 16-bit hybrid adders.

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