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VLSI Implementation of Reconfigurable Low Power Fir Filter Architecture

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Abstract:

Reconfigurable computing provides the flexibility in arriving at the problem specific architectures which helps in improving the performance due to custom approach. We implement the reconfigurable architecture by exploring the regularity of the adder architectures with minimum additional multiplexers. Here re-configurability has been achieved between the adder variants. The growing design complexity has attracted the designs with reconfigurable fabrics, where adaptable fabrics are utilized to solve the computational problems. Reconfigurable computing provides the flexibility in arriving at the problem specific architectures which helps in improving the performance due to custom approach. In this paper, a flexible reconfigurable architecture with different adder variants like Ripple Carry, Carry Look-ahead, Carry Select and Carry Bypass adders are implemented to form dynamically reconfigurable Hybrid adder architectures. Such hybrid architectures are utilized for the applications where design constraints are only for low power or high performance or the low area or sometimes a balanced design metrics. The design was modelled using Verilog HDL. The proposed architecture enables the designer to perform efficient Design Space Exploration. The design can be made adaptable to any of the reconfigurable processor and a similar improvement can be obtained.

Keywords: Adders, low power VLSI, Verilog, Spartan-III, FPGA.

1. INTRODUCTION

Typical issues for VLSI designers are to reduce the area of the chip and increase its performance for computational applications like video compression, graphics, gaming consoles etc. But the development of portable devices and palm held devices, has forced the designers to optimize the power consumption of the device while still meeting the computational requirements. The wireless devices are also making their way to the consumer electronics market where the power consumption is the key design constraint. Hence the power consumption of the device needs to be addressed to increase the run time of the batteries with minimum requirements on size, durability and weight allocated to it. Absence of low power architectures causes the portable devices to suffer from short battery life or require large battery pack. Increase in power consumption in the chips need expensive packaging and cooling devices, and hence it's a clear advantage of cost to go for low power devices. Addition to the cost, high power consumption leads to the issue of reliability, because the high power consumption increases the temperature and it tends to exacerbate several silicon failure mechanisms. Excessive power consumption limits the integration of more transistors on the single chip or on multichip modules. This is due to the heat generated from power consumption limits the feasible packaging and performance of the VLSI systems. Motivation of reducing power consumption depends on the applications and how much the designer is willing to sacrifice in cost or performance to obtain the low power consumption devices. The design sacrifice the performance for extended battery life of the battery powered devices and suppose if both power and performance are important then the power delay product need to be minimized. Hence in this brief, low power architectures are proposed at comparable performance or negligible performance constraints for the data path components as they are the repeatedly used blocks in any digital circuits. Arithmetic components are responsible for the computations and they are the basic building blocks in intensive computational applications. Among the arithmetic components adders are the essential elements and are used repeatedly in

any computational intense applications. This enabled many research organizations towards the development of low power computational architectures. In this brief, an effort has been attempted to develop low power heterogeneous adder architecture which consume less power and provide delay optimizations.

A. ARCHITECTURES

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of ripple carry adder. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. Now CSLA provides away to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. Therefore the CSLA makes use of Dual RCA's to generate the partial sum and carry by considering input carry Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers. Adder is the essential component in any digital system and many variations are introduced in the carry generation schemes for area, speed and power trade-offs. Hybrid adders were developed in the past to provide area and speed trade-off by utilizing different schemes for sum and carry logic separately. Several homogeneous adders were reconfigured with their bit widths to achieve variable performance and power trade-offs. Architectures reported in have adder variants where larger bit system is partitioned in to smaller bits and reconfigured using additional bits. Such adders provide the selection of the bit widths of the adders and improve efficiency of the design. An effort has been put in to add the extra flexibility into the system where different adder variants of smaller bit widths are incorporated in the larger adder system to address the delay optimization under power constraints or power optimization under delay constraints. Such architectures are called as Heterogeneous adders. In this paper, we propose the low power

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heterogeneous adder architecture to provide power optimization with variable performance.

Limitations of the state of the art reconfigurable architectures,

a) In the regular reconfigurable architectures, static/dedicated adder architectures are utilized and multiplexer selects the required adder variant. This requires more area and consumes more power to achievevariable performance and re-configurabilitybetween the adder variants. b) In the state of the art heterogeneous architecture, the static sub-adder blocks consumes more powerwhile still providing good performance.

In this paper, we address the above limitations: - Low power adder architectures Complex cells wereutilized to build the adder architecture, as they eliminate the interconnect delays between the gates and helps in reducing power. - Elimination of inverters in the critical path reduces the switching power. Complex cells reduce the leakage power of the device.

The proposed concept is suitable for any bit widths and at any level of abstractions where the application needs different operating corners by providing the flavours of differentadder variants in the same design.

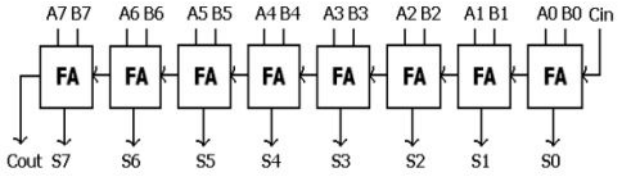

Fig 1: Ripple Carry adder

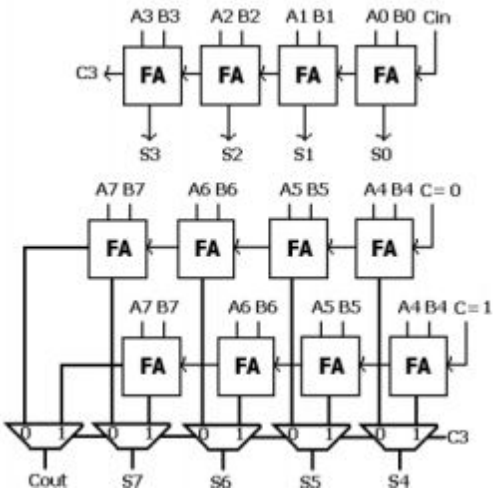

Fig 2: Carry Select adder

II. LITERATURE SURVEY

Literature survey is an important part of the project. It enables assimilation of knowledge required for the project right from the

problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the project.

Zhenyu Liu, Tughrul Arslan, Ahmet T. Erdogan presented a paper entitled as "**A Novel Reconfigurable Low Power Distributed Arithmetic Architecture for Multimedia Applications**", [1]. In this, investigation resulted in novel reconfigurable adders which are the key computation in many digital signal processing applications. 1D DCT is mapped onto the architecture. Compared with some existing ASIC designs, the new architecture achieves good performance in area, speed and power.

K. Anandan, N.S.Yogaananth presented a paper entitled as "**VLSI Implementation of Reconfigurable Low Power Fir Filter Architecture**" [2].The proposed new approaches namely, MSCD for implementing reconfigurable higher order filters for low power. A low power reconfigurable FIR filter architecture is designed to allow efficient trade-off between the filter performance and computation energy. The MSCD architecture results in high speed filters and low power filter implementations. The MSCD provides the flexibility of changing the filter coefficient word lengths dynamically. We have implemented the architectures on Spartan-III XC3S200- PQ-208 FPGA and synthesized. The proposed reconfigurable architectures achieve High speed and low power.

Karthick S, Valarmathy S and **Prabhu E** designed a "**Low Power Heterogeneous Adder**" [3].Low power heterogeneous adder architecture is proposed to enable flexibility to the computing applications and consume less power.Applicationrequirements like low power – same performance, low power– low area, variable performance can be selected.

Nune. Radika and **K. Rajasekhar** presented an improved method for design of "**Hardware Efficient VLSI Adder for Low Power Applications**" [4]. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power.In this paper we proposed new adder in order toreduce the area and power of SQRT CSLAarchitecture. Thereduced number of gates of this work offers the great advantage in the reduction of area and also the total power.The compared results show that the modified CSLA low areaand power as compared to SQRT

CSLA. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere trade off of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

G.O. Jijina, V. Ranganathanand **R. Kalavathy**proposed a concept of analysis of "**Design of Low Power and Area Efficient New Reconfigurable FIR Filter using PSM and Shift and Add Method**"[5].proposed architecturesimplementedby using carry save adder, it offer Low power and area reductions and compared to the best existing reconfigurable FIR filter implementations in the literature and the proposed architectures have been implemented and tested onSpartan-3 xc3s200-5pq208 Field-Programmable Gate Array (FPGA) and synthesized.

J. Pravinadlinand **C. Palaniappan** presented a paper entitled as "**An Area and Delay Efficient CSLA Architecture**" [6]. A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. Regular CSLA suffers from the disadvantage of occupying more chip area. The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by the use of D-latches.

Ms. S. Banupriya and **Mr. G. Lingeswaran** presented a novel "**Area Delay Power Efficient and Implementation of Modified Square-Root Carry Select Adder Architecture**" [7].In this paper, the new 16-bit modified square root carry select adder designed replacement of ripple carry adder by binary to excess one converter (BEC) in existing method. VHSIC Hardware Description Language (VHDL) codes are done by use of Xilinx ISE 8.1i/ Model sim SE 6.5 and simulation waveform and design reports are clearly indicating this design is an efficient to lesser delay and power. Modified SQRT-CSLA design gives

an efficient and fast carry select adder than the existing adder because of this design produced overall delay of 25.209 ns, power of 72 ns and the total logic gates are used in design to 248 gate counts.

N. Durairajaa, J. Joyprincy, and **M. Palanisamy** designed a **"Design of Low Power and Area Efficient Architecture for Reconfigurable FIR Filter"** [8].A low power reconfigurable FIR filter architecture to allow efficient trade-off between the filter performance and computation energy. In the proposed reconfigurable filter, the input data are monitored and the multipliers in the filter are turned off when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Therefore, the proposed reconfigurable filter dynamically changes the filter order to achieve significant power savings with minor degradation in performance.According to the mathematical analysis, power savings and filter performance degradation are represented as strong functions of MCSD window size, the input and coefficient thresholds, and input signal characteristics. Numerical results show that the proposed scheme achieves power savings up to 41.9% with less than around 5.34% of area overhead with very graceful degradation in the filter output. When the CSE method is used in the proposed approach the area overhead can be well reduced.

III. APPLICATIONS

1)Karthick S, Valarmathy S and Prabhu E designed a Low Power Heterogeneous Adder low power heterogeneous adder architecture is proposed to enable flexibility to the computing applications and consume less power.Applicationrequirements like low power – same performance, low power– low area, variable performance can be selected.

2) Nune. Radika and K. Rajasekhar presented an improved method for design of Hardware Efficient VLSI Adderfor Low PowerApplications. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power.

IV.CONCLUSION

This paper provides a brief analysis on different types of adders and their performance analysis. In the proposed

design new modified shared logic architecture is designed for reconfigurable adder applications. The adder architecture will be designed using xilinix software; Design Simulations will be carried out on different adders to obtain the best results. Area and Power analysis is major area of concern.

REFERENCES

[1] Zhenyu Liu, TughrulArslan, Ahmet T. Erdogan "A Novel Reconfigurable Low Power Distributed Arithmetic Architecture for Multimedia Applications"1-4244-0630-7/07/$20.00 ©2007 IEEE.

[2] K.Anandan, N.S.Yogaananth "VLSI Implementation of Reconfigurable Low Power Fir Filter Architecture" International Journal of Innovative Research in Computer and CommunicationEngineering(An ISO 3297: 2007 Certified Organization) Vol.2, Special Issue 1, March 2014

[3] Karthick S, Valarmathy S and Prabhu E "Low Power Heterogeneous Adder" wseas transactions on circuits and systems E-ISSN: 2224-266X Volume 14, 2015

[4] Nune.Radika and K.Rajasekhar"Hardware Efficient VLSI Adder for Low Power Applications"International Journal of Engineering Trends and Technology-Volume3Issue5- 2012ISSN:2231 -5381

[5] G.O. Jijina, V. Ranganathan and R. Kalavathy "Design of Low Power and Area Efficient New Reconfigurable FIR Filter using PSM and Shift and Add Method"Research Journal of Applied Sciences, Engineering and Technology 8(24): 2416-2421 , 2014ISSN: 2040-7459; e-ISSN: 2040-7467

[6] J. Pravinadlin and C. Palaniappanpresented a paper entitled as "An Area and Delay Efficient CSLA Architecture" e-ISSN: 2278-2834, p- ISSN: 2278-8735. Volume 5, Issue 3 (Mar. - Apr. 2013), PP 20-25

[7] Ms. S.Banupriya and Mr.G.Lingeswaran presented a novel "Area Delay Power Efficient and Implementation of Modified Square-Root Carry Select Adder Architecture"

[8] N.Durairajaa, J.Joyprincy, M.Palanisamy "Design of Low Power and Area Efficient Architecture for Reconfigurable FIR Filter" International Journal of Recent Technology and Engineering (IJRTE)ISSN: 2277-3878, Volume-2, Issue-1, March 2013

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