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D.MAHESH KUMAR, K.MANASA, V.ALEKHYA, D.GOUTHAMI, N.LAXMAN

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BORROW SELECT SUBTRACTOR FOR LOW POWER AND AREA EFFICIENCY

D.MAHESH KUMAR[1] K.MANASA[2] V.ALEKHYA[3] D.GOUTHAMI[4] N.LAXMAN[5]

[1]Associate Professor, Department of ECE, Jyothishmathi institute of technology and science,Nustulapur, Karimnagar, TS, India

[2,3,4,5]UG students, Department of ECE, Jyothishmathi institute of technology and science, Ramakrishna Nustulapur, Karimnagar, TS, India

Abstract: Adders and subtractors are important circuit modules in design of processors, which determine the speed of processors. The processing speed of subtraction is limited by the sequential borrow bit propagation from LSB to MSB, which in turn depends on the number of bits of operands (subtrahend and minuend). This paper presents two architectures of modified borrow select subtractor that consume lower power with increased area efficiency. The modifications carried out in the logical flow of subtraction process by using blocks with lower number of logic gates lead to a smaller number of gates, thus resulting in less device count, lower area and lower power dissipation. These proposed designs are implemented using Xilinx ISE 14.7.

Keywords:Borrow Select Subtractor, Low power Subtractor, Area Efficient Subtractor, BSLS, Adder-Subtractor

I. INTRODUCTION

In the past, the main concern for the designers of the VLSI circuits was the area, performance and reliability of the design. But during the recent years, as the demand for the portable devices have gained importance, the main concern for the designers is the power, comparable to the area and speed considerations. The low power VLSI designs are of much interest in the recent years, concerning the demand for long battery life in portable devices and high heat removal in non-portable devices. The problem for low power VLSI design can be broadly classified into two major categories: Analysis and Optimization. Analysis is concerned to be the accurate estimation of the power or energy dissipation during the different designing phase of the circuit. Analysis techniques differ in their accuracy and efficiency. The accuracy of analysis depends on information available to design a particular design. Optimization is the process of generating the best design, given an optimization goal, without violating design specifications.

The interests in low power chips and systems are driven by both business and technical needs. The industry for low power consumer electronic products is booming with a rapidly expanding market. At the same time, current generations of semiconductor processing technologies present more rigorous requirements to the power distribution of digital chips due to increased device density, speed and complexity.

A subtractor is one of the important building blocks in the construction of a binary divider. In modern systems, applications are aimed at battery

operated devices so that power dissipation becomes one of the primary design restrictions. In the past processor speed, circuit speed, area, performance, cost and reliability were of prime significance. Power consumption was of secondary concern. However, in recent years power consumption is being given equal significance. The reason for such a changing trend is attributed probably due to the fast increase in portable computing devices and wireless communication systems which demand high speed calculations and complex functionality with low power consumption. In addition to this high performance processors consume severe power which in turn rises the cost associated with packaging and cooling.Afterwards there is a rise in the power density of VLSI chips thereby disturbing the reliability. It has been found that every 10 degree rise in operating temperature roughly doubles the failure rate of components made up of Silicon due to several Silicon failure mechanisms such as thermal runaway, junction diffusion, electro migration diffusion, electrical parameter shift, package related failure and Silicon interconnect failure. From the environment point of view, the lower the power dissipation of

electronic components, lower will be the heat dissipated in rooms which in turn will have a positive impact on the global environment. Also, lower electricity will be consumed. A full subtractor circuit is one which implements the subtraction between three bits. First bit is minuend, next bit is subtrahend and the third bit is borrowed in input. And the output bits are difference and borrow.

A data processing device is used with peripheral devices having addresses and differing communication response periods. The data processing device includes a digital processor adapted for selecting different ones of the peripheral devices by asserting addresses of each selected peripheral device. Addressable programmable registers hold wait state, which values represents different address ranges. Circuitry responsive to an asserted address to the peripheral devices by the digital processor, generates the number of wait states represented by the value held in one of the addressable programmable registers. This corresponds to the one of the address ranges in which the asserted address occurs, thereby accommodating the differing communication response periods of the peripheral devices. The subtractor circuit analyzes the data with the help of reference signal and allows the signal to the concerned operation without changing its originality. The subtractor circuit is very useful device in signal/data processing, fast multiplier and propagating signals. Low-power IC design has become an especially vibrant area of research and development, resulting in advances in low-power fabrication processes and circuit techniques, dynamically programmable power supplies and power efficient microprocessors. Today, power supply levels are typically kept high, to allow maximum clock speed, and are limited only by hot electron effects.

A VLSI or ULSI circuit according to the present development preferably includes a pair of data bus capable of conducting in parallel number of signals which can be processed simultaneously by the components on the circuit. Signals on the bus are carries in a time-multiplexed manner, each bus having a predetermined number of time slots. Preferably, each component on the chip is connected to one or both of the bus and is assigned a particular time slot for the bus to which it is connected. Subtractor circuit maintains signal level and feed into DSP processor circuit without any losses. To maintain the signal, our proposed circuit compares the input signal with reference signal. Accordingly, it can be readily expanded or contracted in the number of signals which can simultaneously process. The number of components which can be included on the chip is limited only by the number of time slots available on the bus to which it is connected. Since addition of such components involves no custom designed interconnections, but merely extension of the bus, chip die area is conserved while design costs are greatly reduced. Furthermore, the presence of multiplexers at the inputs and/or outputs of elements connected to the bus are unnecessary because the signals thereof are time multiplexed. Additionally, the regularity of the bus structure reduces the criticality in timing paths, race conditions and hangs up states. Regularity in the multiplexing scheme used for the busses further reduces the design efforts. The two input adder/subtractor can be readily accommodated by a chips designer after providing two buses. The dual bus architecture provides ready transfer of data on the chip and off the chip, by appropriate choice of buses, multiplexed timing, as well as for transfer of data between elements on the chip. The bit slice organization of a chip designed, according to the invention, significantly reduces the design effort of the components connected to a bus, since one-bit slice is merely replicated for each conductor of the bus. Ease of expansion along this dimension is achieved at virtually no cost. An overflow detector receives the signal which is generated barrow and difference as an input signal which available from output of subtractor circuit inform of binary numbers. After the overflow detector signal is given to the correction multiplexer circuit for providing the correct signal level according to borrow and difference signal.

The role of arithmetic circuits in all the signal processing units is of paramount importance and in which Adder-Subtractor circuit is indispensable. Adders, Subtractors and multipliers are the essential building blocks of processors. Normally, subtraction is done using adder-subtractor module, which can practically result in slowing down arithmetic operation, since the same hardware has to be used for both addition and subtraction processes using additional control signals. The commonly used Ripple Borrow Subtractor (RBS) used for subtraction of unsigned numbers possesses a simple architecture. However, performance of RBS is limited by borrow propagation time incurred from Least Significant Bit (LSB) to Most Significant Bit (MSB). In other words, the delay of RBS depends on binary word length.

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Borrow Select Subtractor (BSLS) architecture is proposed here to overcome the limitations of existing RBS with multiple RBS circuits. This method generates partial difference and borrow using multiplexers (MUX) and the final difference and borrow is selected. As the BSLS utilizes multiple RBS circuits in it, it is proved normally area inefficient. The conventional method of subtraction for signed numbers uses two's complement method using addition. For addition process, references and use adders. Note that has lower power operational advantage and power delay product (PDP). Here, PDP is the product of power and delay.

The proposed architectures are compared with the conventional two's complement method found in literature, basically employing an added. The adder given in has been considered for comparison of two's complement method against the proposed architectures. For subtraction of signed numbers, a variant of BSLS is proposed. The primary focus is on reducing area and power consumption, which is achieved by using logic blocks with fewer gates occupying less area even while aiming for same logic functionality.

II.LITERATURE SURVEY

T. F. Tay and C. Chang, "A new unified modular adder/subtractor for arbitrary moduli," ***2015 IEEE International Symposium on Circuits and Systems (ISCAS),*** **Lisbon, 2015, pp. 53-56.**

Efficient modular adders and subtractors for arbitrary moduli are key booster of computational speed for high-cardinality Residue Number Systems as they rely on arbitrary moduli set to expand the dynamic range. This paper proposes a new unified modular adder/subtractor that possesses a regular structure for any modulus. Compared to the latest modular adder/subtractor, which works for modulus in the forms of $2^n \pm k$, the proposed design is faster and consumes lower power for n ranging from 4 to 8.

Summary: In this paper, although power is less, more area is required for this circuit

Emam, M. T., &Elsayed, L. A. A. (2010). Reversible Full Adder/Subtractor. 2010 XIth International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD).

This paper proposes two novel designs of Adder/Subtractor using reversible logic gates. The first design is an implementation of two's complement Adder/Subtractor suitable for signed/unsigned numbers. The other design proposes a novel reversible gate that can work singly as a reversible Full Adder/Subtractor unit. The proposed Full Adder/Subtractor is then applied to design a reversible 4-bit ripple Adder/Subtractor.

Summary: In this paper, although power is less, more area is required for this circuit

Khandelwal, R., & Saini, S. (2015). Parity Preserving Adder/Subtractor Using a Novel Reversible Gate. 2015 Fifth International Conference on Communication Systems and Network Technologies.)

Modern VLSI circuit design is governed by low power consumption requirements of ICs. Reversible logic has received great importance because of no information bit loss during computation which results in low power dissipation. Moreover, there is a need to convert the reversible circuits into fault tolerant reversible circuits to detect the occurrence of errors. Parity preserving property can be used for this. A new 5*5 parity preserving reversible gate is proposed in this paper, named as P2RG. The most significant aspect of this work is that it can work both as a full adder and a full subtractor by using one P2RG and Fredkin gate only. Proposed design is better in terms of gate count, garbage outputs, constant inputs and area than the existing similitudes. Thus, this paper provides the initial threshold to design more complex systems which will be able to execute more complicated operations using parity preserving reversible logic.

Summary: In this paper, although low power is achieved transistor count is more.

S. Veeramachaneni and M. B. Srinivas, "Floating point adder/subtractor units realization by efficient arithmetic circuits," ***2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME),*** **Glasgow, 2015, pp. 244-246**

Floating point adder/subtractor units like fused floating point adder, triple path floating point adder, etc., involve exponent comparison/subtraction, mantissa addition/subtraction and incrementing values while rounding as basic operations. To realize these operations, efficient arithmetic units like comparators, adders, subtractors, and incrementers are vital. In this paper an efficient design of an adder and a design methodology for 2's complement block is proposed which helps in design of floating point units.

Summary: More power is required for floating point subtractor

Shabeerkhan "A Novel DBB (Difference Based Borrow) Subtractor for Low Power Applications",

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2018, International Journal of ChemTech Research.

Power is one of the most significant design bound after speed, in integrated circuit. One of the basic essential component in such circuit is adder and subtractor. In order to optimize such circuits there is need of designing proficient and low power fundamental blocks. We present a new design of the full subtractor based on difference based borrow calculation. The proposed full subtractor is optimized in terms of delay, cost and power. The proposed reversible full subtractor is shown to be better than the existing design. The proposed subtractors proposed in this work will be useful in a number of digital signal processing applications.

D. Verma, M. Ramachandran and S. Prince, "Performance analysis for different data-rates of proposed all-optical half-adder and full-adder design," ***2016 International Conference on Communication and Signal Processing (ICCSP),*** **Melmaruvathur, 2016.**

By using optical communication large amount of data can be sent over large distances with minimum error. The transparency feature of all-optical communication overcomes the bottleneck of electronics and opto-electronics at network nodes. To fulfill the day by day increasing data rate demands the optical telecommunication networks will require all-optical add drop function, logic and arithmetic processing. All-optical logic gates are the main element to implement the all optical combinational logic circuits such as: adders, subtractors, multipliers, multiplexers, demultiplexers and comparators. All optical full-adder is the primary elementary unit for the realization of All-Optical multifunction Arithmetic Logic Unit (ALU) which performs the arithmetic as well as logic operations. This paper is mainly proposed to design the all-optical Half-Adder and Full-Adder circuit using logic gates configurations based on SOA-MZI.

III.PROPOSED METHOD

The proposed architecture replaces the second n-bit RBS and BEC-1 of BSLS using (n+1)-bit Binary-Less-One (BLO) logic in all groups. It uses Binary-Less-One (BLO) logic as shown in Fig.1 for 3-bit BLO logic. Table II shows the functional table. The 3-bit BLO has been designed using Boolean expressions (1), (2) and (3). 4-bit BLO, 5-bit and 6bit BLO structures can all be realized by using their respective Boolean expression forms

$$X0 = \sim B0 \quad (1)$$

$$X1 = B1 \text{ xnor } B0 \quad (2)$$

$$X2 = B2 \text{ xor } \sim (B0 + B1) \quad (3)$$

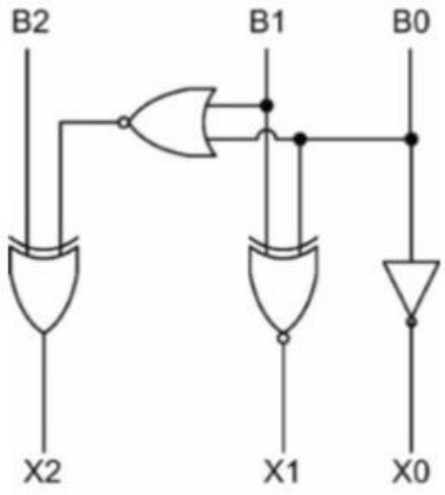

Fig. 1. 3-bit Binary-Less-One (BLO)

The proposed Binary-Less-One (BLO) logic accomplishes the same operation of generating the difference and borrow assuming that the Bin from the previous stage is 1. This is analogous to the adder in but the internal components are different. It takes the difference and borrow when the Bin is 0 as input and subtracting one from the received difference and borrow. The output of the BLO logic is the same as that of difference and borrow when Bin is 1. Fig. 2 shows the architecture of the modified Borrow Select Subtractor circuit configured using Binary-Less-One logic (BSLS-BLO). The Binary-Less-One logic is employed in all groups except the group 1 to compute difference and borrow bits. The partial difference and borrow bits obtained from first n-bit RBS, considering Bin=0 and Binary-Less-One (BLO) considered as Bin=1 are given as input bits to multiplexer, which selects the actual difference and borrow based on Bin generated from previous group. The first group has only one two-bit RBS, while, each of the functional groups except the first consists of one n-bit RBS, (n+1)-bit BLO and a (2n+2):(n+1) multiplexer.

A full subtractor normally requires 2 numbers each of XOR, NOT and AND gates and one OR gate. A half subtractor can be realized using one each of XOR, NOT and AND gates. To realise 2:1 MUX, one NOT gate, 2 AND gates and one OR gate are required. First 3-bit processing in RBS requires

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one half subtractor and 2 full subtractors. Thus, the first 3-bit RBS requires 5 XOR gates, 5 NOT gates, 5 AND gates and 2 OR gates. The 4-bit BLO is realized using 2 each of XOR, NOT and NOR gates and one XNOR gate. 8:4 MUX selects actual difference and borrow bits, and this comprises of four 2:1 multiplexers, containing 4 NOT, 8 AND and 4 OR gates.

Total gate count required to implement the group 3 structure in BSLS-BLO is thus the sum of counts, namely, 1) first 3-bit RBS, 2) 4-bit BLO and 3) 8:4 MUX. Therefore, the total number of gates employed to implement group 3 of BSLS-BLO is 7 XOR, one XNOR, 11 NOT, 13 AND, 6 OR and 2 NOR gates. Totally 40 gates are needed for group 3 in BSLS-BLO.

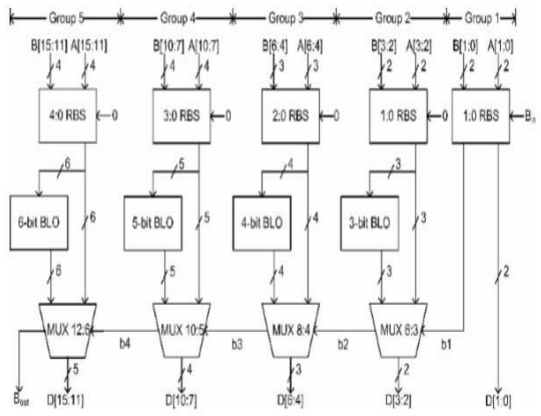

Fig. 2. Modified Borrow Select Subtractor using Binary-Less-One Logic

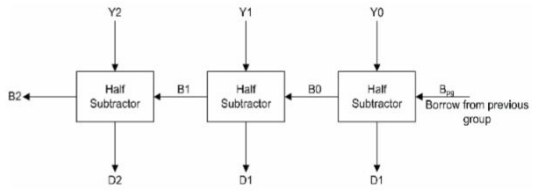

Fig. 3 3-bit Ripple Borrow Half Subtractor (RBHS)

A second variant of the BSLS has been proposed in this Section, which replaces the second n-bit RBS and BEC-1 of BSLS or the n-bit BLO in BSLS-BLO using n-bit ripple borrow half subtractor (RBHS) in all groups. It employs Ripple Borrow Half Subtractor (RBHS) as shown in Fig.3, as depicted for a 3-bit ripple borrow half subtractor (RBHS). It is analogous to the adder in [10]. The n-bit ripple borrow half subtractor takes the input from n-bit RBS with Bin as 0 for corresponding group. Depending on the borrow from previous group (Bpg), operation of RBHS varies. If borrow is 0, then the received input is passed as it is to output. Else, (Bpg = 1), output is produced by subtracting one from input. This is achieved by use of half subtractors. Table IV shows functional table of 3-bit RBHS. An n-bit RBHS comprises of n half subtractors. The input Y to each half subtractor is from n-bit RBS with Bin=0. The other input to the half subtractor is borrow from previous group or from previous half subtractor. The borrow output (Bout) from nth half subtractor is the final borrow out of the n-bit RBHS.

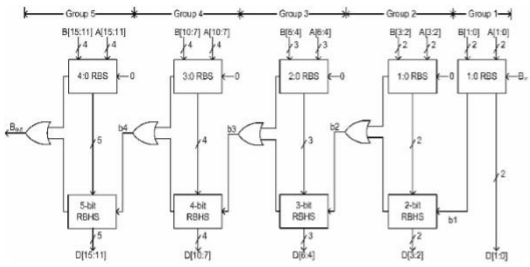

Fig. 4 Modified Borrow Select Subtractor using Ripple Borrow Half Subtractor

Fig.4 shows the structure of the modified borrow select subtractor circuit using ripple borrow half subtractor (BSLSRBHS). Ripple borrow half subtractor is used in all groups except group 1 to compute difference and borrow bits. The partial difference and borrow bits obtained from first n-bit RBS, considering Bin=0 and the partial difference and borrow is given as input to the n-bit RBHS. Based on the borrow bit Bin generated from the previous group, the difference and borrow bit values have been computed. The borrow-out bit Bout from both n-bit RBS and n-bit RBHS are given as input to the OR gate. The output of the OR gate is the borrow-out bit Bout for the current group and borrow-in for the succeeding group. In this architecture, the (2n+2) :(n+1) multiplexer in each group has been replaced with a OR gate. This results in reduction of number of gates. Each functional group except first group has one n-bit RBS, n-bit RBHS and an OR gate. The first group has only one two-bit RBS

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IV.RESULTS

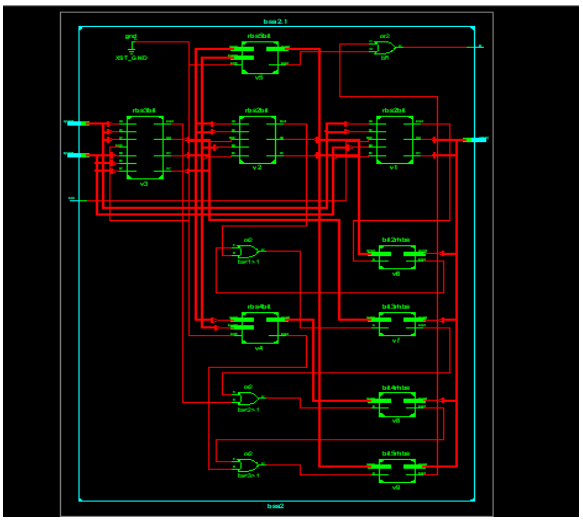

Fig.5 RTL schematic of proposed modified borrow select subtractor using RHBS

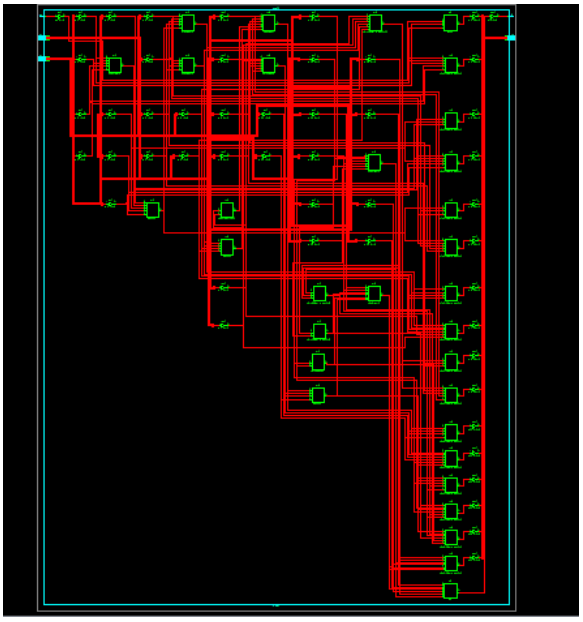

Fig.6 Technology schematic of proposed modified borrow select subtractor using RHBS

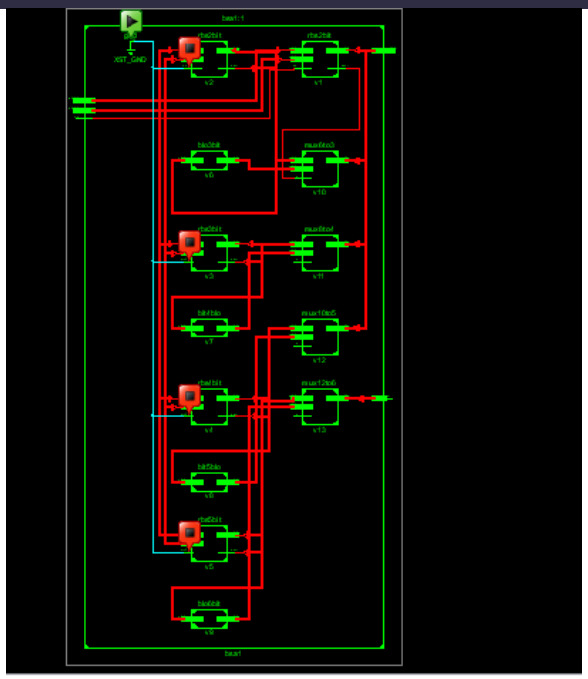

Fig.7 RTL schematic of proposed modified borrow select subtractor using BLO

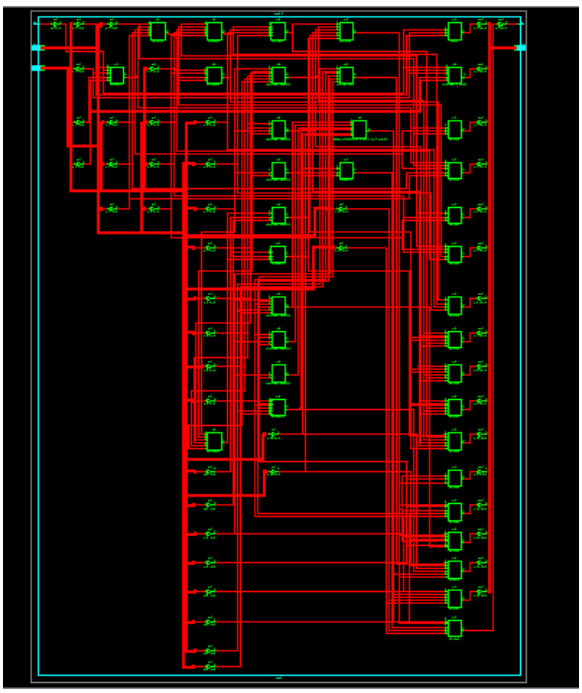

Fig.8Technology schematic of proposed modified borrow select subtractor using BLO

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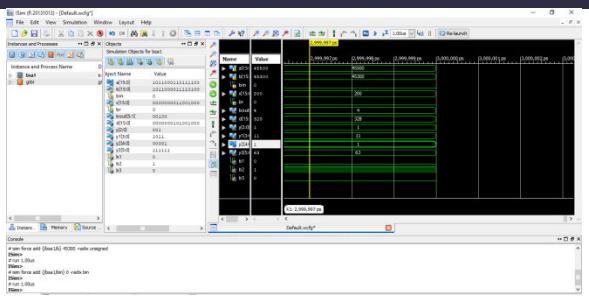

Fig.9 Simulation result of proposed modified borrow select subtractor using RHBS

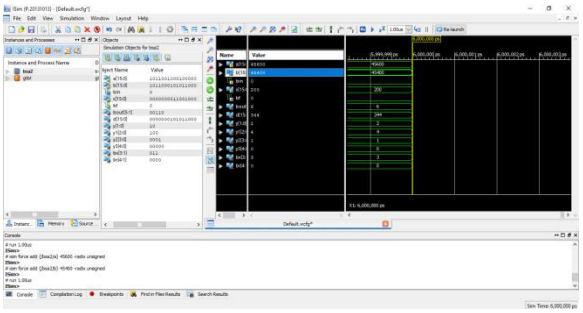

Fig.10 Simulation result of proposed modified borrow select subtractor using BLO

Evaluation table for area, delay and power:

Evaluation table for area, delay and power BSA Table-1

	Area	Delay(ns)	Power(w)
Proposed BSA 1	39	4.49	0.082
Proposed BSA 2	32	5.53	0.082

CONCLUSION:

This paper presents modified borrow select subtractor using BLO and modified borrow select subtractor using RHBS. The number of gates employed is less in both the modified architectures that the counterpart architectures. This design approach also leads to reduced number of transistors utilized, lower area and reduced power consumption. Simulation results show that the proposed modified borrow select adder using RHBS occupies less area and power.

FUTURE SCOPE:

Since Mostly adders and subtractors are used in Dsp applications which are error tolerant. By applying the concept of approximation we can achieve better results in terms of area, power and delay.

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