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Interfacing of Multi Input-Output Card With ARM9 Processor

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Abstract- In the past, the high performance real time control applications have employed 8 and 16 bit microcomputers together with interrupt handler chips, programmable timer chips, ROM (Read Only Memory) and RAM (Random Access Memory) chips to achieve what can now be achieved in a single state-of-art Microcontrollers chip. Even for those real time control applications for which the resources of a single chipper are not adequate, such a chip slice generally offers the optional design approach. Its on-chip resources provide an integrated approach to a variety of real time tasks. By operating the chip in an expanded mode, we not only gain the on-chip features, but we can also augment those features as we see fit.With all the above said advantages, in many Industrial and Scientific fields we are vastly using the microcontrollers instead of microprocessors, because processors are not suitable for controlling purposes. Now days, for all controlling purposes microcontrollers are replacing the processors

Index Terms- Read Only Memory, Random Access Memory, ARM architecture, RISC

I. INTRODUCTION

The ARM architecture is a 32-bit RISC processor architecture developed by ARM Limited that is widely used in a number of embedded designs. Because of their power saving features, ARM CPUs are dominant in the mobile electronics market, where low power consumption is a critical design goal. The ARM architecture, which provides the basis for the company's technology leadership, is the most widely used 16/32-bit embedded RISC solution in the world. Latest reports show that ARM's market share of the embedded RISC microprocessor market is approximately 75 percent and to date, ARM Partners have shipped more than 2.5 billion ARM core-based microprocessors. It has excelled because it is an open architecture that provides unparalleled levels of compatibility and design reusability, combined with superior performance. The industry-proven Thumb instruction set is an extension to the ARM architecture. While incorporating the same design characteristics, the Thumb instruction set requires only a 16-bit wide system data bus, thereby using less power, offering a smaller footprint, and reducing overall system cost. The Thumb instruction set features a subset of the most commonly used 32-bit ARM instructions, which have been compressed into 16-bit wide codes to provide excellent code densities. On execution, these 16-bit instructions are decompressed transparently and in real-time to full 32-bit instructions – without performance loss. Designers can combine ARM code with Thumb code for maximum flexibility in their applications. ARM has enhanced many cores by extending the instruction set to include 16-bit and 32-bit arithmetic capabilities. These DSP-enhanced cores enable products that require a mixture of DSP and control functionality to be implemented with a single core, saving the time, cost and complexity of implementing a dual-core design. Typical applications include mass storage devices, such as hard disk drives, and automotive satellite controllers. ARM offers the industry's broadest range of 16/32-bit embedded RISC cores that are grouped into a range of families: the ARM7, the ARM9, the ARM9E, the ARM10, ARM11, SecurCore and Cortex families of microprocessor cores. Each product family consists of high-performance, energy-efficient designs built to handle the performance demands of today's increasingly complex electronics applications.The Net Silicon NS9360 is a single chip 0.13µm CMOS network-attached processor. This chapter provides an overview of the NS9360, which is based on the standard architecture in the NET+ARM family of devices. The NS9360 uses an ARM926EJ-S core as its CPU, with MMU, DSP extensions, Jazelle Java accelerator, and 8 kB of instruction cache and 4 kB of data cache in Harvard architecture. The NS9360 runs up to 180 MHz, with a 90 MHz system and memory bus and 45 MHz peripheral bus. The NS9360 offers an extensive set of I/O interfaces and Ethernet high-speed performance and processing capacity. The NS9360 is designed specifically for use in high-performance intelligent networked devices and Internet appliances including high-performance, low-latency remote I/O, intelligent networked information displays, and streaming and surveillance cameras.

The processor has in-built modules for Ethernet, i2c, SPI, USB, clock generator, timers and finally counters. The processor is

built up as an integrated device with all these specified modules as each individual block. Each block has a prescribed function and will act accordingly when enabled.Flash boot can be done from 8-bit, 16-bit, or 32-bit ROM or Flash. Serial EEPROM boot is supported by NS9360 hardware. A configuration header in the EEPROM specifies total number of words to be fetched from EEPROM, as well as a system memory configuration and a memory controller configuration. The boot engine configures the memory controller and system memory, fetches data from low cost serial EEPROM, and writes the data to external system memory, holding the CPU in reset. Master reset using an external reset pin resets NS9360. Only the bus error status registers retain their values; software read resets these error status registers. The input reset pin can be driven by a system reset circuit or a simple power-on reset circuit. Reset can be done either using the hardware or software reset. Hardware reset duration is 4ms for PLL to stabilize where as software reset duration depends on speed. The minimum reset pulse width is 10 clock cycles.The PLL parameters are initialized on power up reset, and can be changed by software. If changed by software, the system resets automatically after the PLL stabilizes (approximately 4 ms). The system clock provides clocks for CPU, AHB system bus, peripheral Bus, LCD, timers, memory controller, and Bus modules (serial modules and 1284 parallel port). The Ethernet MAC uses external clocks from a MII PHY or a RMII PHY. LCD controller, serial modules (UART, SPI), and the 1284 port optionally can use external clock signals.The critical timing requirement is the rise and fall time of the input. If the rise time is too slow for the reset input, the hardware strapping options may be registered incorrectly. If the rise time of a positive-edge-triggered external interrupt is too slow, then an interrupt may be detected on both the rising and falling edge of the input signal. A maximum rise and fall time must be met to ensure that reset and edge sensitive inputs are handled correctly. With Net Silicon processors, the maximum is 500 nanoseconds. If an external device driving the reset or edge sensitive input on a NetSilicon processor cannot meet the 500ns maximum rise and fall time requirement, the signal must be buffered with a Schmitt trigger device.

II. Existing Work or Literature Survey

It's the foremost preliminary step for proceeding with any research work writing. While doing this go through a complete thought process of your Journal subject and research for its viability. The ARM926EJ-S processor supports the 32-bit ARM and 16-bit Thumb instructions sets, allowing you to tradeoff between high performance and high code density. The processor includes features for efficient execution of Java byte codes, providing Java performance. The ARM926EJ-S supports the ARM debug architecture, and includes logic to assist in both hardware and software debug. The processor has a Harvard-cached architecture and provides a complete high-performance processor subsystem. The processor executes three instruction sets: ARM instruction set The ARM instruction set allows a program to achieve maximum performance with the minimum number of instructions. The majority of instructions are executed in a single cycle. Thumb instruction set The Thumb instruction set is simpler than the ARM instruction set, and offers increased code density for code that does not require maximum performance. Code can switch between ARM and Thumb instruction sets on any procedure call. Java instruction set In Java state, the processor core executes a majority of Java byte codes naturally. Byte codes are decoded in two states, compared to a single decode stage when in ARM/Thumb mode.A hardware-based system for managing multiple input/output devices is the multiple I/O card. A multiple I/O card is used to significantly reduce the time overload, that is caused when many cards are connected to one CPU for all its activities. Another distinct feature of a multiple I/O card is the low power consumption.The part contains four on-chip registers which can be accessed by via the serial port on the part. The first of these is a Communications Register that decides whether the next operation is a read or writes operation and also decides which register the read or write operation accesses. All communications to the part must start with a write operation to the Communications Register. After power on or RESET, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a write or a read operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. A read operation from any register on the part (including the Communications Register itself and the output data register) starts with a write operation to the Communications Register followed by a read operation from the selected register. The Communication Register also controls the standby mode and the operating gain of the part. The DRDY status is also available by reading from the Communications Register. The second register is a Setup Register that determines calibration modes, filter selection and bipolar/unipolar operation. The third register is the Data Register from which the output data from the part is accessed. The final register is a Test Register that is accessed when testing the device.The Communications Register is an eight-bit register from which data can either be read or to which data can be written. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation and to which register this operation takes place. Once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register.

The part contains a Test Register which is used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-On or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising RESET will exit the part from the mode. An

alternative scheme for getting the part out of one of its test modes is to reset the interface by writing 32 successive 1s to the part and then load all 0s to the Test Register. The Data Register on the part is a read-only 16-bit register which contains the most up-to-date conversion result from the AD7715. If the Communications Register data sets up the part for a write operation to this register, a write operation must actually take place to return the part to where it is expecting a write operation to the Communications Register (the default state of the interface). However, the 16 bits of data written to the part will be ignored by the AD7715.

The key feature of the converters that employ sigma-delta conversion technique is that they are the only low cost conversion method which provides both high dynamic range and flexibility in converting low bandwidth input signals.Digital Converter (ADC). The input signal X comes into the modulator via a summing junction. It then passes through the integrator which feeds a comparator that acts as a one-bit quantizer. The comparator output is fed back to the input summing junction via a one-bit digital-to analog converter (DAC), and it also passes through the digital filter and emerges at the output of the converter. The feedback loop forces the average of the signal W to be equal to the input signal X.The input signal to the analog input is continuously sampled at a rate determined by the frequency of the master clock, MCLKIN, and the selected gain. A charge-balancing A/D Converter (sigma-delta modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A sinc digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate.The AD7715 contains three on-chip registers which the user accesses via the serial interface. Communication with any of these registers is initiated by writing to the Communications Register first. Figure A outlines a flow diagram of the sequence which is used to configure all registers after a power-up or reset. The flowchart also shows twodifferent read options—the first where the DRDY pin is polled to determine when an update of the data register has taken place, the second where the DRDY bit of the Communications Register is interrogated to see if a data register update has taken place. Also included in the flowing diagram is a series of words which should be written to the registers for a particular set of operating conditions. These conditions are gain of 1, no filter sync, bipolar mode, buffer off, clock of 2.4576MHz and an output rate of 60 Hz.

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III. WRITE DOWN YOUR STUDIES AND FINDINGS

The AD420 is a complete digital to current loop output converter, designed to meet the needs of the industrial control market. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop signals in a compact 24-lead SOIC or PDIP package. The output current range can be programmed to 4 mA–20 mA, 0 mA–20 mA or an over range function of 0 mA–24 mA. The AD420 can alternatively provide a voltage output from a separate pin that can be configured to provide 0 V–5 V, 0 V–10 V, ±5 V or ±10 V with the addition of a single external buffer amplifier. It can be used in three-wire or asynchronous mode and a serial-out pin is provided to allow daisy chaining of multiple DACs on the current loop side of the isolation barrier. The AD420 uses sigma-delta (SD) DAC technology to achieve 16-bit monotonic at very low cost. Full-scale settling to 0.1% occurs within 3 ms.The only external components that are required (in addition to normal transient protection circuitry) are two low cost capacitors which are used in the DAC output filter.

Pin #	Symbol	Function
1, 12, 13, 24	NC	No Connection. No internal connections inside device.
2	V_{LL}	Auxiliary buffered +4.5 V digital logic voltage. This pin is the internal supply voltage for the digital circuitry and can be used as a termination for pull-up resistors. An external +5 V power supply can be connected to V_{LL}. It will override this buffered voltage, thus reducing the internal power dissipation. The V_{LL} pin should be decoupled to GND with a 0.1 µF capacitor. See Power Supplies and Decoupling section.
3	FAULT DETECT	FAULT DETECT, connected to a pull-up resistor, is asserted low when the output current does not match the DAC's programmed value, for example, in case the current loop is broken.
4 5	RANGE SELECT 2 RANGE SELECT 1	Selects the converter's output operating range. One output voltage range and three output current ranges are available.
6	CLEAR	Valid V_{IH} will unconditionally force the output to go to the minimum of its programmed range. After CLEAR is removed the DAC output will remain at this value. The data in the input register is unaffected.
7	LATCH	In the three-wire interface mode a rising edge parallel loads the serial input register data into the DAC. To use the asynchronous mode connect LATCH through a current limiting resistor to V_{CC}.
8	CLOCK	Data Clock Input. The clock period is equal to the input data bit rate in the three-wire interface mode and is 16 times the bit rate in asynchronous mode.
9	DATA IN	Serial Data Input.
10	DATA OUT	Serial Data Output. In the three-wire interface mode, this output can be used for daisy-chaining multiple AD420s. In the asynchronous mode a positive pulse will indicate a framing error after the stop-bit is received.
11	GND	Ground (Common).
14	REF OUT	+5 V Reference Output.
15	REF IN	Reference Input.
16	OFFSET TRIM	Offset Adjust.
17	V_{OUT}	Voltage Output.
18	I_{OUT}	Current Output.
19	BOOST	Connect to an external transistor to reduce the power dissipated in the AD420 output transistor, if desired.
20 21	CAP 1 CAP 2	These pins are used for internal filtering. Connect capacitors between each of these pins and V_{CC}. Refer to the description of current output operation.
22	NC	No Connection. Do not connect anything to this pin.
23	V_{CC}	Power Supply Input. The V_{CC} pin should always be decoupled to GND with a 0.1 µF capacitor. See Power Supplies and Decoupling section.

The AD420 uses sigma-delta (SD) architecture to carry out the digital-to-analog conversion. This architecture is particularly well suited for the relatively low bandwidth requirements of the industrial control environment because of its inherent monotonicity at high resolution. In the AD420 a second order modulator is used to keep complexity and die size to a minimum. The single bit stream from the modulator controls a switched current source that is then filtered by two, continuous time resistor-capacitor sections. The capacitors are the only external components that have to be added for standard current-out operation. The filtered current is amplified and mirrored to the supply rail so that the application simply sees a 4 mA–20 mA, 0 mA–20 mA, or 0 mA–24 mA current source output with respect to ground.The P89C668 device is a Single-Chip 8-Bit Microcontroller manufactured in advanced CMOS process and is a derivative of the 80C51 microcontroller family. The device has the same instruction set as the 80C51. It contains a non-volatile 64 kbytes Flash program memory that is both parallel programmable and serial In-System Programmable. In-System Programming allows devices to alter their own program memory, in the actual end product, under software control. This opens up a range of applications that can include the ability to field update the application firmware. A default serial loader (boot loader) program in ROM allows serial. In-System programming of the Flash memory without the need for a loader in the Flash code. User programs may erase and reprogram the Flash memory at will through the use of standard routines contained in ROM. The device is also equipped four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. The added features of the P89C668 makes it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities.The P89C668 contains 64 KB of Flash program memory. This memory is organized as separate blocks. The first two blocks are 8 KB in size, filling the program memory space from address 0 through 3FFF hex. The final three blocks are 16 KB in size and occupy addresses from 4000 through FFFF hex. 3.4.3 TIMER 2 OPERATION Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2* in the special function register T2CON. Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON.In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1-to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively.The 8255 Programmable Peripheral Interface (PPI) is a very popular and versatile input output chip that is easily configured to function in several different configurations. This chip allows you to do both digital input and output (DIO).

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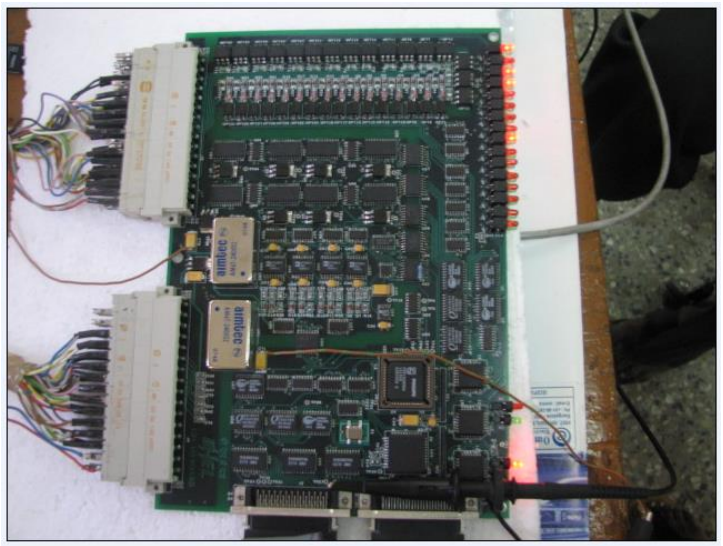
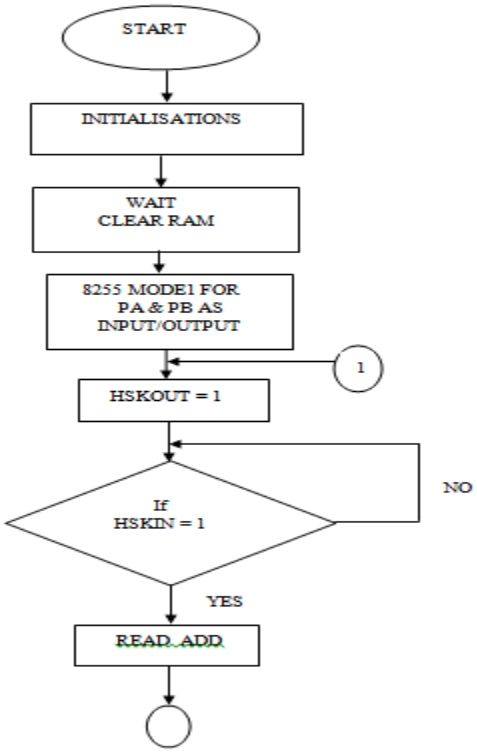
INTERFACING: Two devices are said to be properly interfaced if they can communicate efficiently with one another. Here, the multiple I/O card and the ARM Processor are interfaced only if data is said to flow between them in both the directions which means that if we can perform read and write operations on the microcontroller of the multiple I/O card and the ARM Processor then, we are said to have interfaced both the devices.

BUS INTERFACING For the interfacing of the NS9360 with the multiple I/O card, the GPIO pins of the ARM processor are used. Of the available 73 pins, 48 are being made use of – 16 pins for These 3-State octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements. The device allows data transmission from the A Bus to the B Bus or from the B Bus to the A Bus depending upon the logic level at the direction control (DIR) input. The enable input (G) can be used to disable the device so that the buses are effectively isolated.It is an octal D-Type tristate transparent Latch. The eight latches of the 74LS373 are transparent D type latches meaning that while the enable is high the Q outputs will follow the data inputs. When the enable is taken low the output will be latched at the level of the data that was set up. The eight flip-flops are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs. A buffered output control input can be used to place the eight outputs in either high or low logic level or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.The LSTTL/MSI SN74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.The 8255 Programmable Peripheral Interface (PPI) is a very popular and versatile input output chip that is easily configured to function in several different configurations. This chip allows you to do both digital input and output (DIO).

address, 16 pins for data and the other 16 pins are used as the I/O pins.In the case of SPI, the data is sent bit by bit which involves time overhead and for every bit sent, the buffers are to be checked if they are empty. Thus, the time consumption is much greater than bus interfacing. For bus interfacing, before all the bits are transmitted or received, the processor checks for handshake signals. This reduces the time required from transmission to a great extent.

IV. RESULTS AND DISCUSSION





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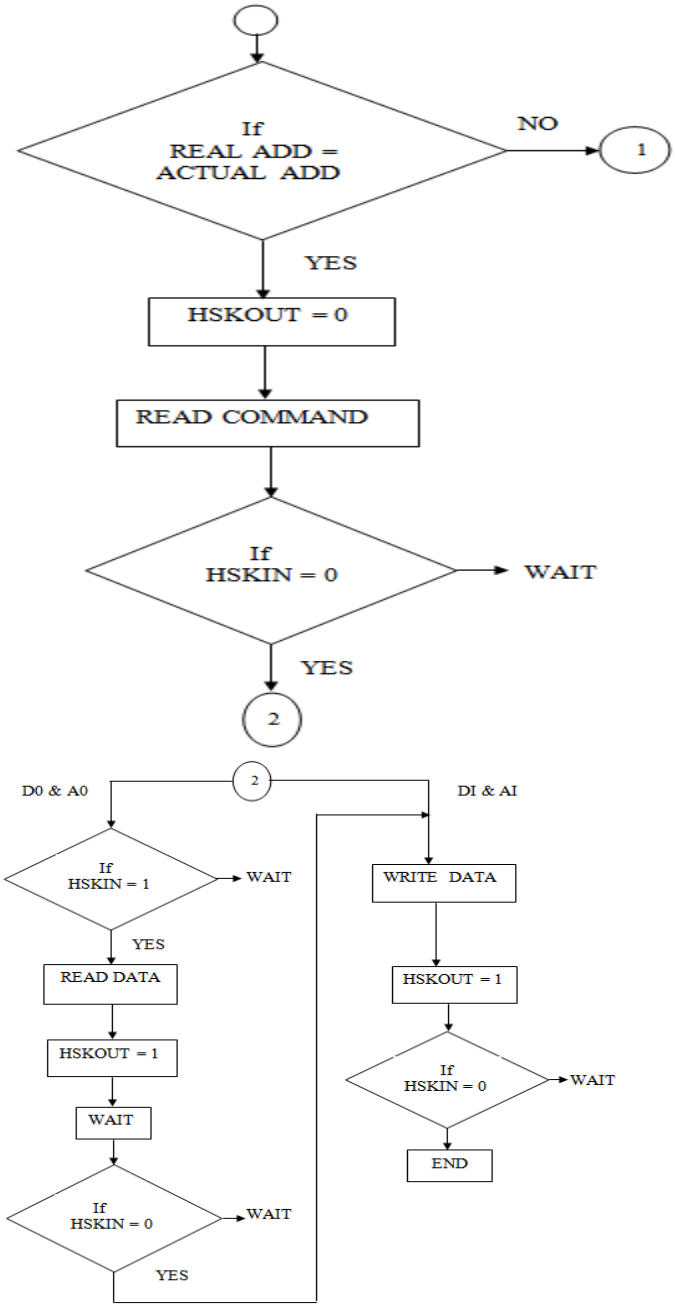

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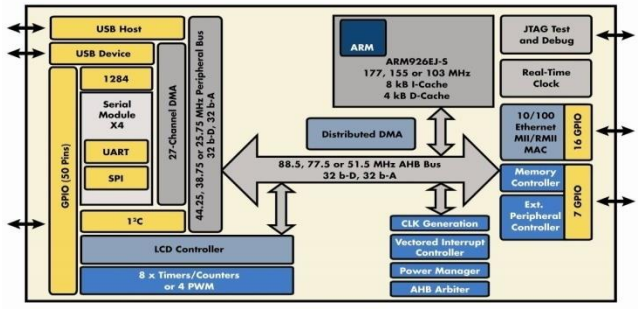

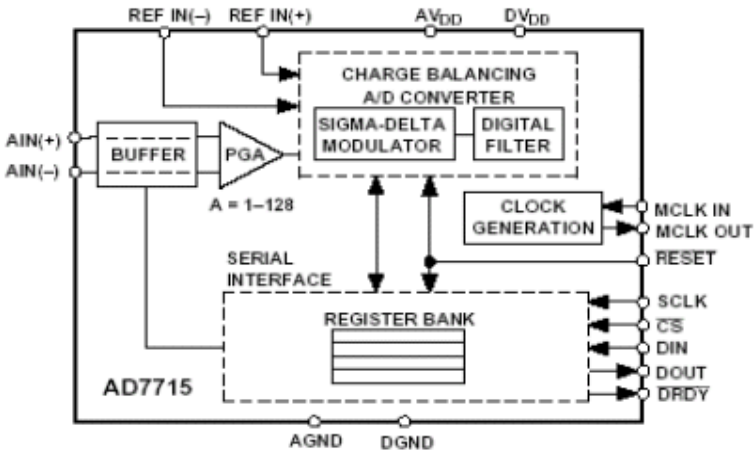

V. CONCLUSION

The controller is efficiently minimizing the error and the input is corrected to required voltage.This is particularly useful in fields where accuracy and resolution are very important. This controller is used in various power plants and industrial applications like Weigh scales, Industrial or process control ARM Processor, being the least power consuming and the most economical processor, may invariably become the indispensable part of the future generation computers.

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