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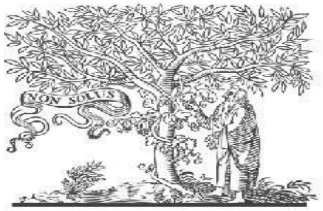

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Paper Authors **P. Kiran kumar, K. Prerthi, M. Ramya, D. Monuika, A. Nikil**

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HIGH PERFORMANCE 10-T XOR XNOR CELL USING HIGH SPEED HYBRID LOGIC FULL ADDER

P. Kiran kumar[1], K. Prerthi[2], M. Ramya[3], D. Monuika[4], A. Nikil[5]
[1]Assistant Professor, Dept. of Electronic & communication Engineering, Balaji Institute of technology and science, Warangal, Telangana, India

[2,3,4,5]UG Student, Dept. of Electronic & communication Engineering, Balaji Institute of Technology and Science, Warangal, Telangana, India

Abstract:

Full adder (FA) circuits are frequently built using hybrid logic techniques. How effectively the XOR-XNOR circuit functions has a significant impact on the hybrid FA's delay, power, and driving characteristics. The 10-T high-speed, low-power XOR-XNOR circuit suggested in this article provides simultaneous full swing outputs and improved delay performance. Its performance is assessed by simulating the recommended circuit using 90-nm CMOS technology in tanner tool. The power delay product (PDP), as compared to the current XOR-XNOR modules, is decreased by at least 7.5 percent in the proposed circuit. The FA designs described in this article make use of readily accessible sum and carry modules and the required XOR-XNOR circuit. The recommended FAs provide returns between 2% to 28.13 percent.

Keyword: Hybrid full adder (FA), XOR-XNOR circuit, cascaded full adder (CFA)

I. Introduction:

Mobile phones, laptops, and personal digital assistants (PDAs) are a few examples of portable electronic gadgets that are increasingly necessary for daily living. These electrical systems' designers strive to create circuits that are small, quick, and energy-efficient. These electrical systems are mostly made up of arithmetic circuits. Most arithmetic circuits require an adder as a key component, including. The power consumed by these arithmetic circuits in high-performance microprocessors' data channels is around one-third. The total system performance thus rises dramatically when the adders' performance is increased. Several static CMOS logic types have been developed in order to construct a full adder (FA) circuit. These logical layouts may be divided into two groups: traditional design styles and hybrid design styles. The FA employs MOS transistors and is constructed as a single module. This method is shown by the complementary CMOS (C-CMOS) FA. In this design, the pull-up and pull-down networks of an FA are realised using 28 transistors. It offers full-swing outputs and resistance to voltage and transistor size scaling Each input is coupled to a gate that has a PMOS and a NMOS transistor, at the very least. The major disadvantage of this circuit is high input capacitance, which slows down the adder's speed Complementary pass-transistor logic (CPL) FA is a further illustration of the conventional technique The cross-coupled PMOS structure, static inverter at the output, and high-speed differential stage gives this structure excellent driving capabilities, full swing output, and high speed. The circuit's excessive power dissipation is caused by the circuit's many internal nodes, though. Additionally, due to the asymmetrical transistor configuration, the circuit architecture is not consistent. FA can also be produced the conventional way, with pass transistors. The pass transistors, however, have a built-in issue with threshold voltage drop. Full-swing logic "1" and "0" are not produced at the output when logic "1" and logic "0," respectively, are transmitted using NMOS and PMOS. A transmission gate (TG)-based solution has been created to address this problem. In this configuration, complementary control signals are used to drive parallel connections between NMOS and PMOS

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transistors. To offer full-swing outputs, this PMOS and NMOS are simultaneously switched on and give routes to both logics (logic "1" and "0"). Although the TG-based adder uses less power, its driving performance is subpar. This circuit's performance might be improved.

II . BLOCK DIAGRAM

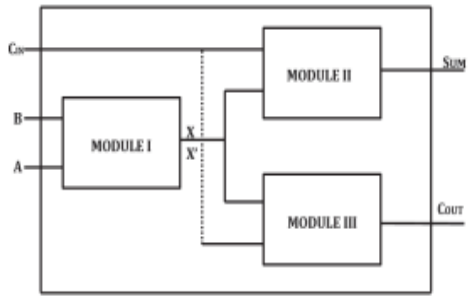

Fig. 1. Block diagram of hybrid logic FA circuit.

According to the hybrid design aesthetic, the FA structure is separated into three modules, as seen in Fig. 1. Full-swing XOR and XNOR outputs are generated simultaneously in Module I from the usage of two input signals (A and B). These signals need to be XOR-XNOR and have excellent driving capabilities since they need to drive two further units. The sum-and-carry circuits in Modules II and III produce the sum-and-carry outputs (COUT), respectively, using the outputs of Module I and the third input signal (CIN). The fundamental benefit of hybrid designs is that each module may be improved at the individual level. Additionally, by using fewer transistors, internal power-dissipating nodes can be decreased. Although hybrid Style FAs function on with single units or small chains, they lack the potential to drive installed higher bit adders by means of cascading steps.

Module I

In Module I, two input signals (A and B) are employed to concurrently produce full-swing XOR and XNOR outputs. These XOR-XNOR signals need to be powerful drivers since they must drive the other two modules. Using the outputs of Module, I and the third input signal (CIN), Modules II and III are the sum and carry circuits that generate the sum and carry outputs (COUT), respectively.

Module II

The outputs of the XOR-XNOR circuit and CIN may be used as input signals to construct Module II (SUM circuit) using the formula in (7). The primary requirement for this module is that the following gates have adequate driving power:

$$SUM=(A\oplus B)\oplus C_I^{r}{}_N+(A\oplus B)^{r}\oplus C_{IN}$$

Module III

Carry circuit (COUT) is the FA's third module. The outputs of modules I's XOR and XNOR, as well as earlier carries CINOR and CIN, may be used to determine the FA's output carry. Because this module's output depends on the previous FA's output carry, its delay has the most impact on the total delay in cascading systems.

$$C_{OUT}=(A\oplus B)^{r}A+(A\oplus B)C_{IN}$$

III . EXISTING SYSTEM

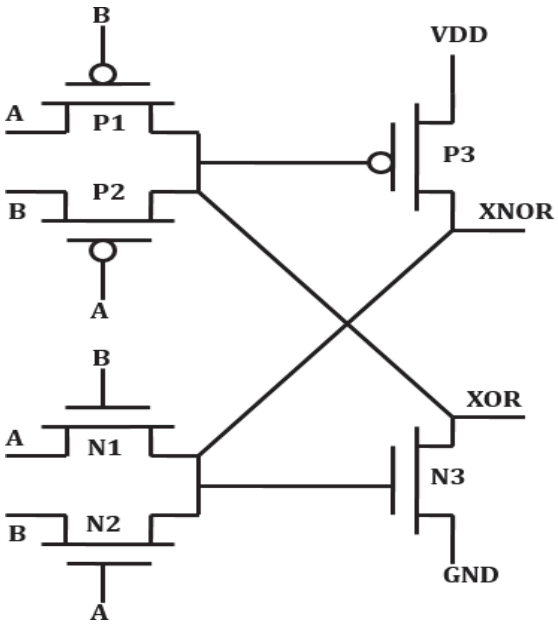

Fig: 2 XOR-XNOR Circuit with 6 transistors

We offer an XOR-XNOR circuit that

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generates XOR-XNOR outputs simultaneously utilizing CPL. The feedback transistors in this circuit are used to recover the output voltage levels. However, the feedback transistor maintains the delay and power higher. The important route's NOT gate was eliminated, however the cross-coupled design still results in a greater circuit delay. The weak logic in the complementary output nodes (XOR-XNOR) is restored by building the XOR-XNOR circuit with just six transistors and two complementary feedback transistors.

when either "00" or "11" (the same value) is present in both inputs. For the inputs "11" or "00," this circuit has a significant worst-case delay because in these scenarios, the outputs reach their ultimate voltage level in two stages. At the XOR and XNOR output nodes, two more NMOS and PMOS transistors can be used to overcome this problem. This circuit provides good driving capability, lower critical path delay, however power dissipation remains higher (This circuits required external inverter). By proposed low power high speed full adder by proposed XOR-XNOR we eliminate external inverter.

Numerous researchers have proposed hybrid logic-based FA systems, which provide the optimum performance without compromising output. According to Vastrabacka et al. [9], a 2-to-1 multiplexer circuit was utilized to implement the sum and carry modules in an XOR-XNOR module that utilized pass transistor logic (PTL).

Zhang et al. [10] used PTL to simultaneously construct XOR-XNOR outputs and C-CMOS style to manufacture carry modules in their hybrid FA cell. The XOR-XNOR circuit was used in another design, a new low-power and high-speed (LPHS) adder. using feedback transistors, whereas the sum and carry modules are constructed using PTL and a 2-to-1 multiplexer, respectively.

Six transistors were all that were needed for the XOR-XNOR circuit that Radhakrishnan proposed at this design, when both inputs have the same value (either "00" or "11"), two complimentary feedback transistors are utilised to restore the weak logic at complementary output nodes (XOR and XNOR). The inputs of this circuit have a significant worst-case delay. When "11" or "00" is used, outputs take two steps to achieve their ultimate voltage values. Valashani and Mirzakuchaki[14] who utilised an inverter, significantly enhanced the construction of an XOR-XNOR circuit. This structure offers a shorter critical path latency, but power dissipation is still larger.

The XOR-XNOR circuit was upgraded by Naseri and Timarchi [15], and it is now made up of 12 transistors. Compared to previous circuits, this one uses less power and has superior latency performance. However, this circuit requires an extra inverter. Eliminating this external inverter will considerably enhance the circuit's performance. This article suggests a brand-new XOR-XNOR circuit that features robust driving capabilities and full-swing XOR-XNOR outputs without requiring any external inverters. The internal NOT gate and feedback circuitry in this design help to achieve full-swing output for each transition. By carefully sizing different transistors, the power consumption and latency of the suggested circuit are both reduced.

II. Proposed XOR–XNOR Circuit

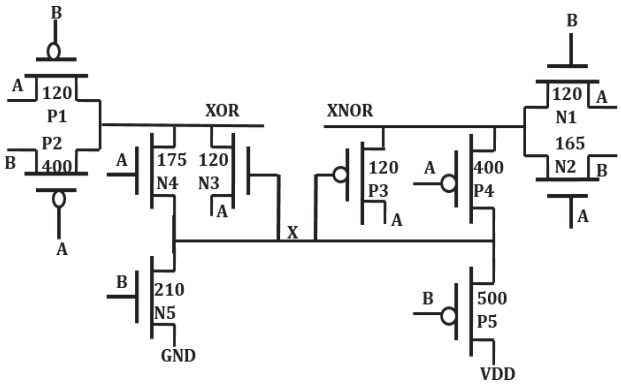

Fig: 3 Proposed XOR-XNOR circuit

Inputs AB	Path		Path	
	XOR (Full Swing)	XOR	XOR	XNOR (Partial Swing)
00	N3			-
01	P2	-	N1	P4, P3
10	P1	N4, N3	N2	-

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11	N4, N5	-	P3	N1,N2

Table 1 The various input combinations charging and discharging routes

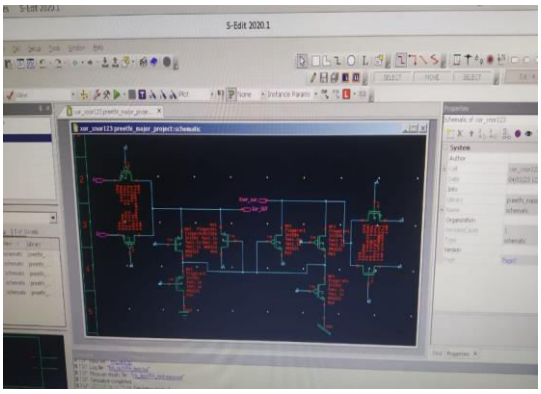
A variety of XOR-XNOR circuit design techniques have recently been developed; they are presented. A full-swing output is produced by an XOR-XNOR circuit [13]. In Fig., just six transistors are utilised. The CPL logic and feedback restorer transistors used to build this system. For the inputs, it offers good delay performance. AB: "01" and "10."

For the inputs AB: "11" and "00," there is a switching delay at the output, though. Two NMOS and two PMOS transistors were included into the circuit to solve the issue with higher levels, as shown in Fig. Naseri and Timarchi's[15] technique is utilized to address the delay for these inputs. Contrarily, the latter design not only tackles the issue of delayed responsiveness but also lowers the circuit's power consumption. However, it requires input A, which necessitates the usage of an extra inverter. This section introduces the special XOR-XNOR circuit, which generates the inverted input internally and does not call for any external inverters. This configuration decreases the total delay and power consumption of the XOR-XNOR circuit by using fewer internal nodes and transistors. It displays the 10-transistor (10-T) XOR-XNOR circuit that is advised.

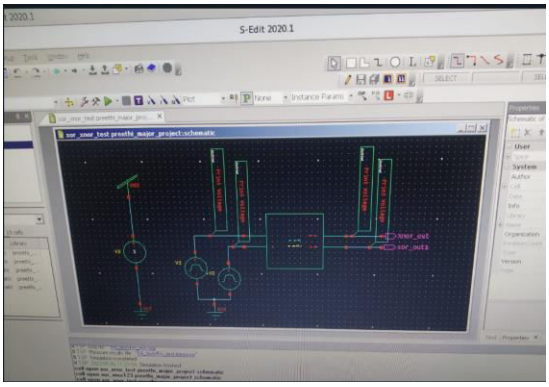
The XOR-XNOR circuit that has been suggested is based on a CPL and cross-coupled construction. On the XOR output side, it utilizes two PMOS (P1 and P2), three NMOS (N3, N4, and N5) transistors, while on the XNOR output side, it uses two NMOS (N1 and N2), three PMOS (P3, P4, and P5) transistors.

P1 and P2 are coupled in parallel as PTLs at the XOR together with N4, N5, a restorer that generates an output with full swing, and N3, a feedback transistor. The N1 and N2 transistors are similarly coupled in parallel as PTL, P4, and P5, and are stored to produce a full swing output, while the P3 acts as a feedback transistor at the XNOR output side. This circuit simultaneously produces two full-swing XOR-XNOR outputs.

V.SIMULATION AND RESULTS



Proposed XOR XNOR Schematic



Proposed XOR XNOR test bench

Proposed XOR XNOR waveform

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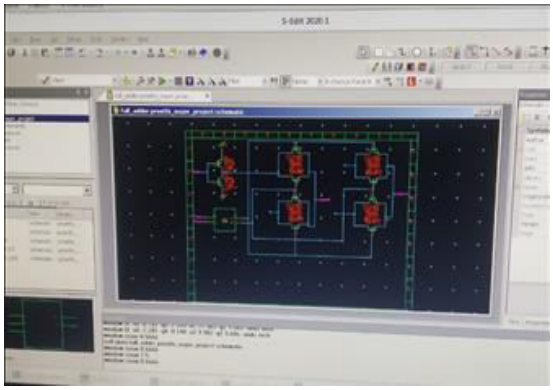
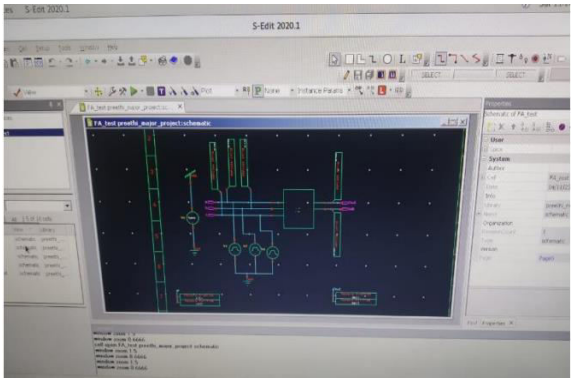


Proposed Full Adder Schematic



Proposed Full Adder Test Bench

Proposed Full Adder Waveform

V. CONCLUSION

This article introduces a brand-new 10-T XOR-XNOR circuit that simultaneously produces two full-swing outputs. Using the suggested XOR-XNOR circuit, new FA cells based on hybrid logic design approaches were also created. By simulating the proposed XOR-XNOR circuit and the FA cells in Tanner with 90 nm CMOS technology, their performance was evaluated. The recommended XOR-XNOR circuit's latency and PDP dropped by up to 65.16% and 70.13%, respectively, in comparison to comparable designs. The suggested FA design outperformed existing FAs in terms of PDP by 28% to 45%. The efficiency of the hypothesised FA cells in cascaded connections was also evaluated with 2-bit and 4-bit cascading chains; nevertheless, with an 8-bit cascading chain, the hypothesised FA design performed best. The suggested FA cell performed better than the existing FA cells.

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