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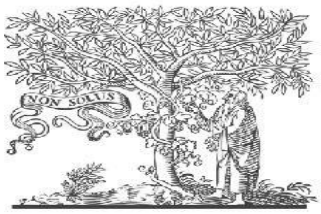

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Paper Authors

A.Sai Sruthi, G.L.Madhumathi

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IMPLEMENTATION OF COMPARATOR USING GATE DIFFUSION INPUT

A.Sai Sruthi[1], G.L.Madhumathi[2]

[1]P.G Scholar. ECE., Dhanekula Institute of Engineering and Technology.
[2] Professor. ECE., Dhanekula Institute of Engineering and Technology.

ABSTRACT: A digital comparator with a 300-mV output voltage and an auto-shutdown feature was presented. Traditional 180-nm Tanner EDA software was used for the design simulation. Measurement results show that the auto shut down comparator consuming a total power of 2.9 µW with the clock gating network. The input to the comparator that uses only 5.07pW provides even greater power-saving advantages. Moreover, the simulated GDI based comparator need fewer transistors compared to the clock gating comparator.
Keywords: Comparator, Clock gating network, Gate Diffusion Input

I. INTRODUCTION

Today's technology-driven society has seen an increase in the use of portable gadgets like laptops and smartphones. The schematic design of these mobile gadgets has become increasingly concerned with power and space consumption before they are implemented in the layout. Electronic devices, such as smartphones and portable PCs, have limited battery and storage capacities—power and area requirements for VLSI applications like bioelectronic circuitry and nano-electronics. Consequently, new VLSI design techniques and methodologies are necessary to manage and limit power and area usage. [1]-[2]. Implementing the comparator using a parallel adder ([3]). 56 transistors are used to build the comparator design, which is very difficult. LaxmeeshaSomappa [4] proposed a new technique to reduce the transistor count and improve power consumption. [5] Comparing the proposed GDI comparator to a clock gating comparator, the suggested GDI comparator consumes less power.

Interface circuitry between analog sensors and digital processing is a key component of an ADC (analog-to-digital converter). ADCs that are small, low-power, and energy-efficient must be utilized in portable and wearable devices to ensure their long lifespan. CTDSM and DTDSM-based ADCs are also worth consideration. SAR ADCs have good energy efficiency, but the frequency array perfectly matched requirement limits the overall device size[6]. The SAR ADC's capacitor bank necessitates an antialiasing filter, which results in inefficient power and area consumption. Antialiasing filters can be eliminated and matching requirements reduced with a CTDSM, resulting in less area and power use. With a passive switching capacitor integrator, a low-power DTDSM is possible [7] and [8]. Because of the vast range of capacitor values required, integrators require a large area to be implemented. In [9], a higher-order DTDSM based on an active-passive integrator is explored. 73 W of power is needed for an effective modulator on the other. In [10], third-order DTDSM is realized through the use of bulk-driven OTA's. In order to make a low-voltage comparator, the MOSFET stacking must be reduced while the power consumption is reduced to a level.

In this study, a low voltage and low power auto shut down comparator based on a unique clock gating network and Gate Diffusion input is developed and simulated in a standard Tanner EDA tool version 16.01 utilizing 180nm technology.

The GDI-based Comparator has a variety of advantages, including a lower number of transistors and a lower power consumption. There are five main components to this study. Section I introduces the comparator and the analogue-to-digital converter, as well as a literature review. Section Ii describes the clock-gated low-voltage auto-shutdown comparator. The fundamentals of gate diffusion input are discussed in Section III. Section IV proposes a comparator based on the GDI. Section V shows the performance analysis of clock gating comparator and proposed GDI based comparator. Section VI concludes the paper with results.

II. AUTO SHUTDOWN COMPARATOR FOR LOW VOLTAGE WITH CLOCK GATTING SYSTEM.

PMOS input pair, inverter-based latch, and inverter auto-shutdown comparator were all shown in the Fig. 1 layout pMOS inputs reset clock-gating network switches, which reset the clock-gating network switches. As soon as the input and output pMOS pairs have been resolved and brought to near logic levels, an automatic shut-off mechanism is started, shutting down both pairs. The comparator

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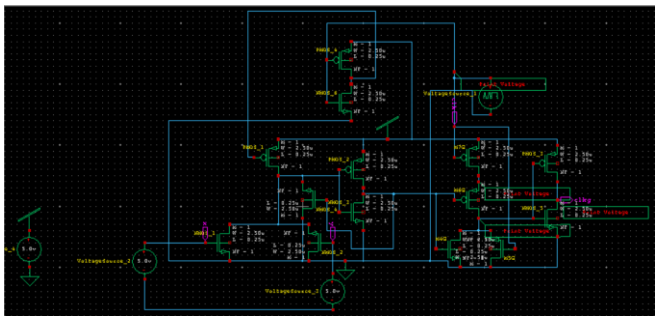
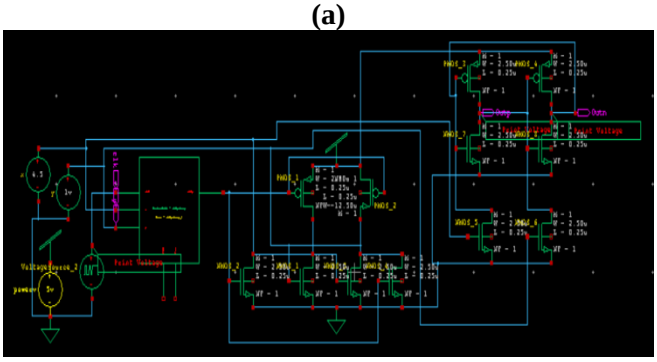
ensures that no static current flows from the VDD to the ground once the comparator has determined that it is secure. There must be no interference between the comparator and the gating network's working clock edge. When the auto-shutdown comparator is activated, it performs the following four stages: This is depicted in Fig. 2, where the clock-gating network is in motion. This diagram illustrates the output voltage waveform of a 300-mV-powered comparator and the clock-gating network. In Fig. 3, the input dc voltages are X=4.5V and Y=1V. As shown in Fig 4, the input dc voltage conditions are input X=1V and input Y=3.9V.



(a)



(b)

Fig.1 (a) Clock gating network and (b) the nMOS comparator with a cross-coupled latch and the gating network for the clock.

A. Phase I: Predischarge

A new phase begins when the input clock is set to a high logic level (logic high). On the "Event" node, the charge will be set to zero. The input clock will be completely obliterated once this has been achieved. For nodes X and Y, the pMOS input pair CLK G is logic high, maintaining them in their basic reset condition.

B. Phase II: Clock Transparent, Input Sampled

MOSFETs M6G and M7G are also turned-on during Phase II of the investigation. CLK G's PMOS inputs may be seen when the input clock is low due to MOSFETs M6G and M7G and an inverter. Due to the lack of a pMOS input pair, the input is only sampled at this location. Ending phase two occurs when the sampled information is about to regenerate the two nodes. C.

Phase III: Comparator Active, Decision Latched

Phase III is characterized by "CLK G" continuing at a very low level and regeneration of the comparator. Node "Event" will be pulled into logic 1 if either node X or Y is regenerated to a high logic level by the MOSFET M1G or M2G. M4G is engaged, and the pMOS input pair's clock is began to slow down.As a result of X and Y's decision, nodes OUTP and OUTN are held in the new state. At the end of this phase, the keeper MOS Mk, which is weaker than the MOS M4G, begins to activate.

D. Phase IV: Input and Regeneration MOSFET Shut Down

When the current phase's "CLK G" becomes high, it resets the cross-coupled nMOS regenerate pair and the input pMOS pair. Phase IV comes to an end when the input clock hits a logic high. (start of Phase I). As a result, the MOSFETs M1G and M2G have been turned off. The keeper MOSFET then holds the node "Event" at logic 1.Since low Vt MOSFETs are employed to create the clock gating network, the node "Event" can alter logic levels in the FF process region due to leakage currents.

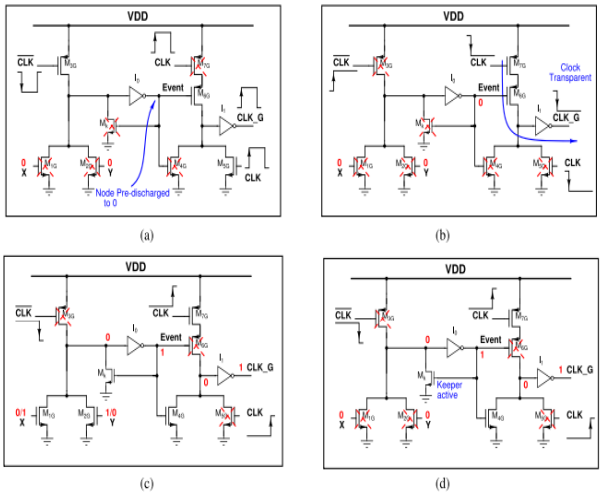


Fig2. The clock gating network's four stages are shown in this diagram.(a) Phase I: Predischarge. (b) Phase II: Clock-free input is sampled using a comparator. (c) Phase III: the comparator is running and the choice has been made. (d) Phase IV: Shutdown of the comparator input and regeneration pairs.

Comparator auto-shutdown requires a significant number of transistors, as seen in Figure 1. GDI approach is used to build an auto shutdown comparator to tackle this problem of a high transistor count consuming more power and taking up a lot of space.

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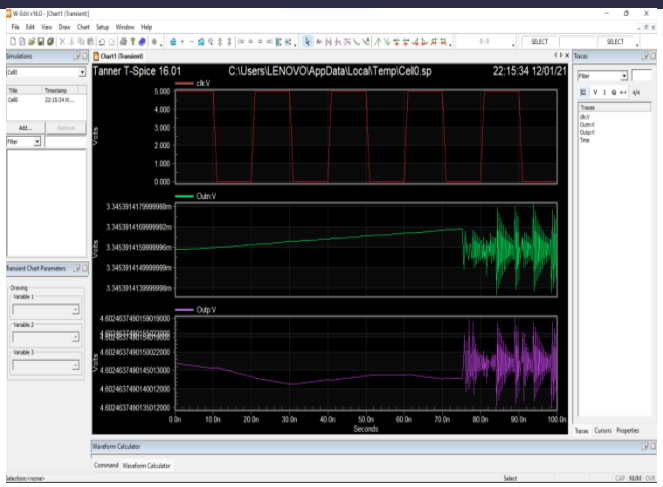

Fig 3: Output waveforms when X=4.5V & Y=1V

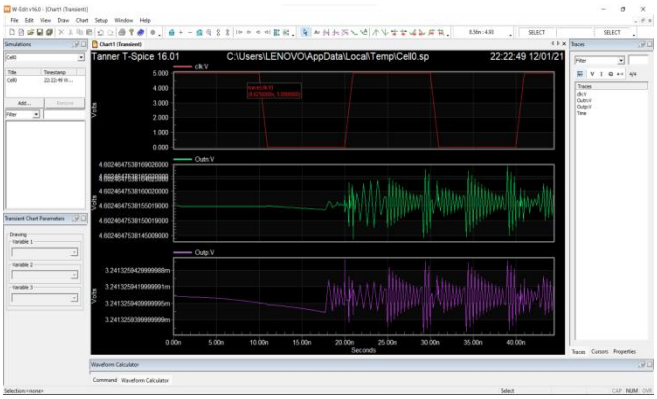

Fig 4: Output waveforms when X=1V & Y=3.9V

III. GATE DIFFUSION INPUT(GDI)

GDI (Gate Diffusion Input) - A new method for designing low-power digital circuits has been described. Digital circuits can be reduced in power consumption, response time, and area while keeping low complexity of logic design using this method.

In the GDI approach, the cell depicted in Fig 5 is used. There are a few key distinctions between the basic cell and the conventional CMOS inverter.

(1) GDI cell contains 3 inputs - G (common gate input), P (input to the PMOS source/drain), and N (input to the nMOS source/drain) are included in this classification.

(2) Configuration is possible because N and P are directly connected to both nMOS and PMOS. In CMOS inverters, there are no linked bulks. Some operations are not feasible with the normal CMOS process, but can be implemented with twin-well CMOS or SO1 technology.

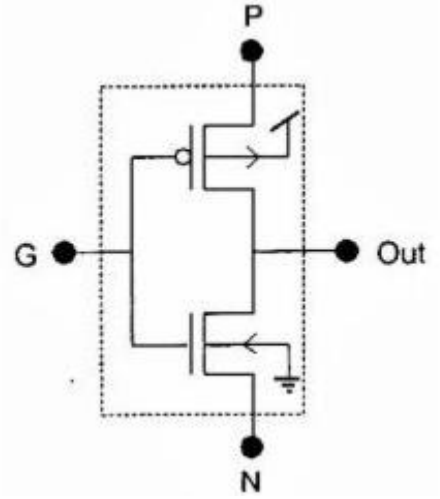

Fig 5: GDI basic cell

Table 1 An input configuration modification can yield widely varied Boolean functions for the same GDI cell, as shown in this example. A conventional CMOS implementation of these processes requires six to twelve transistors, but only two transistors with the GDI design method.

The table shows that utilizing the GDI technique AND, OR, Function 1, Function 2, XOR, XNOR may be more efficiently implemented. There are only two transistors in each of GDI's universally assigned functions 1 and 2.

The FI and F2 functions were used frequently in the construction of the circuits.

$$F1=\overline{A}.B$$

$$F2=\overline{A}+B$$

The reasons for this are as follows:

(1) In both F1 and F2, all of the logic families are included (allows realization of any possible 2-input logic function),

(2) Due to the continuous biasing of all nMOS transistors, F1 is the only GDI function that can be implemented in p-well CMOS technology.

Table I. GDI cell logic functions for different input configurations.

N (1st dedicat.)	P (2nd dedicat.)	G (Cmn.)	D	Function
Low	B	A	$\overline{A}B$	F1
B	High	A	$\overline{A}+B$	F2
High	B	A	$A+B$	OR
B	Low	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
Low	High	A	$\overline{A}$	NOT

GDI cell structure differs from the conventional PTL approaches and includes various

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essential properties that allow advances in design complexity level, transistor count, static power consumption, and logic level swing.

IV. PROPOSED GDI BASED AUTO SHUTDOWN COMPARATOR

Figure 6 illustrates our suggested dual-comparator circuit in its entirety. The n-FETs M2 to M5 are shown as two complementary MOSFETs that reflect the Ix current to the output branch. They're called supportive because they are (M1 and M2). There are also six additional MOSFETs in the circuit for further processing. N-FETs M2 and M4 show similar Vgs, indicating that they are both saturated in most of the circuit's operational range. Due to M3 and M5 sharing the same source voltages, the current mirror can produce an exact replica of Ixm. M2 and M4's ohmic-zone mirroring will be somewhat out of sync with high Vin levels.

The constant current Ic is subtracted from a duplicate of Ix, Ixm. Vout's output current is Ic minus Ixm, or Ic minus Ixm. In order for the output voltage Vout to change sign, IcIxm must change. The speed at which Vout can change from Vdn to Vdd is determined by the pull-up transistor M6 (carrying Ic). It is possible to have two values of Vin that satisfy the requirement Ix = Ic.

To first order approximation, these values are:

$$V_{dn}^{t} \triangleq \frac{1}{k}\left(U_T \ln \frac{I_C}{I_{0n}} + V_{dn}\right) \quad \text{—— (1)}$$

$$V_{up}^{t} \triangleq \left(V_{up} - U_T \ln \frac{I_C}{I_{0n}}\right) \quad \text{—— (2)}$$

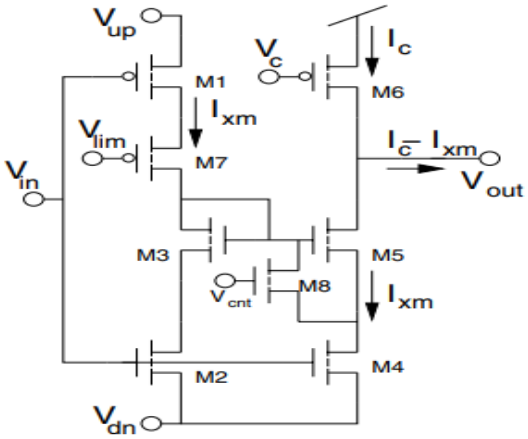

Fig6: GDI based COMPARATOR

Taking into account that $I_c = I0p\ \exp\kappa(V_{dd}-V_c)/U_T$ and assuming I0n=I0p the above equations can be further simplified to:

$$V_{dn}^{t} = (V_{dd} - V_c) + \frac{V_{dn}}{k} \quad \text{—— (3)}$$

$$V_{up}^{t} = V_{up} - (V_{dd} - V_c) \quad \text{—— (4)}$$

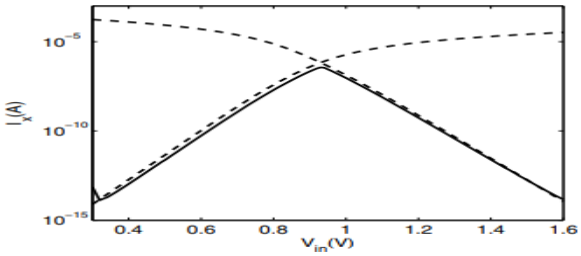

Fig7: Drain current for individual pand n-FETs as a function of Vgs (dotted lines) and the consequence of merging them on one branch (solid line). Voltages Vup and Vdn are 1.6 volts each.

TABLE 2: power consumption performance at different conditions

The equations (3) & (4) provide us with two simple expressions for V_{dn} and V_{up} that should be used to determine the desired switching point. If the difference between Vup and Vdn is large, transistors can enter the strong inversion domain, allowing the maximum peak Ix to reach very high values.

In order to keep the transistors in the weak-inversion regime and limit the maximum current dissipation, we employed an extra nFET (M7) with an adequate constant voltage Vlim. It is also possible to totally disable the comparator using the n-FET M8 and Vcnt control signal. There are two ways in which this can be done: by shorting out the Vgs of one of the mirrors (M3), or by pulling the output node Vout high (M6), which finally brings M6 into the triode area of operation and closes it down.

V. SIMULATION RESULTS & DISCUSSION

It was done using Tanner EDA software, version 16.01, with an input voltage range of 0. An automatic shutdown comparator that uses a GDI interface and is gated by the clock will operate in the range of V to 5V. Power consumption at varied input voltages, i.e., x>y and XY, is simulated using the proposed GDI automatic shutdown comparator design.The output waveforms are displayed in fig. 8, 9. As shown in Table 2, the suggested GDI auto shut down comparator uses less power than the more traditional clock gated auto shut down comparator.

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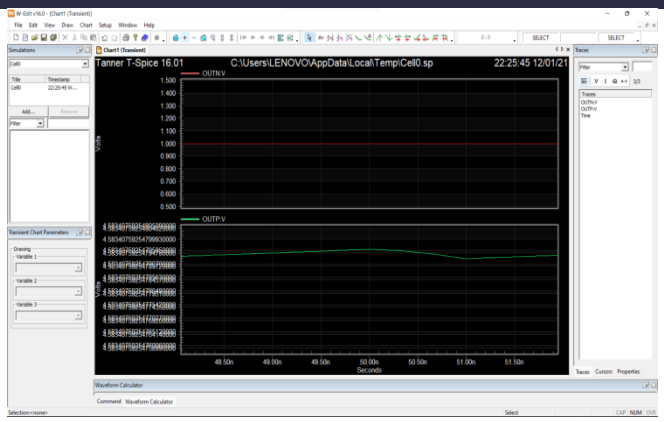

Fig 8: Output waveforms when X>Y

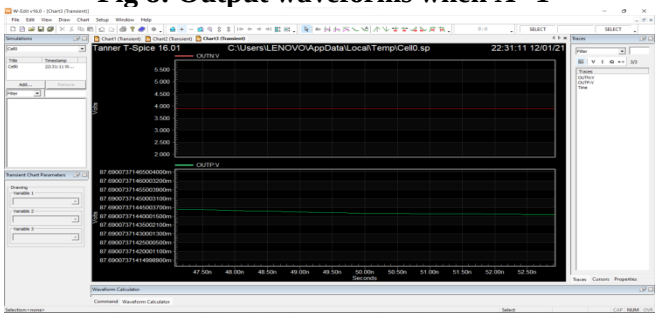

Fig 9: Output waveform when X<Y

Technique used		Clock gating comparator		GDI Comparator	
conditions		X>Y	X<Y	X>Y	X<Y
Inputs	X	4.5v	1v	4.5v	1v
	Y	1v	3.9v	1v	3.9v
power		2.9µW	2.8µW	5.07pW	2.7pW

VI. CONCLUSION

In Tanner EDA tool version 16.01 employing 180nm technology, a gate diffusion input (GDI) was used to build the auto-shutdown comparator. It has been proved that the suggested GDI auto shut down comparator circuit performs better than the present clock gated auto shut down comparator.When it comes to power consumption at different input voltages, the clock gated auto shutdown comparator and the proposed GDI auto shut down comparator are compared, and the proposed GDI auto shut down comparator consumes less power than the clock gated auto shutdown comparator at all voltages. Due to the reduced size, more efficient GDI comparator placements and routing algorithms will be possible, which means shorter interconnects and less cross-talk. As a result, the suggested comparator based on the GDI approach consumes less power and occupies less space than a clock-gated comparator. As a result, this novel design is a viable option for a low-power system.

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